Basic Electrical and Electronics Engineering

About the Authors

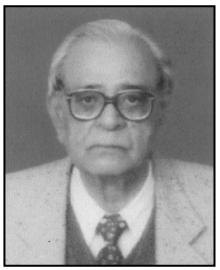
D P Kothari is presently Director–Research, MVSR Engineering College, Hyderabad. He obtained a BE (Electrical) in 1967, ME (Power Systems) in 1969 and PhD in 1975 from the Birla Institute of Technology and Science (BITS Pilani), Rajasthan. From 1969 to 1977, he was involved in teaching and development of several courses at BITS Pilani. Dr Kothari has also served as Director General–Raisoni Group of Institutions, Nagpur; Emeritus Director General, Vindhya Institute of Technology and Science (VITS), Indore; and Vice Chancellor–Vellore Institute of Technology (VIT), Vellore. He has also served as Director In-charge and Deputy Director (Administration) as well as Head Centre for Energy Studies at Indian Institute of Technology Delhi; and as Principal–Visvesvaryaya National Institute of Technology, Nagpur. He was Visiting Professor at the Royal Melbourne Institute of Technology, Melbourne, Australia, during 1982–83 and 1989 for two years. He was also NSF Fellow at Purdue University, US, in 1992.

Dr Kothari, who is a recipient of the *Most Active Researcher Award*, has published 780 research papers in various national as well as international journals, conferences, guided 40 PhD scholars and 65 MTech students, and authored 32 books in Power Systems and other allied areas. He has delivered several keynote addresses and invitee lectures at both national and international conferences on Electric Energy Systems. He has also widely popularised science and technology through 42 video lectures on YouTube with a maximum of 30,000 hits!

Dr Kothari is a Fellow of the Indian National Academy of Engineering (FNAE), Fellow of Indian National Academy of Sciences [FNASc], Fellow of Institution of Engineers (FIE) and Hon. Fellow, ISTE, and Fellow IEEE.

His many awards include the National Khosla award for Lifetime Achievements in Engineering (2005) from IIT Roorkee. The University Grants Commission (UGC), Government of India, has bestowed the UGC National Swami Pranavananda Saraswati Award (2005) on Education for his outstanding scholarly contributions.

He is also a recipient of the Lifetime Achievement Award (2009) by the World Management Congress, New Delhi, for his contribution to the areas of educational planning and administration. His fields of specialization are Optimal Hydro-thermal Scheduling, Unit Commitment, Maintenance Scheduling, Energy Conservation (loss minimization and voltage control), and Power Quality and Energy Systems Planning and Modelling.



I J Nagrath is Adjunct Professor, BITS Pilani, from where he retired in July 1999 as Professor of Electrical Engineering and Deputy Director. He is now actively engaged in writing books related to his long teaching and research experience.

Prof Nagrath obtained his BE with Honours in Electrical Engineering from Birla Engineering College in 1951, and MS from the University of Wisconsin, USA, in 1956.

He has co-authored several successful books, which include *Electric Machines*, 4/e, *Modern Power System Analysis, Power System Engineering,* 2/e*, System Modeling and Analysis and Electrical Machines*, 2/e (Schaum's Outline Series) and has authored Basic Electrical Engineering, 3/e (all published by MHEI). He has also co-authored *Control System Engineering* and authored *Electronics: Analog and Digital*. He has also published several research papers in prestigious national and international journals and continues to be active in studies and writing.

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Preface

The excellent response to the three editions of our book *Basic Electrical Engineering* has motivated us to bring out a book on Basic Electrical and Electronics Engineering that offers a panaromic purview of this popular first-year engineering course. The main aim was to provide the complete material on basic topics in electrical and electronics engineering in one volume to students and teachers of all branches of engineering.

Aim of this Book

The objective of this book, like our other books, is to give an exhaustive exposition of the fundamental concepts, techniques and devices in Electrical and Electronics Engineering. In attempting to do so, we have covered the basic concepts in Electric Circuit Theory, Electrical Machines, Electronics, Communication Engineering and Computers in a single volume.

Target Audience

The book attends to the basic course in EEE of almost all Indian technical universities and some foreign universities as well. It is particularly well suited for undergraduate students of all engineering disciplines. Diploma students of EEE and ECE will find it useful too. The specialty of the book is that it covers very basic as well as advanced topics in Electrical and Electronics Engineering. The book can be used for a single course (basic Electrical /Electronics) at the basic level for all branches of engineering.

Salient Features

The highlights of this book are its rich pool of pedagogical features, large number of solved problems in all the 30 chapters, along with numerous review questions, additional solved problems and multiple-choice questions. A brief look at the highlights follows:

- ❏ Emphasis on delivering the preliminaries of electrical and electronics engineering
- ❏ Span of coverage ensures introduction to all important subject areas in the field
- ❏ Highly pedagogical exposition of subject area:
  - Over 775 illustrations
  - 290 Solved Examples
  - 466 Review Questions
  - 290 Numerical Problems
  - About 300 Multiple-Choice Questions and other Objective-Type Questions

Chapter Organisation

The book, spanning over 30 chapters and 2 appendices, has been structured to provide in-depth information of all the concepts with appropriate pedagogy. **Chapters 1 to 5** are on Electric Circuit Theory; **chapters 6 to 10** cover Transformers and Electrical Machines. **Chapter 11** is on Measuring Instruments and Electric and Electronic Instrumentation. **Chapter 12** provides in-depth understanding of Power Systems. **Chapter 28** deals with the Basics of Computers. **Chapter 30** tells the story of Communication Engineering. The rest of the chapters explain the basic concepts of various topics in Electronics Engineering. Some useful appendices have been provided for easy reference.

Online Learning Center

The book is accompanied by an online learning center, available at *http://www.mhhe.com/kothari/beee* that offers valuable resources for instructors and students.

❑ **For instructors**

- Solution Manual
- Chapterwise PowerPoint slides with diagrams and notes for effective presentation

❑ **For students**

- Chapter on 'Control System (Chapter 31)'
- Links to reference material
- Chapter outlines for quick revision during the examinations

Acknowledgements

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Special note from Dr Kothari

He wishes to place on record his gratitude to his colleagues at IIT, Delhi; VIT, Vellore; VITS, Indore; RGI, Nagpur; JBIET, Hyderabad and MVSR Engineering College, Hyderabad, for help in preparing rough drafts of certain portions of the manuscript and in working out the solutions of examples and unsolved problems of certain chapters.

Feedback

We look forward to receiving suggestions and constructive criticism from teachers and students at the publisher's email id, mentioned below.

D P Kothari
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Piracy-related issues may also be reported.

Elementary Concepts and Definitions

chapter 1

Goals & Objectives

- Definition of electrical quantities and their units
- Understanding the relationship between charge, voltage, current and power
- Acquiring capability to work with sign convention—voltage and current
- The dc and ac current and voltage; characteristics of sinusoidal waveform universally used for ac currents and voltages
- Resistor and Ohm's laws, in relation to inductor and capacitor
- Acquiring ability to employ basic circuit laws—Kirchhoff's Current Law [KCL] and Kirchhoff's Voltage Law [KVL]
- Ability to deal with independent and dependent sources

1.1 INTRODUCTION

Electric energy is convenient and efficient for production of light, mechanical energy and is also used in information processing. For the first two uses, it can be transported economically and in a clean fashion (as compared to transporting coal, for example) over long-distance lines to be available at the point of use. Electric energy also can transport information over tremendous distances, with or without wires, equally efficiently and economically. There is almost no competitor to electric energy in these fields.

Electric energy does not occur naturally in usable form and must therefore be centrally generated and instantly transported to myriad points of use spread geographically over vast areas, even beyond state or national boundaries. It cannot be stored in large-enough quantities for any major use. Electric-energy generation is generally done through three processes:

1. Generating from naturally occurring chemically bonded energy as in fossil fuels (like coal and oil).
2. From nuclear energy, which is converted to heat form by combustion or nuclear fission. The thermodynamic cycle converts it to mechanical form (rotational) which is then employed to run an electric energy generator.
3. For limited use, electric energy is directly obtained from chemical energy, as in batteries, or solar energy is converted to electric energy as in a solar cell. The trend in electric energy generators is towards mega sizes, due to economy in large scales.

Information, usually visual or audio signals or coded messages, have to be processed and/or transported by the intermediate form of electric energy. Speed of processing and the economy dictate that the electric energy for these purposes must be in minutest possible quantities, in either continuous form or bit form (modern trend). Hence, the trend is towards micro sizes. Range and variety of such use of electric energy is varied and wide as in video and audio systems, control processors, computers, etc.

Fibre optics using light signals is beginning to offer stiff competition to electric energy for purposes of information processing. The end-use energy form of such systems would, for a long time to come, continue to be electric.

This being the first chapter, it begins by introducing the fundamental laws of electricity and conservation of energy. The concepts of electric charge, current, voltage and electric sources and power are clarified along with the sign convention. Idealised circuit elements such as resistance, capacitance and inductance are dwelled upon along with basic laws that govern their terminal behaviour. The practical circuit elements such as resistor, capacitor and inductor are introduced.

Interconnection of circuit elements leads to the concept of electric circuit. The two fundamental circuit laws lay the foundation stone of the circuit theory to which the first six chapters of this book are devoted. The chapter ends on the principle of superposition, homogeneity and concept of linearity.

The importance of circuit theory can be judged from the fact that almost all electric and electronic devices, transducers, transmission lines, energy and information processing systems, etc. are modelled in the form of a circuit with sources for the purpose of their analysis and design. Circuit modelling cannot be applied as such to very high-frequency devices (microwave equipment, etc.) where travelling-wave concept is necessary for their modelling.

In view of the above account, the electric circuit theory is fundamental to all fields of electrical engineering. An electric circuit on an analogic basis can model even some mechanical systems.

1.2 WORK, ENERGY AND POWER

Work

Work is done whenever an object moves in a field of force, F (unit of force is newton, N). If the object moves in the direction of force, work is done by the force. However, if the object moves in a direction opposite to the force, work is done by an external agency that moves the object.

Energy

It is the capacity for doing work. When a mass is lifted against gravity, work done by an external agency in lifting it gets stored in the mass as potential energy (by virtue of its position in the gravitational force field). If the mass is now allowed to fall, the potential energy will get converted to kinetic energy (associated with velocity). Further, if the mass were to fall on a wedge, it will drive the wedge into a piece of wood (say), thereby doing work. The process of doing work in some sense is a process of energy transfer. In the example cited above, energy is transferred from the external agency to the mass and gets stored as potential energy. When the mass falls, potential energy stored in the mass gets converted to kinetic energy. Upon hitting the wedge, some of the kinetic energy in the mass gets transformed to heat which is generated while driving the wedge against wood friction.

Energy W = force $N \times$ distance moved (m)

Therefore, the energy, W, is measured in unit of joules (J) or newton-metres (Nm).

❑ Kinetic Energy

$$\text{Linear } w = \frac{1}{2}mv^2 \text{ Nm}$$

m = mass of body, kg
v = velocity of body, m/s

$$\text{Rotational, } w = \frac{1}{2}J\omega^2$$

J = inertia of body, kg m^2
ω = rotational speed in rad/s

❑ Potential Energy

$$w = mgh \text{ Nm}$$

where m = mass of body, kg
g = acceleration due to gravity = 9.81 m/s^2
h = height above a reference point, m (say ground)

Principle of Conservation of Energy

In nonrelativistic processes, energy (w) never gets destroyed; it gets converted from one form to another as illustrated in the above example of the mass falling on the wedge.

Power

It is the rate of doing work (i.e. rate of transferring energy). Instantaneous power is

$$p = \frac{\mathrm{d}w}{\mathrm{d}t} \text{ J/s or watts (W)} \tag{1.1}$$

Average power is given by

$$P(\text{av}) = \frac{W}{T} \tag{1.2}$$

where T = time (in seconds) during which energy W flows

The integral forms of Eq. (1.1) are

$$W = \int_{t_0}^{t_0 + t} p\,\mathrm{d}t \tag{1.3}$$

$$P(\text{av}) = \frac{1}{T}\int_{t_0}^{t_0 + t} p\,\mathrm{d}t \tag{1.4}$$

1.3 BASIC MANIFESTATIONS OF ELECTRICITY

Fundamental electric-charge-carrying particles are electrons (negative charge) and protons (positive charge). The unit of electric charge is coulomb, C. In terms of this unit, the electronic charge is 1.602×10^{-19} C (–ve for electron and +ve for proton). Since coulomb is a large unit, it is more practical to use micro-coulomb, μC.

An *electric field* is established in the space surrounding an electric charge and is manifested in the form of force exerted on another charge brought into the field. This force is given by *Coulomb's law* as

$$F = \frac{Q_1 Q_2}{4\pi\varepsilon d^2}\text{N} \tag{1.5}$$

where Q_1, Q_2 are charges in coulombs,

d is the distance between them in metres, and

ε is the permittivity of the medium ($= \varepsilon_r\varepsilon_0$; ε_r = *relative permittivity* of medium and ε_0 = *permittivity of free space* = 8.85×10^{-12}).

When we are dealing here with a stationary charge, the field is called *electrostatic fields.* The field at any point is measured quantitatively in terms of the force exerted on a unit positive charge and is called *electric field intensity* **E**, which is a directed quantity (vector).

Potential Difference

It is the work (J) done when a unit positive charge is moved from a point b in the field to another point a. As in the gravitational field, the potential difference or *voltage difference* between two points is a *scalar* quantity independent of the path chosen. The unit of potential difference is *volts* (V); 1 V = 1 J/unit positive charge. The symbol of potential difference (or voltage) is as v or V.

If work must be done on the charge (energy input to the charge) as it moves from b to a, the voltage of a is higher than that of b (voltage rises from b to a) and is indicated as v_{ab} (a above b) as in Fig. 1.1. In this case, if the charge moves from a to b, energy is output. Obviously,

$$v_{ba} = -v_{ab}$$

i.e. the voltage drops in going from a to b.

There are two ways of indicating the voltage difference on a diagram, as shown in Fig. 1.1. It can be indicated by a line with an arrow pointing towards the point whose voltage is higher than that of the other point (no arrow) by the symbol indicated on the arrow as in Fig. 1.1(a), or by arrows at both ends with + and – sign placed at the ends (points) as in Fig. 1.1(b).

Fig. 1.1 *Potential difference (voltage difference)*

The transfer of electric energy is associated with the motion of charges. In our circuit study, we will consider motion of charges confined to a definite path constituted of materials that are good conductors of electricity (aluminium, copper). Poor conductors of electricity are known as insulators and are used to wrap the conductors to prevent the charge from leaking away.

Current

Electric current is the rate of flow of charge through a conducting path as shown in Fig. 1.2. The *positive direction* of current is the direction in which *positive charge flows*; this direction is opposite to that in which *electrons* flow. Unit of current is *ampere*, A. One ampere is the charge flow rate of 1 C/second. The symbol used for current is i or I. The symbol for charge is q.

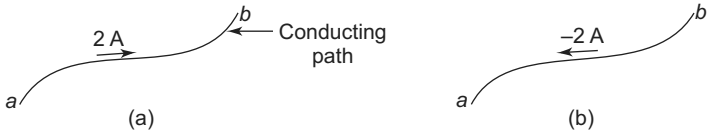


Fig. 1.2 *Current*

Average current over a period of time is

$$i(\text{avg}) = \frac{\Delta q}{\Delta t} \tag{1.6a}$$

while the instantaneous current is defined as

$$i = \frac{\mathrm{d}q}{\mathrm{d}t} \tag{1.6b}$$

The paths of interest along which charges move (flow) are known as *circuits*.

The charge transferred from time t_0 to t is

$$q = \int_{t_0}^{t} i \, \mathrm{d}t \tag{1.7}$$

As in Fig. 1.2(a), a reference positive direction is chosen for the current. The current in the opposite direction would then be negative as in Fig. 1.2(b). If a current is flowing from a point a to b, it may be indicated by the symbol i_{ab} (a to b). Obviously,

$$i_{ba} = -i_{ab}$$

We shall generally avoid such double suffix symbolisation.

Unidirectional current is known as *direct current* (dc) and, unless otherwise indicated, it is assumed to have constant value with time as shown in the graphical representation of Fig. 1.3.

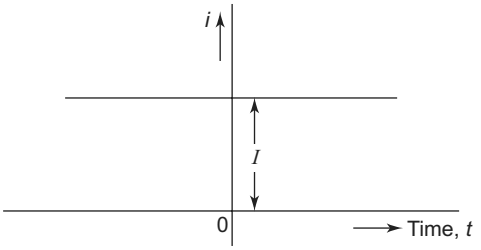


Fig. 1.3 *Direct current (dc)*

Alternating current or ac is cyclic in nature, with current flowing in positive direction in half the cycle

and in negative direction in the other half, as shown in Fig. 1.4. The current wave shape shown in Fig. 1.4 is sinusoidal, which is a very common occurrence in circuits. It can be expressed as

$$i(t) = I_m \cos\frac{2\pi}{T}t \tag{1.8}$$

where T = time period of one cycle in seconds
I_m = maximum (peak) current

It easily follows that the *frequency*

$$f = \frac{1}{T} \text{ Hz (cycles/s); Hz = hertz} \tag{1.9}$$

Equation (1.8) can now be rewritten as

$$i(t) = I_m \cos 2\pi ft \tag{1.10}$$

We can express *angular frequency* ω as

$$\omega = 2\pi f; \text{ frequency in rad/s} \tag{1.11}$$

so that $$i(t) = I_m \cos \omega t \tag{1.12}$$

where I_m = maximum or peak value of current

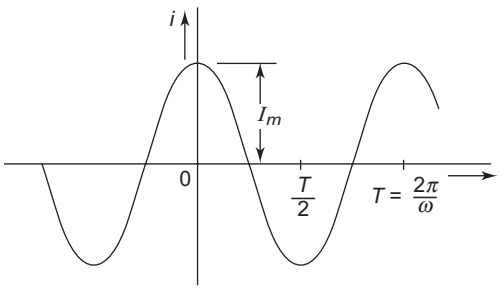


Fig. 1.4 *Alternating current (ac)—sinusoidal*

It is convenient to plot alternating current in the form of Eq. (1.12) with cordinate as ωt as in Fig. 1.5.

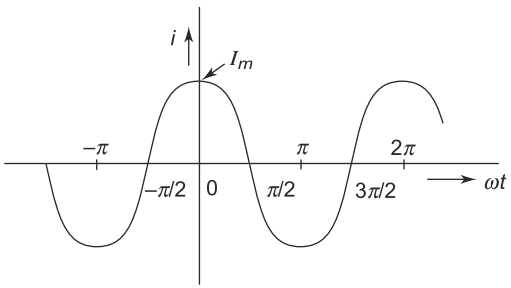


Fig. 1.5 *Alternating current—sinusoidal*

Mathematically, Eq. (1.12), as well as Eq. (1.8), can have any reference point so that in general,

$$i(t) = I_m \cos(\omega t + \theta) \tag{1.13}$$

where θ can be either positive or negative as shown in Fig. 1.6(a) and (b). θ is known as the *phase angle* of the current and causes the current wave to shift to right (lag) or left (lead) in time.

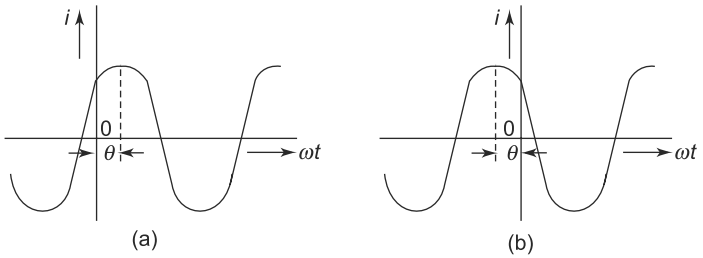


Fig. 1.6 *(a) $i(t) = I_m \cos(\omega t - \theta)$; lagging phase angle*
(b) $i(t) = I_m \cos(\omega t + \theta)$; leading phase angle

Relative Phase Angle

Consider the sinusoidal voltages

$$v_1(t) = V_m \sin \omega t \tag{1.14}$$

and

$$v_2(t) = V_m \sin(\omega t + \theta) \tag{1.15}$$

For phase-angle comparison, we choose any corresponding points on the two waves. It is convenient to choose the first zero value of $v_1(t)$ which occurs at $\omega t = 0$. The corresponding zero value of $v_2(t)$ occurs at $(\omega t + \theta) = 0$ or at $\omega t = -\theta$. We find that the zero point of $v_2(t)$ occurs earlier in angle by θ radians or in time by θ/ω seconds from the corresponding point of $v_1(t)$. It means that wave $v_2(t)$ leads $v_1(t)$ by angle θ radians or time θ/ω seconds. The two waves are sketched in Fig. 1.7 and the angle θ is indicated therein.

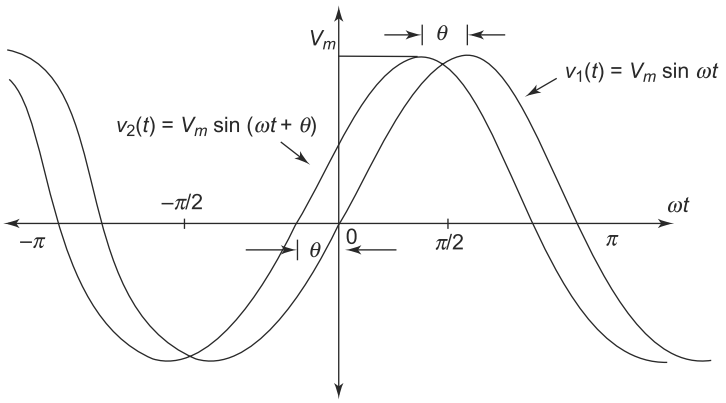


Fig. 1.7 *$v_2(t)$ leads $v_1(t)$ by angle θ*

It is not necessary to sketch the sine wave to determine the phase angle. Consider

$$v_3(t) = V_m \sin(\omega t - \theta)$$

The first zero occurs at $(\omega t - \theta) = 0$ or $\omega t = \theta$, i.e. later than the *reference sine wave* by angle θ. The reader may sketch $v_3(t)$ and observe.

For determination of relative phase angle, it is convenient to express both the waves as sines or cosines. For cosine waves, convenient corresponding points are where the cosine has unit value.

It is essential that the sinusoidal waves, being phase compared, have the same frequency.

In engineering applications, the phase angle θ is expressed in degrees. If the corresponding time is to be determined, it should be converted to radians.

Converting Sines to Cosines and Vice Versa

The sine and cosine are essentially the same function except for 90° phase difference. Thus,

$$\cos(\omega t - 90°) = \sin \omega t \tag{1.16}$$

It means that cos ωt with a lagging angle of 90° is sin ωt. In other words, cos ωt leads sin ωt by 90°. Adding 90° on both sides of Eq. (1.16), we find

$$\sin(\omega t + 90°) = \cos \omega t$$

which means sine with 90° lead is cosine.

Adding or subtracting 360° to the argument of cosine and sine does not cause any change in their values.

Adding or subtracting 180° to the argument of cosine and sine causes a sign reversal. Thus,

$$\cos(\omega t - 90° + 180°) = -\cos(\omega t - 90°) = -\sin \omega t$$

For example,

$$v_1(t) = V_{m1} \cos(15t + 20°);$$

$$= V_{m1} \sin(15t + 90° + 20°); \text{ sine with } 90° \text{ lead is cosine}$$

$$= V_{m1} \sin(15t + 110°)$$

Compare it with

$$v_2(t) = V_{m2} \sin(15t - 30°)$$

We find v_1 leads v_2 by (110° + 30°) = 140°. If we subtract 360° from the argument of v_1, we have

$$v_1 = y_{m1} \sin(15t - 250°)$$

which equivalently means v_1 is lagging v_2 by (–250° + 30° = –220°)

It is preferable to express the phase angle between sinusoids as an angle less than 180°.

Example 1.1

Find the angle by which i_1 lags v_1 if v_1 = 100 cos (100t − 40°) V and i_1 equals (a) 4 cos (100t + 20°) A, and (b) 1.5 sin (100t − 60°) A.

Solution

(a) Both are cosines. From Fig. 1.8(a), we can see i_1 lead v_1 by (20° + 40°) = –60°

(b) For phase comparison, we convert i_1 from sine to cosine form.

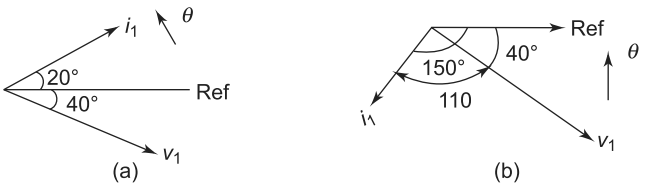


Fig. 1.8

$$1.5 \sin(100t - 60°) = 1.5 \cos (100t - 60° - 90°)$$
$$= 1.5 \cos (100t - 150°)$$

Comparing with

$$v_1 = 100 \cos (100t - 40°)$$

i_1 lags v_1 by $(150° - 40°) = 110°$ [Fig. 1.8(b)]

Example 1.2

Convert $50 \cos (120t - 45°) - 30 \sin (120t + 160°)$ to the following forms: (a) $A \cos 120t + B \sin 120t$, (b) $C \cos (120t + \phi)$.

Solution

(a) $$50 \cos (120t - 45°) = 50 [\cos 120t \cos 45° + \sin 120t \sin 45°]$$
$$= 35.36 \cos 120t + 35.36 \sin 120t \quad \text{(i)}$$

$$30 \sin (120t + 160°) = 30 [\sin 120t \cos 160° + \cos 120t \sin 160°]$$
$$= -28.19 \sin 120t + 10.26 \cos 120t \quad \text{(ii)}$$

Subtracting Eq. (ii) from Eq. (i), we get the result as

$$25.10 \cos 120t + 63.55 \sin 120t \quad \text{(iii)}$$

(b) We want Eq. (iii) in cosine form. So let

$$\left.\begin{aligned} 25.10 &= C \cos\phi \\ 63.55 &= C \sin\phi \end{aligned}\right\} \Rightarrow C = 68.33, \phi = 68.5°$$

Substituting in Eq. (iii),

$$C \cos \phi \cos 120t + C \sin \phi \sin 120t = C \cos (120t - \phi)$$

or

$$= 68.33 \cos (120t - 68.5°) \quad \text{(iv)}$$

Magnetic Effect of Currents

A current-carrying conductor exerts forces on other current-carrying conductors and on magnetic materials in its vicinity, which is explained by the presence of a magnetic field. A magnetic field by virtue of this force acts as a medium of energy transfer and is commonly employed for interconversion of electrical and mechanical energy. These ideas will be pursued in Chapter 7.

Electric and magnetic fields both exist simultaneously whenever moving charges are present; the electric field is caused by the presence of the charge, and magnetic field, by virtue of motion of the charge.

1.4 ELECTRIC ENERGY AND POWER

According to the definition of voltage, when a charge of q coulombs moves through voltage v volts from –sign to + sign (see Fig. 1.9a), it acquires energy

$$w = vq \ J \quad (1.17)$$

As it moves out of + terminal, it carries (or delivers) the energy to the circuit beyond. The electric power is the rate of delivering the energy and is given by the time derivative of Eq. (1.17). Assuming v to be constant, the instantaneous power delivered is

$$p = \frac{dw}{dt} = v\frac{dq}{dt}$$

or $$p = vi \text{ W} \tag{1.18}$$

This is illustrated in Fig. 1.9(a) where the current i is flowing out of the + terminal of voltage v. In other words, it means that the circuit is delivering power p.

If the current i flows into the + terminal of v, the power p is input to the circuit or the circuit is receiving power as illustrated in Fig. 1.9(b).

The average power over a period of time T is given by

$$P = \frac{1}{T}\int_0^T p\,dt = \frac{1}{T}\int_0^T vi\,dt \tag{1.19a}$$

when V and I are both constant (dc), the energy transferred (either way) in time T is

$$w = VIT \tag{1.19b}$$

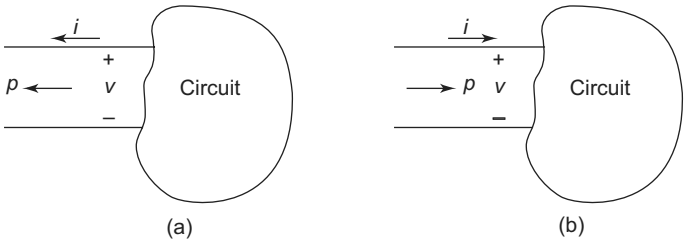


Fig. 1.9 *(a) Power output of circuit p = vi, (b) Power input to circuit p = vi*

Thermal Energy

Heat energy is indeed molecular vibrations of the substance. It is manifested as *temperature.* Depending on temperature a substance can have three forms—solid, liquid and gas.

Unit of temperature (T)

°C — Celsius

K—Kelvin = (273 + °C)

Zero degree Kelvin = –273°C

Unit of heat—calorie

One *calorie* in the amount of heat required to raise the temperature of 1 gram of water through 1°C. This is known as *specific heat* of water. Heat capacity, c, of any substance is the number of calories required to raise the temperature of 1 kg of it through 1°C.

Heat stored in a body

$$Q = McT \text{ cal} \tag{1.19c}$$

Heat Flow

Heat flows from a high-temperature region to a low-temperature region. The means of heat flows are

- **Conduction**—in solids
- **Convection**—in liquids and gases where a part of the substance moves to the lower temperature region

Rate of change of heat stored in a body is

$$q = Mc\frac{dT}{dt} - C\frac{dT}{dt} \tag{1.19 d}$$

where $C =$ heat calories conduced and/or convected away par deg temperature rise.
$Q \times T \neq$ heat power

1.5 SUPERPOSITION AND HOMOGENEITY

Principle of Superposition

An element or circuit obeys the principle of superposition if the net effect of the sum of causes equals the sum of their individual effects.

Mathematically, let cause x and effect y be related as

$$f(x) = y; f(.) = \text{function} \tag{1.20}$$

Let the cause be scaled by a sector a. Then, the functional relationship obeys **homogeneity**, if

$$f(ax) = \alpha f(x) = \alpha y \tag{1.21}$$

Consider two causes x_1 and x_2; then

$$f(x_1) = y_1$$
$$f(x_2) = y_2$$

Let the combined effect of these two causes be scaled by α_1 and α_2 respectively. The principle of superposition then yields

$$f(\alpha_1 x_1 + \alpha_2 x_2) = f(ax_1) + f(\alpha_2 x_2) \tag{1.22a}$$

If homogeneity is also satisfied then

$$f(\alpha_1 x_1 + \alpha_2 x_2) = \alpha_1 f(x_1) + \alpha_2 f(x_2)$$
$$= \alpha_1 y_1 + \alpha_2 y_2 \tag{1.22b}$$

A functional relationship is said to be **linear** if it obeys both superposition and homogeneity. Any element (of a circuit or system in general) governed by such a functional relationship is *linear*. A circuit composed of such elements would also be linear.

1.6 IDEAL CIRCUIT ELEMENTS

The general representation of a circuit element is drawn in Fig. 1.10. It has voltage and current associated with it. The voltage is an *Across Variable* (AV) and the current is a *Through Variable* (TV). Any one of these variables could be regarded as an independent variable, and the other as dependent variable.

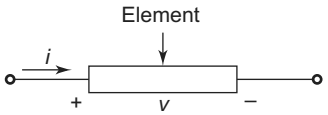


Fig. 1.10 *Circuit element*

A circuit element is *ideal*, when its voltage and current are related by

- constant of proportionality, or
- a differential or integral relationship.

These relationships can be shown to be linear which means that an ideal circuit element has linear behaviour.

1.6.1 Resistance

When a voltage is applied across a metallic conductor, (say, copper), the electric field created accelerates the *conduction* (*free*) electrons. These electrons collide with metal ions of the crystal lattice (of the metal) and lose a part of their energy as heat. Repeated accelerations and collisions cause two components of electron motion, the *drift* (average velocity) and the *random motion*. It is the drift of electrons that constitutes the electric current in the conductor (the conventional current flows in the opposite direction) which is associated with energy loss in the form of heat.

Therefore, the resistance is a *dissipative element*, which converts electric energy into heat, when the current flows through it in any direction. This process of energy conversion is irreversible.

Figure 1.11 shows the schematic representation of resistance. The element has *two terminals* (also called *nodes*). It conducts current from any one node to the other and in the process, voltage drop occurs across the element in the direction of current flow (the terminal at which the current enters acquires positive polarity with respect to the terminal at which the current exits).

Fig. 1.11 *Schematic representation of resistance*

Ohm's Law

It states that the voltage across the two terminals of a conducting material is proportional to the current flowing through it as

$$v = Ri \tag{1.23}$$

The constant of proportionality R is the resistance, represented in Fig. 1.11. The unit of resistance is *ohm* (V/A = R), abbreviated as capital omega, Ω.

By virtue of the polarities indicated on the resistance of Fig. 1.11, the charge loses energy in passing through the resistance which appears in the form of heat. A practical element that possesses the property of resistance is called a *resistor*.

Power dissipated by the resistance (Fig. 1.11) is

$$p = vi = i^2R = \frac{v^2}{R} W \tag{1.24}$$

Equation (1.23) can also be written as

$$i = Gv \tag{1.25}$$

where $G = 1/R$ = *conductance* in units of mhos (℧) or in units of Siemens (S). We shall use the symbol ℧.

Power dissipated can then be expressed in the alternative form

$$p = \frac{i^2}{G} G\, v^2 \tag{1.26}$$

The resistance of a resistor is *temperature dependent* and rises[1] with temperature. Temperature rise must be limited to a specified value by conducting away the heat generated. Every resistor has therefore a *specified wattage*. Manufacturing limitations impose a tolerance band. A resistor is therefore specified as, for example, 2 W, 20 Ω, (nominal) ± 10% at 25°C. It is only within specified limits that a resistor can be regarded as linear, outside which the behaviour becomes nonlinear.

[1] Resistance of carbon resistors decreases with temperature.

1.6.2 Conduction in Metals

As has been explained above, the conduction in metal is caused by the drift velocity (v_d) of charge carriers (electrons) under influence of electric field E.

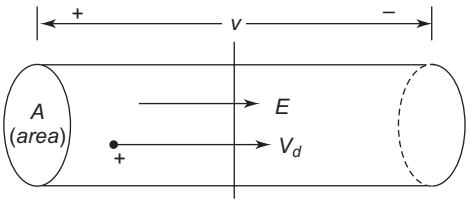


Fig. 1.12 *Long straight conductor with voltage V*

Though the charge carriers are electrons with charge $-q$ (1.6×10^{-19}C), we shall consider equivalently positive charge carriers, charge $+q$, as the conventional current is in the direction of flow of positive charges.

For simplicity, we consider a long straight conductor with voltage V applied across it as shown in Fig. 1.12. The charge carriers acquire a drift velocity

$$v_d = k_d E \text{ m/s} \tag{1.27}$$

where $E = \dfrac{V}{l}$, electric field in V/m

$k_d =$ drift constant

Let the concentration of charge carriers be n/m^3. Then the rate of charge flow across any cross section of the conductor in time dt is

$$dQ = q(nAv_d \mathrm{d}t)$$

The current flow is then given by

$$I = \frac{\mathrm{d}Q}{\mathrm{d}t} = qnAv_d = qnAk_dE \tag{1.28}$$

or
$$I = qn\, k_d A\, \frac{V}{l} \tag{1.29}$$

or
$$I = \frac{V}{R}\, A, \text{ Ohm's law} \tag{1.30}$$

where R = conductor resistance

$$R = \rho \frac{L}{A}\, \Omega, \rho = \frac{1}{qnk_d} \tag{1.31}$$

where ρ = *resistivity* if the conductor in Ωm

The inverse of resistivity is *conductivity* σ in units $(\Omega\text{-m})^{-1}$ or $\mho$/m

The *current density* is

$$J = \frac{I}{A} \text{ A/m}^2$$

whereas $I = \dfrac{V}{R} = \left(\dfrac{A}{\rho}\right)\dfrac{V}{l} = \left(\dfrac{A}{\rho}\right)E$

$$J = \frac{E}{\rho} = \sigma E \tag{1.32}$$

where ρ = resistivity

It is the basic form of Ohm's law.

1.6.3 Resistivity and Temperature

It has been qualitatively explained earlier that the resistivity of conductors increase with temperature. In not too large a range of temperature, linear law applies

$$\rho(T) = \rho_0[1 + \alpha(T - T_0)] \tag{1.33}$$

where

α = *temperature coefficient of resistivity at temperature* T_0

T_0 is usually taken as 0°C or 20°C.

The law of Eq. (1.33) will apply to the resistance of any particular conductor (replace ρ by R).

Example 1.3

The 18-gauge copper wire has a nominal diameter of 1.02 mm. It is carrying a constant current of 1.56 A. The density of free electrons is 8.5×10^{28} electrons/m^3. Find the value of current density and also the drift velocity.

Solution

$$A = \frac{\pi d^2}{4} = \frac{\pi(1.02 \times 10^{-3})^2}{4} = 8.17 \times 10^{-7}\ \text{m}^2$$

Current density

$$J = \frac{I}{A} = \frac{1.56}{8.17 \times 10^{-7}} = 1.906 \times 10^6\ \text{A/m}^2$$

From Eq. (1.28),

$$v_d = \frac{I}{A}\frac{1}{nq} = \frac{J}{nq}$$

Substituting values,

$$v_d = \frac{1.906 \times 10^6}{(8.5 \times 10^{28})(1.6 \times 10^{-19})} = 1.4 \times 10^{-4}\ \text{m/s}$$

Example 1.4

The 18-gauge copper wire of Example 1.3 have a diameter of 1.02 mm and so a cross-sectional area of $A = 8.17 \times 10^{-7}$ m^2. The wire is carrying a constant current of 1.56A.

Find (a) the magnitude of electrical field, (b) the potential difference between two points, if these are 50 m apart, and (c) the resistance of 50 m length of wire.

Given resistivity of copper = $1.72 \times 10^{-8}\ \Omega$m

Solution

(a) From Eq. (1.32),

$$E = \rho J = \rho \frac{I}{A}$$

or
$$E = \frac{1.72 \times 10^{-8} \times 1.56}{8.02 \times 10^{-7}} = 0.0327 \text{ V/m}$$

(b) The potential difference is

$$V = EL = 0.0327 \times 50 = 1.635 \text{ V}$$

(c) Resistance of 50 m length of wire

$$R = \frac{V}{I} = \frac{1.635}{1.56} = 1.05\ \Omega$$

or directly

$$R = \rho \frac{L}{A} = \frac{(1.72 \times 10^{-8}) \times 50}{8.20 \times 10^{-7}} = 1.05\ \Omega$$

Example 1.5

The resistance of the wire in the above two examples is found to be 1.05 Ω, at 20°C. Find its resistance at 0°C and at 100°C. Given: α(copper) = 0.00393(C°)$^{-1}$ at 20°C.

Solution

$$R = R_0[1 + \alpha(T - T_0)]$$

$\alpha = 0.00393\ (\text{C}°)^{-1}$ at 20°C

At $T = 0$°C,

$$R = 1.05\ [1 + 0.00393\ (20 - 0)] = 0.97\ \Omega$$

At $T = 100$°C,

$$R = 1.05\ [1 + 0.00393\ (100 - 20)] = 1.38\ \Omega$$

Observation

It is found from the above examples that increasing the temperature from 0°C to 100°C increases the wire resistance by a factor of

$$\frac{1.38}{0.97} = 1.34 \text{ or an increase of } 42\%$$

which is significant and so must always be accounted for copper.

It is convenient to use α (at 0°C). For copper conductor change of resistance with temperature is

$$\alpha(0°\text{C}) = \frac{1}{234.5} = 0.00426$$

We can find the copper-conductor resistance at another temperature if it is known at one temperature by the relationship.

$$\frac{R(T_2)}{R(T_1)} = \frac{234.5 + T_2}{234.5 + T_1} \tag{1.34}$$

1.6.4 Change of Resistance with Frequency

The ac and dc resistances of a copper conductor are related as R.

$$\frac{R_{ac}}{R_{dc}} = \rho(f) \ = \text{function of frequency} \tag{1.35}$$

When ac current is flowing through a conductor, the current is non-uniformly distributed over the cross section. This effect becomes more pronounced as frequency is increased. This phenomenon is called *skin effect*. It causes larger power loss for a given rms ac, than the loss when the same value of dc is flowing through the conductor. Consequently, the effective conductor resistance is more for ac than for dc.

Apart from skin effect, non-uniformity of current distribution is also caused by *proximity effect*. Thus, the ratio of R_{ac}/R_{dc} is a function of frequency. R_{ac}/R_{dc} versus frequency plot for copper is shown in Fig. 1.13.

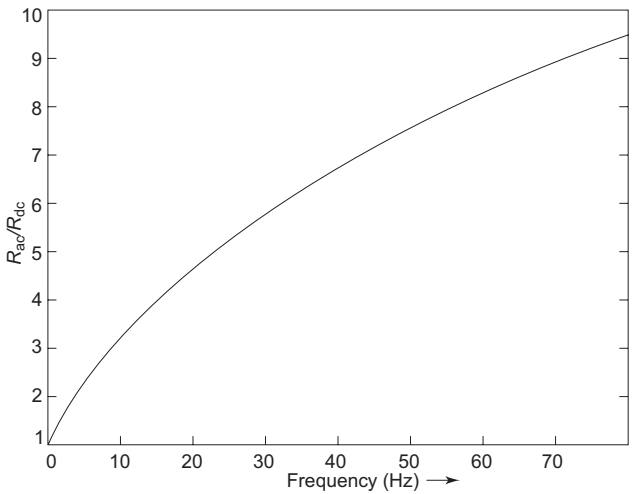


Fig. 1.13 *R_{ac}/R_{dc} versus frequency plot for copper*

1.6.5 Capacitance

It is a two-terminal element that has the capability of energy storage in an electric field. The stored energy can be fully retrieved. Figure 1.14 is the schematic representation of a capacitance. There is a voltage drop in the direction of current with the terminal where the current flows in acquiring positive polarity with respect to the terminal at which the current leaves the element. The law governing the *v-i* relationship of a capacitor is

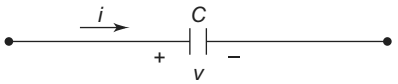


Fig. 1.14 *Schematic representation of a capacitance*

$$i = C\frac{dv}{dt}A \tag{1.36}$$

where C has the units of *farads*, F; the practical unit being a microfarad or μF.

Integrating Eq. (1.36),

$$v = \frac{1}{C}\int_0^t i\,dt + v_C(0) \text{ where } v_C(0) = \text{capacitance voltage at } t = c \tag{1.37}$$

For an initially uncharged capacitor, $v_C(0) = 0$, so that

$$C = \frac{q}{v}; \text{ as } q = \int_a^t i\,\mathrm{d}t \tag{1.38}$$

As per Eq. (1.37), *the voltage* (*or charge*) *of a capacitance cannot change instantly* as it would require infinite current.

Energy Stored in Capacitance

The power fed into capacitance is

$$p = vi = Cv\frac{\mathrm{d}v}{\mathrm{d}t} \tag{1.39}$$

Integrating Eq. (1.39) and assuming initially uncharged capacitance ($v = 0$ at $t = 0$), the stored energy is found to be

$$w_C = \int_0^t p\,\mathrm{d}t = C\int_0^t v\frac{\mathrm{d}v}{\mathrm{d}t}\mathrm{d}t$$

or
$$w_C = C\int_0^v v\,\mathrm{d}v = \frac{1}{2}Cv^2 \text{ J} \tag{1.40}$$

Observe that the energy stored in a capacitance is a function of its (instantaneous) voltage magnitude and is independent of the history of how this voltage is reached.

As the voltage is reduced to zero, all the energy stored in the capacitor is returned to the circuit in which the capacitor is connected.

A practical element possessing the property of capacitance is known as a *capacitor*. It is constructed of two parallel plates (in various forms) with an intervening dielectric.

The capacitance of a parallel-plate capacitor is given by

$$C = \varepsilon_0\varepsilon_r\left(\frac{A}{d}\right), \text{ with units of farads (F)} \tag{1.41}$$

where ε_0 = permittivity of free space = 8.85×10^{-12}
ε_r = relative permittivity of medium
A = area of each plate (m^2), and
d = distance between plates (m)

To get a capacitance of 1 F, let us calculate the value of (A/d) for $\varepsilon_r = 1$ (in air).

From Eq. (1.41),

$$\frac{A}{d} = \frac{1}{8.85\times10^{-12}} = 0.113\times10^{12}$$

If we assume $d = 1$ mm then

$$A = 0.113 \times 10^{12} \times 10^{-3}\text{m}^2$$
$$= 113 \text{ km}^2$$

It is obvious from this figure that it is not practical to construct a capacitor of IF value. It is still an impossibility even if we use $\varepsilon_r = 8$.

In view of the above, the practical value of a capacitor is in units of microfarad (μF) = 10^{-6} F. Capacitors with some μF value are made from two thin aluminium films wrapped round a dielectric material. Larger values are obtained with electrolyte dielectric medium. Capacitors needed for solid-state microchips are built from silicons or other semiconductors. These may be in ranges, of nanofarads nF = 10^{-9} F or even picofarads pF = 10^{-12} F.

As an example, consider a capacitor of 10 μF to which is applied 50 mA rectangular pulse of duration 0.4 ms as shown in Fig. 1.15(a). The capacitor is given by

$$q = \int_0^t i\,dt = 50\int_0^t dt = 50\,t \tag{i}$$

The charge increases linearly till at t = 0.4 ms,

$$Q = 50\text{ mA} \times 0.4\text{ ms} = 20\ \mu\text{C}$$

as shown in Fig. 1.15(b).

The capacitor voltage $v = \dfrac{q}{C}$ also rises linearly till at 0.4 ms,

$$v = \frac{20\ \mu\text{C}}{10\ \mu\text{F}} = 2\text{ V}$$

as shown in Fig. 1.15(c).

Energy stored in the capacitor is

$$w = \frac{1}{2}Cv^2$$

increase by square law to a value

$$w = \frac{1}{2} \times (10\ \mu\text{F}) \times (2)^2 = 20\ \mu\text{J}$$

as shown in Fig. 1.15(d).

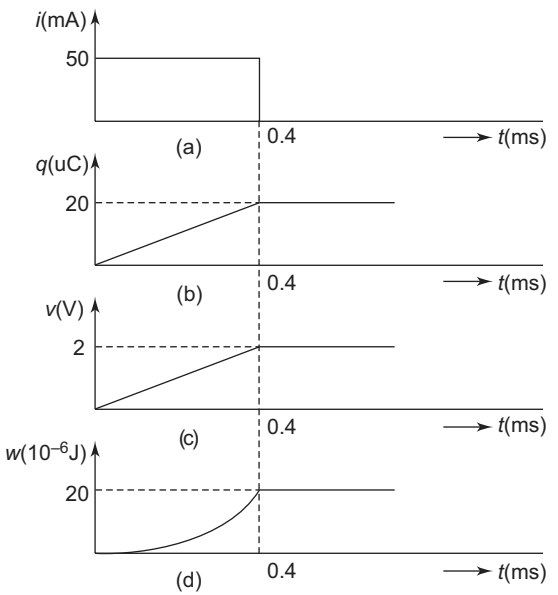


Fig. 1.15 *Waveforms of (a) current, (b) charge, (c) voltage, and (d) energy in a capacitor*

1.6.6 Inductance

It is a two-terminal storage element in which energy is stored in the magnetic field. The schematic representation of the inductance is shown in Fig. 1.16. The changing magnetic field set up by the time-varying current through the inductance reacts to induce voltage in it to oppose the change of current (see polarity shown in Fig. 1.16). The voltage as in the case of previous two elements is shown to drop in the direction of current. The *v-i* relation of an inductance is

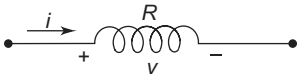


Fig. 1.16 *Schematic representation of inductance*

$$v = L\frac{\mathrm{d}i}{\mathrm{d}t} \tag{1.42}$$

where L = inductance in henries, H.

Integrating Eq. (1.42),

$$i = \frac{1}{L}\int_0^t v\,\mathrm{d}t + i(0) \tag{1.43}$$

where $i(0)$ = inductance current at $t = 0$.

According to Eq. (1.43), *current through an inductance cannot change instantly* (compare with capacitance voltage) as it would require infinite voltage.

Energy Stored in Inductance

The power fed to inductance is

$$p = vi = Li\frac{\mathrm{d}i}{\mathrm{d}t}$$

Assuming $i\,(t = 0) = 0$, the stored energy is found by integrating power (p) as

$$w_L = \int_0^t p\,\mathrm{d}t = \int_0^t L\frac{\mathrm{d}i}{\mathrm{d}t}\mathrm{d}t$$

or
$$w_L = L\int_0^t i\,\mathrm{d}i = \frac{1}{2}Li^2 \text{ J} \tag{1.44}$$

The energy stored in the inductance depends upon the instantaneous current and is independent of the history of the current. As the current reduces to zero, the energy stored in the inductance is returned to the circuit in which it is connected.

❑ **An Observation** Let us juxtapose the differential-integral equations governing the elemental behaviour of a capacitance and inductance.

Capacitance $\quad i = C\dfrac{\mathrm{d}v}{\mathrm{d}t};\; v = \dfrac{1}{C}\int i\,\mathrm{d}t$

Inductance $\quad v = L\dfrac{\mathrm{d}i}{\mathrm{d}t};\; i = \dfrac{1}{L}\int v\,\mathrm{d}t$

It is seen from these relationships that one set can be obtained from the other by replacing

$v \leftrightarrow i$

$L \leftrightarrow C$

This interchangeability is known as the concept of *duality*. Let us now examine a resistance element for which

$v = Ri$

$i = Gv$

Duality is extended to resistance by interchanging. ($R \leftrightarrow G$) R and G

A practical inductance is called an *inductor*. It is a coil wound on a magnetic core (may be air core for small values of inductance). A magnetic core inductor has constant inductance only in a limited range of current (at high current, the core saturates and inductance reduces. See Chapter 7).

This means that it is linear in a limited range of currents. In electronic circuits, the use of an inductor is avoided except in high-power circuits. In fact, inductance cannot be fabricated as such in semiconductor integrated circuits. Consider that an inductance of 1 H is excited with current waveform sketched in Fig 1.17.

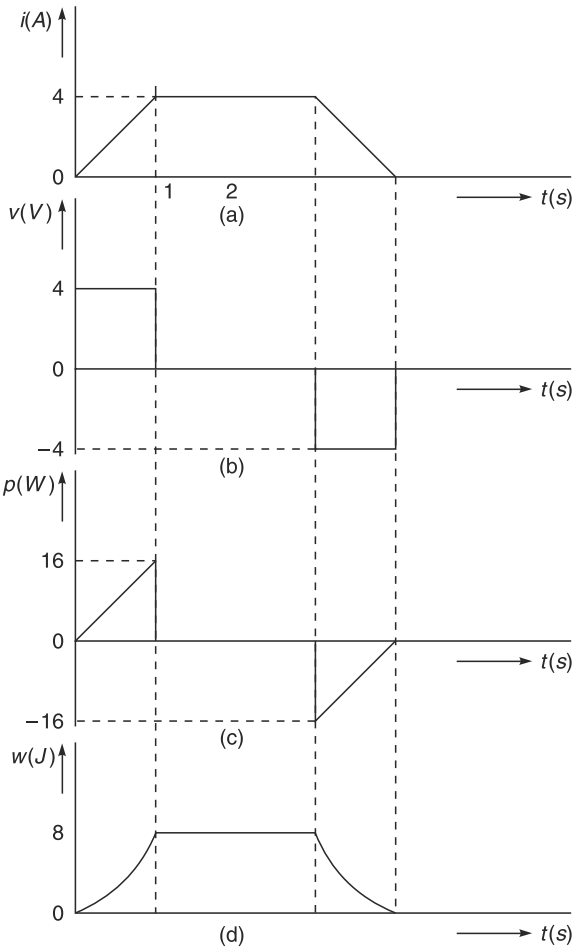


Fig. 1.17 *Waveforms of (a) current, (b) voltage, (c) power, and (d) energy in an inductance*

- During voltage waveform up to 1s, the $i(t)$ rises from 0 to 4 A at rate 4 A/s. So the voltage $v = L\frac{di}{dt} = 1.4 = 4$ V, which is constant. From 1 s to 3 s, the rate of change of current is zero and so is the voltage. From 3 s to 4 s, the current reduces to zero at rate of 4 A/s. So the voltage is constant at –4 V. The voltage waveform is sketched in Fig. 1.17(b).
- Power waveform is the product vi and is sketched in Fig. 1.17(c). The maximum power is $4 \times 4 = 16$ W.
- Stored energy waveform is $w_L = \frac{1}{2}Li^2 = \frac{1}{2}i^2$. It rises by square law up to $1/2 \times 4^2 = 8$ J at 1 s, remains constant from 1 s to 3 s as i is constant. It then decays to zero from 3 s to 4 s (square law) as shown in Fig. 1.17(d).

1.6.7 Independent Source

While the two storage elements (capacitance and inductance) studied earlier can absorb energy and deliver back the same, an independent source can deliver or absorb energy continuously (without any limit). Such elements are called *active* elements.

An independent voltage source is shown in Fig. 1.18(a) and (b) along with its polarity markings. The source voltage is assumed to be completely independent of the current (ideal source). If current flows out of the positive terminal, the source is delivering energy (and power) to the circuit in which it is connected. On the other hand, if current flows into the positive terminal of the source it absorbs power. There is no limit to the power that an ideal source can deliver or absorb.

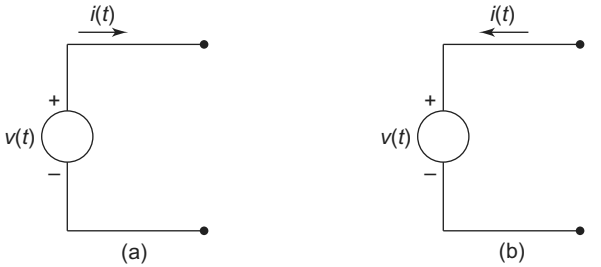


Fig. 1.18 *Independent voltage source (two-terminal device): (a) Delivering power (b) Absorbing power*

In a practical voltage source, energy is obtained or absorbed by a conversion process from another energy form. For example, in a battery source, chemical energy is converted to electrical form when the source is delivering, and vice-versa when the source is absorbing. In a practical source, the terminal voltage is current dependent, though in the useful current range this dependency is limited. Further, a practical source can handle only a certain maximum power called *rated power*.

Similarly, an ideal *independent current source* can supply (or receive) a specified current independent of its voltage. Such a source is represented in Fig. 1.18(c). Its terminal voltage is determined by the conditions in the circuit to which it is connected. Such sources occur in electronic circuits. In a practical current source, current is voltage dependent but is practically independent of it in the useful range.

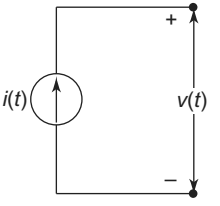


Fig 1.18(c) *Independent current source*

Supplying/Absorbing Power

It is not only sources that can supply or absorb power, any element can in fact supply or absorb power. In Fig. 1.19(a) below, the element is supplying power and in Fig. 1.19(b), it is absorbing power.

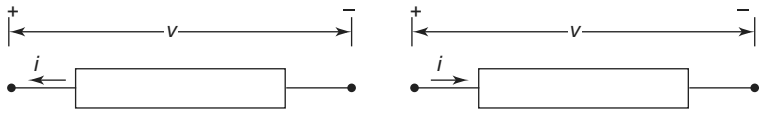


Fig. 1.19 *(a) Element supplying power (b) Element absorbing power*

Capacitor and inductor can absorb or supply power, and thereby store or give away stored energy to the circuit to which their terminals are connected.

If the element is a resistor, it absorbs power only for positive value of resistance. However, an active electronic circuit can exhibit negative resistance and so supply power.

1.6.8 Dependent Sources (Ideal)

The voltage/current of a *dependent voltage/current source* is determined by voltage/current at another point in the circuit. The law of dependence is linear, say, a constant of proportionality. Figure 1.20 shows the representation of such dependent source[2]. Such sources are encountered in modelling of electronic devices.

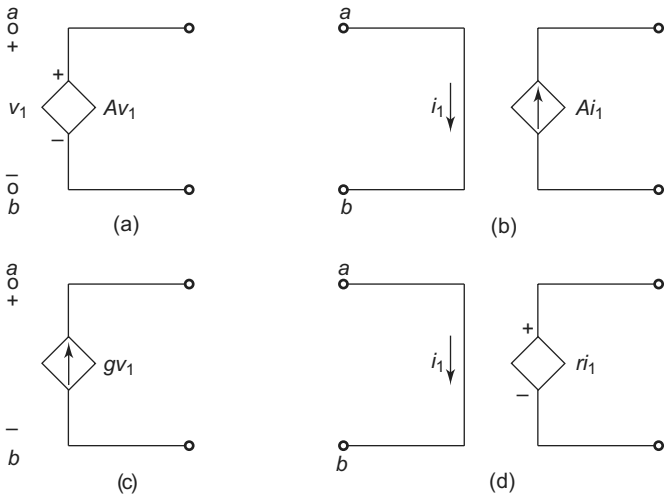


Fig. 1.20 *(a) Voltage-dependent voltage source (b) Current-dependent current source (c) Voltage-dependent current source (d) Current-dependent voltage source*

The ideal circuit elements we have studied are of two kinds:

❑ **Passive Elements (*R*, *L*, *C*)** Resistance is the dissipative element. Capacitance and Inductance can store and deliver energy without any loss of energy in the process, but their energy-handling capacity is limited. Practical passive elements would possess all the three properties (resistance, capacitance and inductance) but depending upon their design, one of these properties will predominate. A practical element can be modelled using ideal *R*, *L* and *C*.

[2] The concept of dependent sources is useful in modelling transistors and other active devices in electronics.

❑ **Active Element (Sources)** Ideal sources (independent, dependent) can handle infinite power and energy. But practical sources can handle finite (rated) power but infinite energy.

❑ **Certain Properties of Ideal Circuit Elements (*R, L, C*)** These elements are,

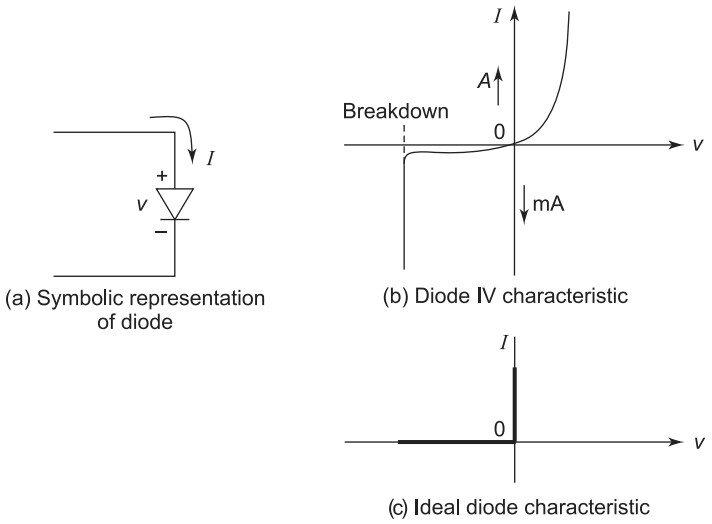
- Linear (already explained)
- Bilateral
- Time invariant
- Lumped

❑ **Bilateral and Unilateral** *R, L, C* ideal elements' behaviour is independent either of the terminal (node) at which current is fed in or of the direction of voltage applied at the terminals. If the terminal connections of an element in a circuit are reversed, it would not make any difference to the circuit response. This is the *bilateral* property of *R*, *L*, *C* elements.

If an element or circuit does not possess the above property, it is said to be *unilateral*. For example, for the dependent voltage source of Fig. 1.20(a), the input voltage controls the output voltage. However, a voltage applied at the output terminal would not control the voltage at the input terminals. This is the behaviour of an active device represented by this source which is inherently unilateral.

❑ **Nonlinear** Linear behaviour of an element in an approximation (idealisation) of a general nonlinear behaviour in a limited range of variables (voltage/current). Consider, for example, an electric lamp. As it is switched on, the element heats up and its resistance increases. It stabilises at a particular temperature at which the element glows and gives off light (and some heat). This kind of behaviour is not only nonlinear but also *time-varying*.

Consider another element, a solid-state diode shown schematically in Fig. 1.21(a).



(a) Symbolic representation of diode

(b) Diode IV characteristic

(c) Ideal diode characteristic

Fig. 1.21 *The IV characteristic of an Si-diode*

It is plotted in Fig. 1.21(a) and is highly nonlinear with directional behaviour. When *V* is positive, only a small value of this voltage can cause the diode to conduct large current, whose value is determined by the circuit in which the diode is connected. For negative values of *V*, the diode conducts negligible current and the diode breaks down above a certain (large) negative voltage.

We see from the above account that a diode is a *nonlinear unilateral* element.

Distribution Effects

In the ideal model for R, L and C, assume that there are no distribution effects. So in that sense, these are *lumped elements*. A word about distribution: consider a transmission line (say electric). It has resistance, inductance and capacitance all along the line, spread out in length. Except for a short line, we cannot lump these elements. But in the circuit we shall deal with, the element's physical dimensions are small enough compared to voltage/current wave length so that lumping is valid.

Statement

The R, L, C ideal elements that we shall deal with are *linear*, *bilateral lumped* and *time-invariant*. This statement will not be repeated in the text but it applies to all the circuits we shall deal with as well as electric machines.

Example 1.6

A voltage of $200\sqrt{2}$ sin $(314t)$ V is applied across a 10 uF capacitor shown in Fig. 1.22.

(a) Determine the capacitance current i as a function of time.

(b) Sketch voltage and current waveforms. What conclusions do you draw?

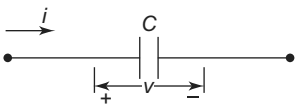


Fig. 1.22

(c) Sketch instantaneous power as a function of time. What do you observe? Also calculate the value of average power.

Solution

(a) $$i = C\frac{dv}{dt} = 10\times10^{-6}\frac{d}{dt}[200\sqrt{2}\sin 324t]$$

$$= 10\times10^{-6}\times200\sqrt{2}\times314\cos314t$$

$$= 0.888\cos 314t$$

(b) Voltage and current waveforms are plotted in Fig. 1.23. It is observed that the positive peaks of the current occurs 90° earlier than the positive peaks of the voltage. It means the current *leads* the voltage by 90°.

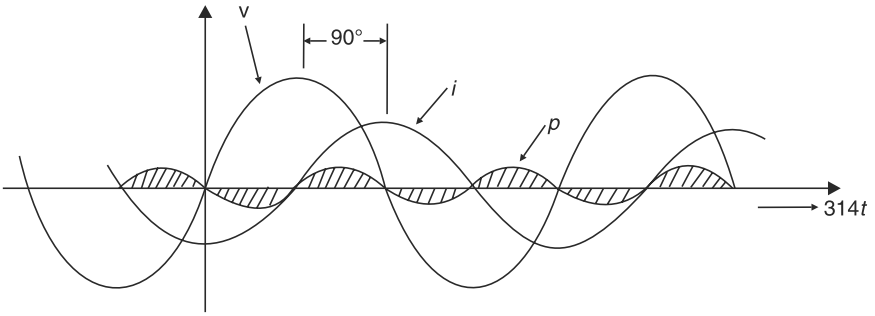


Fig. 1.23

(c) Instantaneous power

$$p = vi = 200\sqrt{2}\times0.888\sin(314t)\cos(314t)$$

Using trigonometric identity, $2\sin\theta\cos\theta = \sin 2\theta$, we can write

$$p = 125.56\sin(628t)\ \text{W}$$

We find that the instantaneous power oscillates at twice the frequency (i.e. 628 rad/s) of the voltage/current frequency. The average power is zero.

Example 1.7

A voltage of 25 cos 500*t* V is applied to 25 mH inductor. The inductor current is zero at $t = 0$. Find the power being absorbed by the inductor and the energy stored in it at $t = 5$ ms. Find the first time ($t > 0$) at which the power absorbed is zero and the time when energy stored is zero.

Solution

$$i(t) = \frac{1}{L}\int v(t)\,dt; i(0) = 0$$

$$= \frac{1}{L}\int 25\cos 500t\,dt$$

$$= \frac{10^3}{25} \times 25 \times \frac{1}{500}\sin 500t$$

or $i(t) = 2\sin 500t$

At $t_1 = 5$ ms, $500t_1 = 500 \times 5 \times 10^{-3} = 2.5$ rad or 143.2°

$\cos 143.2° = -0.8$, $\sin 143.2 = 0.6$

$v(t_1) = 25 \times (-0.8) = -20$ V

$i(t_1) = 2 \times 0.6 = 1.2$ A

Power being absorbed

$p(t_1) = -20 \times 1.2 = -24$ W

Example 1.8

A capacitor is fabricated from two thin aluminium discs with 1 cm diameter separated by 150 μm, with air in between. Calculate its capacitance. What voltage should be applied across this capacitor to store 1 mJ of energy? What should be the relative dielectric constant of the material to be placed in between the disc so as to store 2 μJ of energy at 100 V?

Solution The capacitance of the parallel-plate capacitor is

$$C = \varepsilon_r \varepsilon_0 \left(\frac{A}{d}\right) F \qquad \text{(i)}$$

$\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, $\varepsilon_r = 1$ for air

Area: $A = \pi \times \left(\frac{1 \times 10^{-2}}{2}\right) = \left(\frac{\pi}{4}\right) \times 10^{-4}\, m^2$

Diameter: $d = 150 \times 10^{-6}$m

For these values in Eq (i), we get

$$C = \left[88.5 \times 10^{-12} \times \frac{(\pi/4) \times 10^{-4}}{150 \times 10^{-6}}\right]$$

$$= 4.6 \text{ pF}$$

Energy stored

$$w_C = \frac{1}{2}Cv^2$$

$$1 \times 10^{-3} = \frac{1}{2} \times 4.6 \times 10^{-12} v^2$$

or $v = 6.59$ kV

To store 2 μJ at 100 V, we have to find ε_r.
From Eq. (i), capacitance would now be

$$C = \varepsilon_r \times 4.6\,\text{pF} \qquad \text{(ii)}$$

Substituting values in Eq. (ii),

$$2 \times 10^{-6} = \frac{1}{2}\varepsilon_r \times 4.6 \times 10^{-12} \times (100)^2$$

or $\varepsilon_r = 87$

Example 1.9

(a) Is the power being absorbed or generated by the circuit element of Fig. 1.24(a) and what is the value of this power?

(b) Is the power being absorbed or generated in the circuit element of Fig. 1.24(b) and what is the value of the power?

(c) Find the power being absorbed or supplied by the circuit element of Fig. 1.24(c) at t = 10 ms.

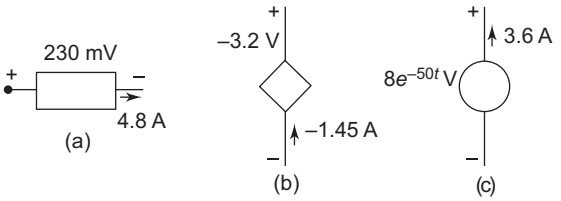


Fig. 1.24

Solution

(a) The current is flowing into the positive terminal. So power is being absorbed is

$$p(\text{absorbed}) = 230 \times 10^{-3} \times 4.8 = 11.04 \text{ W}$$

(b) The current is flowing out of the positive terminal. So power generated is

$$p(\text{generated}) = -3.2 \times (-1.45) = +4.64 \text{ W}$$

(c) The current is flowing out of positive terminal. So

$$p \text{ (supplied)} = 8e^{-50t} \times 3.6 = 28.8\, e^{-50t} \text{ W}$$

At t = 10 ms,

$$p \text{ (supplied)} = 28.8\, e^{-0.5} = 17.45 \text{ W}$$

Example 1.10

A cubic water tank has a surface area of 6.3 m^2 and is filled to 95 percent capacity thrice daily. The water is heated from 20°C to 50°C. The losses per square metre of tank surface per 1°C temperature difference are 6 W. Find the following:

(a) Loading in kW (b) Efficiency of the tank

Assume specific heat of waters = 4.186 kJ/kg°C and 1 kWh = 3600 kJ

Solution Given data

Surface area of the tank = 6.3 m^2 % capacity to which the tank is filled with water = 95%

Rise in temperature of water, $t_2 - t_1 = 50°C - 20°C = 30°C$

Loss per square metre of tank surface per 1°C temperature difference = 6 W

(a) Loading in kW

Let ℓ = side of the tank

Then the total surface area of the tank = 6 ℓ^2

$\therefore \quad 6\ \ell^2 = 6.3$ or $\ell = 1.0247$ m

Volume of tank $\ell_3 = 1.076\ m^3$

Volume of water to be heated daily = $3 \times 1.076 \times 0.95 = 3.0676\ m^3$

$\therefore$ mass of water to be heated daily = $3.0676 \times 1000 = 3067$ kg

(Note: Mass density of water = 1000 kg/m^3)

Heat required to raise the temperature of water = $m \times c \times (t_2 - t_1)$

$= 3067 \times 4.186 \times 30$

= 385154 kJ

= 385154/3600 kWh

= 106.99 kWh

Daily loss from tank surface = $6 \times 6.3 \times (50 - 20) \times 24/1000 = 27.21$ kWh

Energy supplied per day = $106.99 \times 27.21 = 134.20$ kWh

Loading in kW = 134.20/24 = 5.6 kW

(b) Efficiency of the tank, η_{tank}

η_{tank} = Output/Input = 106.99/134.25 = 0.7969 = 0.8 or 80%

Example 1.11

A resistance oven using nichrome wire is to be operated from a 220 V supply and is to be rated at 20 kW. If the temperature of the element is to be limited to 1200°C and average temperature of the charge is 500°C. Find the diameter and length of the element wire?

Radiating efficiency = 0.59, Emissivity = 0.9, Specific resistance of nichrome = 109×10^{-8} Ωm

Solution Given data:

Applied voltage $V = 220$ V

Rated power $P = 20$ kW

T_1 = element limited temperature in Kelvin = 273 + 1200 = 1473 K

T_2 = average temperature of the charge in Kelvin = 273 + 500= 773 K

η_{rad} = radiating efficiency = 0.59

e = emissivity = 0.9

ρ = specific resistance of nichrome = 109×10^{-8} Ωm

As we know that, $\ell/d^2 = \pi V^2/4\rho P = TT \times (220)2/4 \times 109 \times 10^{-8} \times (20 \times 10^3)$

$= 1743728$ (i)

Now, $H = 5.67 \times \eta_{rad} \times e \times [(T_1/100)^4 - (T_2/100)^4]$ W/m^2

$= 5.67 \times 0.59 \times 0.9 \times [(1473/100)^4 - (773/100)^4]$ W/m^2

= 130989 W/m^2

Now, total heat dissipated/second = electrical power input

$\therefore \quad (\pi d) \times \ell \times 130989 = 20000$

$d\ell = 20000/130989 \times \pi$

$\therefore$ $d\ell = 0.04860$ or $d^2\ell^2 = 0.002362$ (ii)

Now, multiplying (i) and (ii), we have

$d^2\ell^2 \times \ell/d^2 = 1743728 \times 0.002362$

$\ell^3 = 4118.79$

$\ell = 16.03$ m

And, $d = 0.04860/16.03$

$d = 3.03189 \times 10^{-3}$ m

$d = 3.0319$ mm

Example 1.12

A 30 kW, 3-phase, 400 V resistance oven is to be used by nickel-chrome strip 0.35 mm thick for the three-star connected heating elements. If the temperature of the strip is to be 1100°C and that of the charge be 500°C estimate a suitable width for the strip.

Assume, emissivity = 0.9 and radiating efficiency to be 0.5 and resistivity of the strip material is 101.6×10^{-8} Ωm.

Solution Given data:

Power per phase $P_{ph} = 30/3 = 10$ kW

Voltage per phase $V_{ph} = 400/\sqrt{3} = 231$ V

Thickness of strips 0.35 mm $= 0.35 \times 10^{-3}$ m

$T_1 = 273 + 1100 = 1373$ K

$T_2 = 273 + 500 = 773$ K

Emissivity (e) =0.9

Radiating efficiency (η_{rad}) = 0.5

Resistivity of the material (ρ) $= 101.6 \times 10^{-8}$ Ωm

Let width of the strip be w.

If R is the resistance of the strip; then

$R = Vph^2/P = (231)^2/10 \times 10^3 = 5.34\ \Omega$

Resistance of the strip

$R = 5.34 = \rho\ \ell/a = \rho\ \ell\ /wt$

$\ell/w = 5.34 \times (0.35 \times 10^{-3})/101.6 \times 10^{-8} = 1839.6$ (i)

or, heat dissipated from surface of the strip,

$H = 5.67 \times \eta_{rad} \times e[(T_1/100)^4 - (T_2/100)^4]$

$= 5.67 \times 0.5 \times 0.9 \times [(1373/100)^4 - (773/100)^4]$ W/m^2

$= 81563$ W/m^2

Surface area of the strip = $2\ w\ell$

$\therefore$ total heat dissipated = $2\ w\ell \times 81563$

$\therefore$ $2\ w\ell \times 81563 = 10 \times 10^3$

or, $w\ell = 10 \times 10^3/81563 \times 2 = 0.0613$ (ii)

Inserting the value of ℓ (= 1839.6 w) from Eq. (i) in (ii), we get

$w \times 1839.6w = 0.0613$

$$w^2 = 3.33225 \times 10^{-5}$$
$$w = 5.773 \times 10^{-3} \text{ m or } 5.773 \text{ mm}$$

1.7 SI UNITS—INTERNATIONAL STANDARD OF UNITS

Table 1.1 *SI Units*

Quantity	*Symbol*	*Unit*	*Symbol*
SI Base Units			
Length	-	metre	m
Mass	-	kilogram	kg
Time	-	seconds	s
Temperature	-	Kelvin (°C + 273)	K
Current	*i, I*	ampere	A
Derived Units			
Charge	*q*	Coulomb	C
Energy	*w*	Joule	J
Power	*p, P*	Watt	W
Voltage	*v, V*	Volt	V
Circuit Elements			
Resistance	*R*	Ohm	Ω
Conductance	$G = 1/R$	Siemen, Mho	S, ℧
Capacitance	*C*	Farad	F
Inductance	*L*	Henry	H

The SI system uses the decimal system to relate smaller and larger unit values to the basic unit, powers of 10 are prefixed to the basic unit. A list of prefixes, their symbols and names are given in Table 1.2.

Table 1.2 *SI Prefixes*

Factor	*Name*	*Symbol*	*Factor*	*Name*	*Symbol*
10^{-12}	Pico	p		—	—
10^{-9}	Nano	n	10^{9}	Giga	G
10^{-6}	Micro	μ	10^{6}	Mega	M
10^{-3}	Milli	m	10^{3}	Kilo	k
10^{-2}	Centi	c	10^{2}	Hector	h
10^{-1}	Deci	d	10^{1}	Deka	da

For terms of distance, it is much more common to use 'micron (μm)' than micro(μ); also the unit of angstrom (Å) is used for 10^{-10} m.

The student is well advised to memorise these prefixes as these are used in this book and all other technical work.

Engineering Units

A quantity is represented by a number 1 to 999 and appropriate metric unit using a power divisible by 3.
Example: 1.2×10^{-5} s is expressed as 12 μs
13,560,000 Hz as 13.56 MHz
49,000 Ω as 49 kΩ

Summary

- The direction in which positive charges move shows the direction of positive current. Alternatively, positive current flow is in the direction opposite to that in which electrons are moving.
- Any element or source is said to supply power if positive current flows out of the positive terminal. Any element or source absorbs (receives) power if the positive current flows into its positive terminal.
- There are six sources: the independent voltage source, independent current source and four possible dependent sources.
- Ohm's law states that the voltage across a resistor is directly proportional to the current flowing through it, i.e. $v = iR$.
- Power dissipated in a resistance is given by $p = vi = i^2R = v^2/R = Gv^2$ watts.
- Capacitor v-i relationship $i = Cdv/dt$; integral form can also be used; initial voltage to be accounted for. Stored energy, $w_C = (1/2)Cv^2$ joules.
- Inductance v-i relationship $v = L(di/dl)$; integral form can also be used; initial current to be accounted for stored energy; $w_L = (1/2)Li^2$ joules.
- Sinusoidal waveform (voltage or current) $v = V_m \cos(2\pi/T)t$.
  V_m = maximum or peak value
  T = time period (usually in seconds)

  or
  $v = V_m \cos 2\pi ft$
  $f = 1/T$ frequency in Hertz [Hz], i.e. cycles/s

  or
  $v = V_m \cos \omega t$
  $\omega = 2\pi f$; frequency in rad/s
- For comparing the phases of two sinusoidal waveforms, it is convenient to express both in cosine or both in sine form with positive sign. Of course, both must have same frequency.

Exercises

Review Questions

1. Derive the expression for potential difference between two point charges (q coulombs) of opposite sign displaced by distance d apart.

2. Sketch the current and voltage waveforms if
   $i = I \sin(\omega t - 60°)$
   $v = V \cos(\omega t + 30°)$
   What is the phase difference between the two and which one leads the other?
3. A capacitor of C farads is charged with q coulombs. What is the stored energy?
4. State the principles of superposition and homogeneity.
5. Show that an inductor is a linear circuit element.
6. In an inductor L henries, charge is flowing at the rate of q coulombs/second. What is its stored energy?
7. State the conditions for a source or element to supply or absorb power.
8. A capacitor of C farads at an instant has voltage V which is reducing at the rate dv/dt. Is it supplying or absorbing power and how much?
9. State Ohm's law.

Problems

1 Consider a 230 V, 100 W incandescent lamp. Determine:
   (a) the lamp resistance,
   (b) the lamp current, and
   (c) the energy consumed by the lamp in 8 hours.

2. Figure 1.25(a) shows a black box that contains a single ideal circuit element. Three voltage-current relationships for this black box are shown in Fig. 1.25(b), (c) and (d).
   (a) Identify the circuit element in each case and its value in appropriate units.
   (b) Find the peak energy storage/power dissipation,
   (c) In the resistive case find also the total energy consumed.

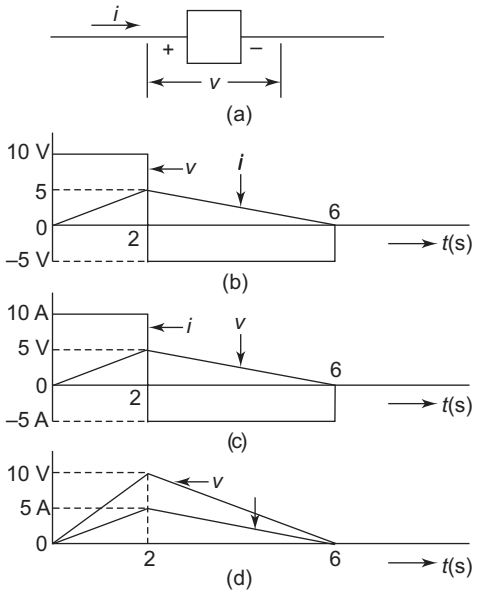


Fig. 1.25

3. A voltage of $200\sqrt{2}$ sin 314 t is applied across a capacitor of 100 uF.
   (a) Determine the capacitor current as a function of time.
   (b) Sketch voltage and current waveforms. What conclusion do you draw?
   (c) Sketch instantaneous power (vi) as a function of time. What do you observe?
4. Repeat Problem 3 for an inductance of 500 mH.
5. Repeat Problem 3 for a resistance of 1 kΩ.
6. Current $i = I_0 e^{-t}$ passes through a resistance R from $t = 0$ onward. What is the total energy dissipated in the resistance up to $t = \times$?

True or False?

1. An induction motor cannot run at synchronous speed.
2. A synchronous motor always has cylindrical rotor.
3. A synchronous motor is fed from ac but also requires small dc power input.

Fill in the Blanks

1. The kinds of synchronous machines are …….
2. The core of a transforms is made of …….
3. The kinds of induction machines are ……. and …….

Multiple-Choice Questions

1. Stored energy of an inductance is dependent upon its
   (a) instantaneous voltage only
   (b) instantaneous current only
   (c) instantaneous voltage and history of its current
   (d) instantaneous current and history of its voltage
2. At a particular instant, an inductance of 1 H carries a current of 2 A, while the voltage across is 1 V. The energy stored in the inductance in joules is
   (a) 1/2 (b) 1 (c) 3/2 (d) 2

Answers

True or False

1. True 2. False 3. True

Fill in the Blanks

1. cylindrical and salient pole
2. cargo steel
3. squirrel cage and wound rotor induction motor

Multiple-Choice Questions

1. (a) 2. (d)

Fundamental Laws of Electric Circuits, Resistive Circuits

chapter 2

Goals & Objectives

- All the methods of circuit analysis and theorems through resistive network
- Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL)
- Reduction of passive resistive network by series, parallel combinations and star/delta conversion
- Practical source conversion—voltage-to-current source and vice versa
- Nodal method of circuit analysis
- Mesh method of circuit analysis
- Ability to choose between nodal and mesh methods
- Network theorems, their basis and applications
- Thevenin and Norton equivalents

2.1 INTRODUCTION

An electric circuit is an interconnection of circuit elements, resistors, inductors, capacitors, and voltage and current sources. We shall present here the famous laws of circuit theory and methods of circuit analysis based on these.

2.2 FUNDAMENTAL LAWS OF ELECTRIC CIRCUITS

An electric circuit is composed of interconnection of several elements and sources. Before enunciating the two general laws governing the circuit behaviour, it is necessary to understand certain terms identifying the interconnections.

❑ **Node** It is a circuit point where ends (terminals) of two or more circuit elements meet.

❑ **Path** It is a traversal through elements from one node to another.

❑ **Branch** It is a path between two adjoining nodes.

❑ **Loop** It is a closed path starting and ending at the same node without going through the same node more than once.

❑ **Mesh** It is a loop that does not contain any other loop within it.

❑ **Junction** It is a node where three or more circuit elements (or branches) meet.

Remark

At a node where only two-circuit element need not be considered (as this node can always be eliminated by combination of elements or if one of these is a voltage source), the voltage at the node is known; it is not an unknown to be determined.

Therefore, in circuit analysis we are concerned with junction but we shall loosely use the term 'node' for a junction.

Consider an electric-transmission line. It has resistance, inductance and capacitance all along the line, spread out in length. Except for a short line, we cannot lump these elements. However, in the circuit we shall deal with, the element's physical dimensions are small enough compared to voltage/current wavelength so that *lumping* is valid.

Statement

The *R, L, C* ideal elements that we shall deal with are *linear*, *bilateral-lumped* and *time-invariant*. This statement will not be repeated in the text but it applies to all the circuits we shall deal with as well as electric machines.

Apart from Ohm's law, already stated for a resistive element, we shall now enunciate two fundamental circuit laws (Kirchhoff's laws) which follow rationally from the nature of electrical quantities.

2.2.1 Kirchhoff's Current Law (KCL)

Algebraic sum of currents going away from or *coming towards a node is zero*. If the current going away from the node is taken as positive, current coming towards the node is negative or vice versa.

This law is a simple and obvious consequence of the fact that no charge can accumulate at a node. Consider the node in Fig. 2.1. It immediately follows that

$$i_1 - i_2 + i_3 - i_4 + i_5 = 0$$

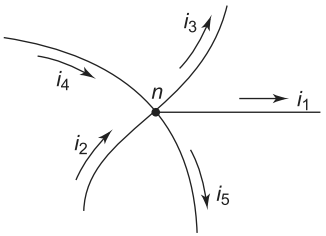


Fig. 2.1 *Node illustrating KCL*

Example 2.1

Consider the two-node circuit of Fig. 2.2. Note that zero-node is the *reference node*. Write the KCL equations for the two nodes.

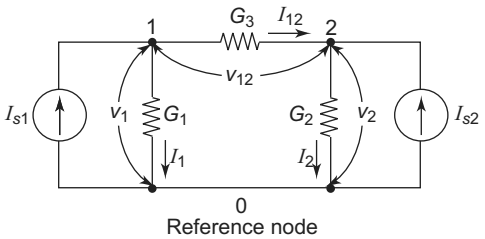


Fig. 2.2

Solution G_1, G_2, G_3 are the conductances of the three branches. There are two nodal voltage v_1, v_2.

At Node 1,

$$I_{s1} - I_1 - I_{12} = 0$$

or $$I_{s1} - G_1 v_1 - G_3 v_{12} = 0$$

or $$G_1 v_1 + G_3 v_{12} = I_{s1} \quad \text{(i)}$$

At Node 2,

$$I_{s2} - I_2 + I_{12} = 0$$

or $$I_{s2} - G_2 v_2 + G_3 v_{12} = 0$$

or $$G_2 v_2 - G_3 v_{12} = I_{s1} \quad \text{(ii)}$$

Going round the inner loop, it is seen that

$$v_{12} = v_1 - v_2 \quad \text{(iii)}$$

Substituting the value of v_{12} in Eq. (i) and (ii), we get

$$G_1 v_1 + G_3 (v_1 - v_2) = I_{s1}$$

$$G_2 v_2 - G_3 (v_1 - v_2) = I_{s2}$$

Rearranging, we have

$$(G_1 + G_3) v_1 - G_3 v_2 = I_{s1} \quad \text{(iv)}$$

$$-G_3 v_1 + (G_2 + G_3) v_2 = I_{s2} \quad \text{(v)}$$

These are the two simultaneous algebraic equations to determine v_1 and v_2.

Remark

1. In writing KCL equation, there is always a reference node w.r.t. which all other node voltages are defined.
2. KCL equation numbers are the same as the number of nodes other than the reference node.
3. KCL equation solutions gives the unknown node voltages.
4. Currents in resistances can be obtained from nodal voltage by Ohm's law.
5. The reader should observe and discover that KCL equations have a symmetry.

2.2.2 Kirchhoff's Voltage Law (KVL)

The algebraic sum of voltage drops (*or rises*) *round a loop* (*closed path*) *or mesh in a specified direction is zero*. If voltage drop is taken as positive, voltage rise is negative or vice versa.

This law is a consequence of the fact that in a loop transversal, we return to the starting node.

Example 2.2

Consider the two-mesh network of Fig. 2.3. Express the currents in the three resistances in terms of mesh currents and then write the KVL equation.

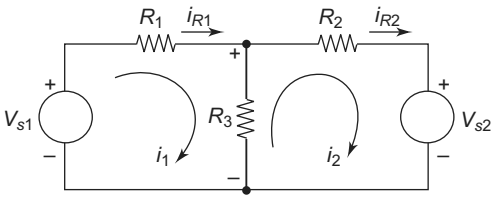


Fig. 2.3

Solution The two mesh currents (i_1, i_2) are indicated in Fig. 2.3. The currents in the resistances are

$$i_{R1} = i_1,\ i_{R2} = i_2,\ i_{R3} = i_1 - i_2 \tag{i}$$

The KVL equations for the two meshes can now be written down (sum of voltage drops) as,

Mesh 1

$$-v_{s1} + R_1 i_{R1} + R_3 i_{R3} = 0 \tag{ii}$$

Mesh 2

$$v_{s2} - R_2 i_{R2} + R_3 i_{R3} = 0 \tag{iii}$$

These equations are expressed in terms of mesh currents [as per Eq. (i)] as

$$-v_{s1} + R_1 i_1 + R_3 (i_1 - i_2) = 0 \tag{iv}$$

$$v_{s2} + R_2 i_2 - R_3 (i_1 - i_2) = 0 \tag{v}$$

These equations are reorganised below as

$$v_{s1} = (R_1 + R_3) i_1 - R_3 i_2 \tag{vi}$$

$$-v_{s2} = -R_3 i_1 + (R_1 + R_3) i_2 \tag{vii}$$

These are the requisite mesh equations.

Remark

1. The two mesh equations can be solved for mesh currents.
2. Currents in resistances can be obtained from the mesh current.
3. The reader should observe symmetry in mesh currents, so the mesh equations can be written down by inspection of the circuit.

2.3 SERIES AND PARALLEL COMBINATIONS OF RESISTANCES

Resistance in Series

A set of resistances are in series when the same current circulates through them as illustrated in Fig. 2.4.

❑ **By KVL**

$$v = R_1 i + R_2 i = (R_1 + R_2) i$$

$$\frac{v}{i} = R_{eq} = R_1 + R_2$$

In general

$$R_{\text{eq}} = \sum_i R_i \tag{2.1}$$

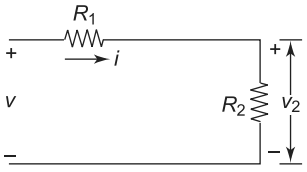


Fig. 2.4 *Circuit showing KVL*

Voltage division

$$v_2 = R_2\, i = R_2 \times \frac{v}{R_1 + R_2}$$

$$v_2 = kv = \left(\frac{R_2}{R_1 + R_2} \right) v \tag{2.2}$$

Resistances in Parallel

❑ **By KCL**

$$i = \frac{v}{R_1} + \frac{v}{R_2} = \left(\frac{1}{R_1} + \frac{1}{R_2} \right) v$$

$$\frac{i}{v} = \frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2}$$

or

$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = R_1 \| R_2 \tag{2.3}$$

In turns of conductances,

$$G_{eq} = G_1 + G_2$$

In general,

$$G_{eq} = \sum_i G_1$$

Current Division

Current i in Fig. 2.5 can be suitably divided into two parts by resistance R_1 and R_2 in parallel.

$$i_1 = \frac{v}{R_1} = \frac{1}{R_1}\left(\frac{R_1R_2}{R_1 + R_2}i\right)$$

$$= \frac{R_2}{R_1 + R_2}i \qquad (2.4)$$

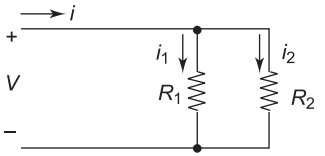


Fig. 2.5 *Circuit showing current division*

Similarly,

$$i_2 = \frac{R_1}{R_1 + R_2}i \qquad (2.5)$$

As per Eqs (2.4) and (2.5), current entering the node of two resistances in parallel divides among them in the inverse ratio of their resistances.

Example 2.3

By using the voltage divider circuit of Fig. 2.6, it is desired to obtain 3/4 V. Find R_2, given R_1 = 100 Ω.

A load resistance R_L is now connected in parallel with R_2. What will be the percentage change in output voltage if (a) R_L = 10 kΩ, and (b) R_L = 1 kΩ.

Solution

$$\frac{R_2}{R_1 + R_2} = \frac{3}{4}$$

$$\frac{R_2}{100 + R_2} = \frac{3}{4} = 0.75$$

or $R_2 = 300\ \Omega$

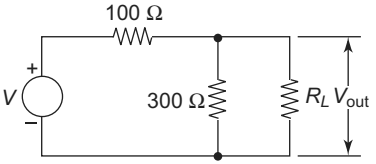


Fig. 2.6

Circuit with load R_L is drawn in Fig. 2.6.

(a) When R_L = 10 kΩ,

$$R_2(\text{eq}) = \frac{300 \times 10 \times 10^3}{10300} = 291.26\ \Omega$$

$$K = \frac{291.26}{391.26} = 0.744$$

Change in output voltage = (0.75 – 0.744) V = 0.006 V

$$\%\ \text{change} = \frac{0.006}{0.75} \times 100 = 0.8$$

(b) For R_L = 1 kΩ,

$$R_2(\text{eq}) = \frac{300 \times 1000}{1300} = 230.77\ \Omega$$

$$K = \frac{230.77}{330.77} = 0.698$$

Change in output voltage = (0.75 – 0.698) V = 0.052 V

Percentage change $= \dfrac{0.052}{0.75} \times 100 = 6.93$

❑ **Observation** As the load resistance is reduced to 1/10, the percentage change in output voltage rises from 0.8 to 6.93.

Example 2.4

In the resistance circuit of Fig. 2.7, find v_1 and i_2.

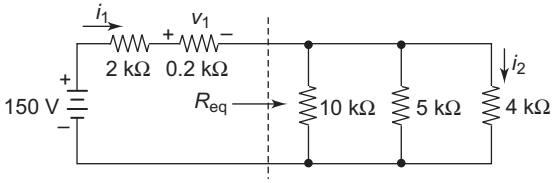


Fig. 2.7

Solution

$$\frac{1}{R_{eq}} = \frac{1}{10} + \frac{1}{5} + \frac{1}{4} = 0.55$$

$$R_{eq} = 1.82 \text{ k}\Omega$$

$$i_1 = \frac{150}{2 + 0.2 + 1.82} = 37.3 \text{ mA}$$

$$v_1 = 37.3 \times 0.2 = 7.46 \text{ V}$$

Voltage across $R_{eq} = 1.82 \times 37.3 = 67.886$ V

$$i_2 = \frac{67.886}{4} = 16.97 \text{ mA}$$

2.4 STAR (*Y*)-DELTA (Δ) CONVERSION

Certain network configurations cannot be resolved by series-parallel combinations alone. Such configurations are handled by *Y*-Δ *transformations*.

Figure 2.8(a) shows three Δ-connected resistances connected between three nodes—*a*, *b* and *c*.

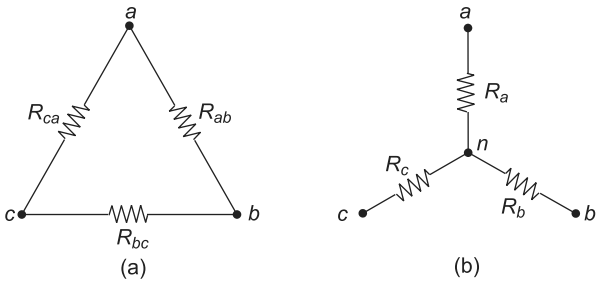


Fig. 2.8 *(a) Delta-connected, and (b) star-connected networks*

On the other hand, in Fig. 2.8(b), there are three *Y*-connected resistances. Notice that *Y*-connection has an extra node *n* that gets eliminated upon converting it to Δ. *Y*–Δ conversion is therefore a *node-reduction* technique.

Equating Resistance between Node Pairs

Node pair *ab*

$$R_a + R_b = R_{ab} \| (R_{bc} + R_{ca}) \tag{2.6}$$

Node pair *bc*

$$R_b + R_c = R_{bc} \| (R_{ca} + R_{ab}) \tag{2.7}$$

Node pair *ca*

$$R_c + R_a = R_{ca} \| (R_{ab} + R_{bc}) \tag{2.8}$$

We solve Eqs (2.6), (2.7) and (2.8).

❑ Y-Δ Conversion

$$R_{ab} = \frac{R_a R_b + R_b R_c + R_c R_a}{R_c} \tag{2.9a}$$

$$R_{bc} = \frac{R_a R_b + R_b R_c + R_c R_a}{R_a} \tag{2.9b}$$

$$R_{ca} = \frac{R_a R_b + R_b R_c + R_c R_a}{R_b} \tag{2.9c}$$

❑ Δ-Y Conversion

$$R_a = \frac{R_{ab} R_{ac}}{R_{ab} + R_{bc} + R_{ca}} \tag{2.10a}$$

$$R_b = \frac{R_{bc} R_{ba}}{R_{ab} + R_{bc} + R_{ca}} \tag{2.10b}$$

$$R_c = \frac{R_{ca} R_{cb}}{R_{ab} + R_{bc} + R_{ca}} \tag{2.10c}$$

❑ Balanced Y-Δ

A balanced *Y* ($R_a = R_b = R_c = R_Y$) leads to balanced Δ($R_{ab} = R_{bc} = R_{ca} = R_\Delta$) wherein

$$R_\Delta = 3R_Y \tag{2.11}$$

Example 2.5

Reduce the network of Fig. 2.9 to obtain the equivalent resistance as seen between nodes *ad*.

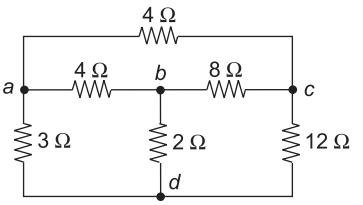


Fig. 2.9

Solution Converting the *Y* at Node *b* to Δ,

$$R_x = \frac{4 \times 8 + 8 \times 2 + 2 \times 4}{2} = 28\ \Omega$$

$$R_y = \frac{4\times 8 + 8\times 2 + 2\times 4}{8} = 7\ \Omega$$

$$R_z = \frac{4\times 8 + 8\times 2 + 2\times 4}{4} = 1.734\ \Omega$$

By series-parallel combination of Fig. 2.10, we get

$$R_{ad}(\text{eq}) = \frac{2.1\times(3.5+6.46)}{2.1+3.5+6.46} = 1.734\ \Omega$$

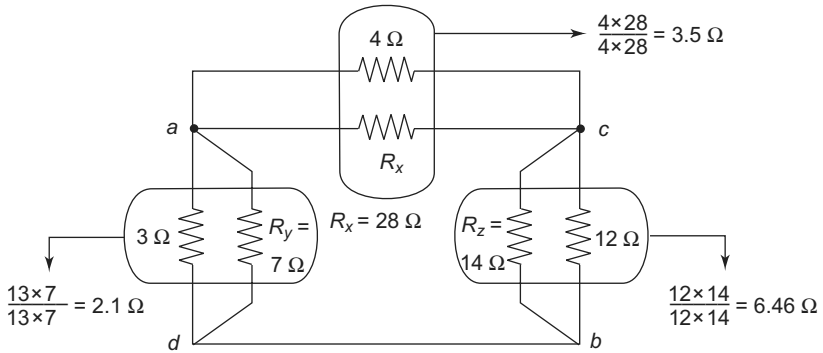


Fig. 2.10

2.5 SOURCE REPRESENTATION AND CONVERSION

In a practical voltage source, the voltage reduces as the load current is increased (by reducing load resistance). A practical source can be approximated by an ideal voltage source with a resistance in series as in Fig. 2.11.

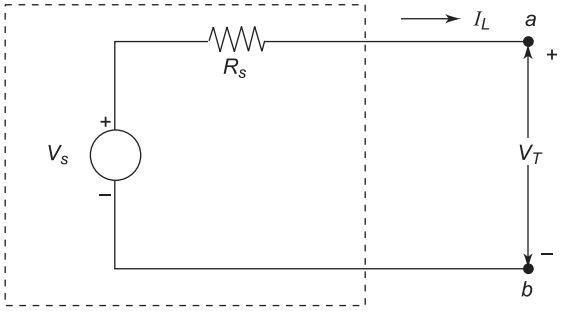


Fig. 2.11 *Practical voltage source*

The *V-I* characteristic of the source is represented by the equation

$$-V_s + R_s I_L + V_T = 0 \tag{2.12}$$

or
$$I_L = -\frac{1}{R_s} V_T + \frac{1}{R_s} V_s \tag{2.13}$$

This characteristic ($V_T - I_L$) is represented graphically in Fig. 2.12 wherein
I_{SC} = short-circuit current, i.e. source terminals shorted through zero resistance load ($V_T = 0$)
V_{OC} = open-circuit voltage, i.e. source terminals open ($I_L = 0$).

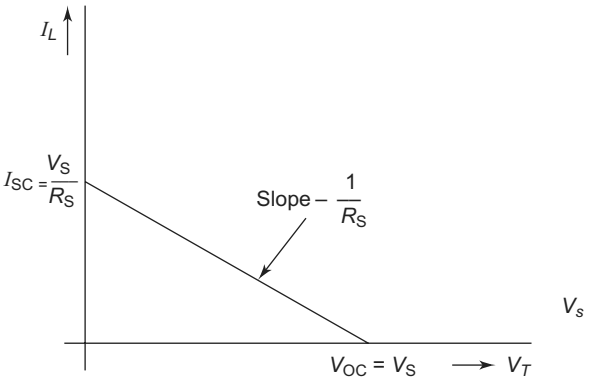


Fig. 2.12 *V-I characteristic of a practical voltage source*

A practical current source feeds a reducing current to a load resistance as its resistance is increased. It can be represented by an ideal current source with a resistance in parallel with it as in Fig. 2.13.

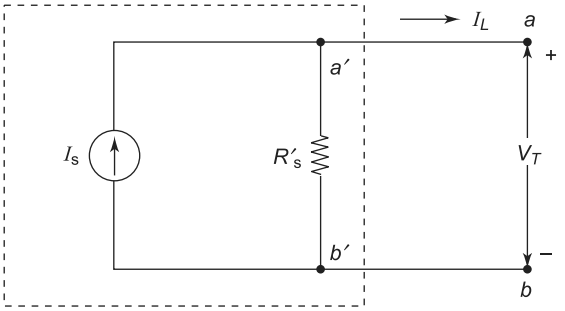


Fig. 2.13 *Practical current source*

Writing KCL equation at the node *a*'

$$-I_s + \frac{V_T}{R'_s} + I_L = 0$$

or
$$I_L = -\frac{1}{R'_s} V_T + I_s \tag{2.14}$$

The *V-I* characteristic as per Eq. (2.14) is drawn in Fig. 2.14, wherein
I_{SC} = short-circuit current, i.e. $V_T = 0$
V_{OC} = open-circuit voltage, i.e. $I_L = 0$
For the two practical source representations to be equivalent [comparing Eqs (2.13) and (2.14)],

$$R'_s = R_s$$

$$V_s = R'_S I_S = V_{OC} \text{ (open-circuit, i.e. source terminals open)}$$

Also, $I_s = \dfrac{V_s}{R_s} = I_{SC}$ (short-circuit, i.e. current through zero resistance load, connecting source terminals)

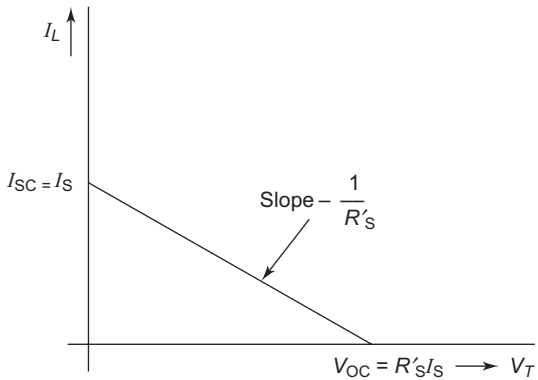


Fig. 2.14 *V-I characteristic of a practical current source*

Thus, source equivalence is also arrived at, by matching open-circuit voltages and short-circuit currents. This result is the consequence of the Thevenin and Norton theorems (Section 2.10).

It must be observed here, that the current direction of the equivalent current source must be such as to produce the same open-circuit terminal voltage polarity as in the voltage source.

It must be observed here that an ideal voltage source ($R_s = 0$) cannot be converted to current source (it would mean infinite current with a short-circuit in front). Similarly, an ideal current source cannot be converted to a voltage source.

General Methods of Circuit Analysis

In Section 2.2, we presented two basic laws of circuit theory—Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL). Based on these two laws, there are two general methods of circuit analysis: the nodal method based on KCL and the mesh method based on KVL. Before applying these methods, the circuit if possible is reduced in complexity by applying the reduction techniques presented in Sections 2.3 and 2.5.

Further in applying nodal and mesh method to analyse a circuit, inter-conversion of voltage and current sources may be needed. This conversion has been presented in Section 2.6.

2.6 NODAL ANALYSIS

It shall be assumed here that all sources are current sources and practical voltage sources, if any, have been converted to equivalent current source form.

Let the circuit have TV nodes in all. One of these nodes is chosen as the *reference* (*datum*) node. The voltages of the remaining $(N - 1)$ nodes with respect to the reference node form an independent set of variables that implicitly satisfy KVL equations (we shall observe in what follows that the voltage of any component is the difference of the voltages of the two nodes to which it is connected). $(N - 1)$ KCL equations are written down at the nodes. For a resistive network, this step results in $(N - 1)$ simultaneous algebraic equations in $(N - 1)$ nodal voltages. Once the nodal voltages are obtained, any voltage and current in the network can be obtained from these. In writing the nodal equations, it is convenient but not necessary to convert all resistance values to conductances before proceeding with the analysis.

For demonstration, consider the circuit of Fig. 2.15(a). The lower two nodes are identical and can be merged for clarity as in Fig. 2.15(b).

Applying KCL at nodes 1 and 2, respectively,

Node 1: $$-i_1 + G_2 v_1 + G_1(v_1 - v_2) = 0 \tag{2.15}$$

Node 2: $$i_2 + G_3 v_2 + G_1 (v_2 - v_1) = 0 \tag{2.16}$$

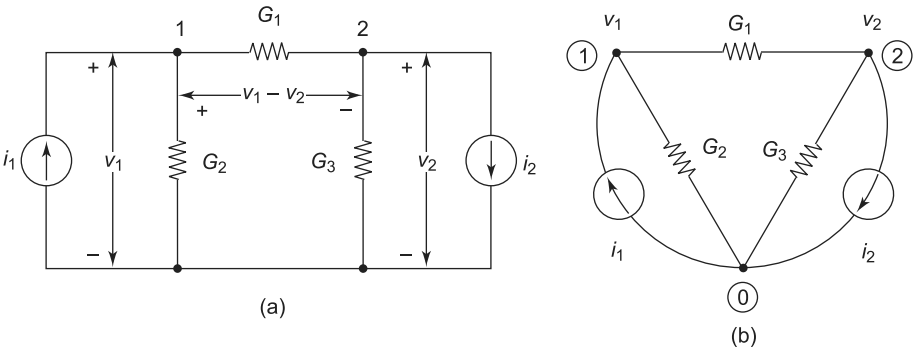


Fig. 2.15

Rearranging,

Node l: $$(G_1 + G_2)v_1 - G_1 v_2 = i_1 \tag{2.17}*$$

Node 2: $$-G_1 v_1 + (G_1 + G_3) v_2 = -i_2 \tag{2.18}*$$

With given values of i_1 and i_2 (source currents), Eqs. (2.17) and (2.18) can be solved for v_1 and v_2. It is possible to generalise these equations for an N-node system, which can be written by inspection.

*Equations (2.17) and (2.18) can be written in matrix form as

$$\begin{bmatrix} G_1 + G_2 & -G_1 \\ -G_1 & (G_1 + G_3) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \begin{bmatrix} i_1 \\ -i_2 \end{bmatrix}$$

or **[G][v] = [i]**

where **[G]** = node admittance matrix whose

diagonal elements = sum of all admittances connected at the node;

off-diagonal elements = minus the sum of all admittances connected between the two nodes (*ij*);

node admittances matrix is a symmetric matrix, where

[v] = vector of node voltages

[i] = vector of currents of all current sources entering at each node

* An efficient method of solving large number of linear algebraic equations is Gaussian Elimination [Ref. 1]. On the other hand, Cramer's rule is a very inefficient method as it requires computation of determinants.

Let $i_1 = 2\ A, i_2 = -3\ A$

$G_1 = 0.2, G_2 = 1, G_3 = 0.5$

Plugging in the values, we have

$1.2\ v_1 - 0.2\ v_2 = 2$

$-0.2\ v_1 + 0.7\ v_2 = 3$

Solving, we get

$v_1 = 5/2V\ v_2 = 5$ V

Example 2.6

For the circuit of Fig. 2.16(a), find all the node voltages and the currents in resistances 0.25 Ω and 1/3 Ω. Use the nodal method.

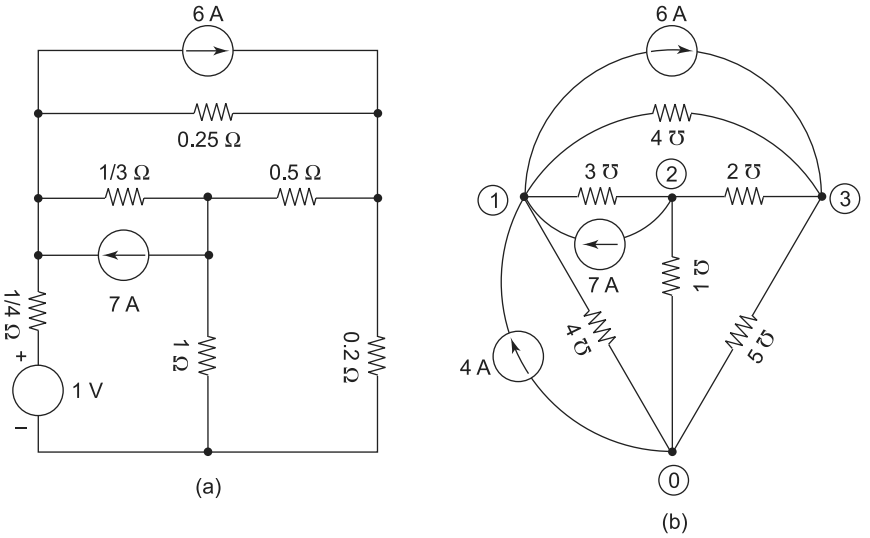


Fig. 2.16

Solution Since one of the sources is a voltage source with series resistance, it is first converted to a current source and all resistances are converted to conductances. The circuit is redrawn in Fig. 2.16(b) where four nodes are identified and labelled 1, 2, 3 and the datum node 0. Writing KCL equations at the three nodes:

Node 1: $(6 - 4 - 7) + 4\ v_1 + 3(v_1 - v_2) + 4(v_1 - v_3) = 0$

or $11\ v_1 - 3\ v_2 - 4\ v_3 = 5$ (i)

Node 2: $7 + v_2 = 3(v_2 - v_1) + 2(v_2 - v_3) = 0$

or $-3\ v_1 + 6\ v_2 - 2\ v_3 = -7$ (ii)

Node 3: $-6 + 5\ v_3 + 2(v_3 - v_2) + 4(v_3 - v_1) = 0$

or $-4\ v_1 - 2\ v_2 + 11\ v_3 = 6$ (iii)

Using Cramer's rule,

$$v_1 = \frac{\begin{vmatrix} 5 & -3 & -4 \\ -7 & 6 & -2 \\ 6 & -2 & 11 \end{vmatrix}}{\begin{vmatrix} 11 & -3 & -4 \\ -3 & 6 & -2 \\ -4 & -2 & 11 \end{vmatrix}}$$

$$= \frac{5\begin{vmatrix} 6 & -2 \\ -2 & 11 \end{vmatrix} + 7\begin{vmatrix} -3 & -4 \\ -2 & 11 \end{vmatrix} + \begin{vmatrix} -3 & -4 \\ 6 & -2 \end{vmatrix}}{11\begin{vmatrix} 6 & -2 \\ -2 & 22 \end{vmatrix} + 3\begin{vmatrix} -6 & -4 \\ -2 & 11 \end{vmatrix} - 4\begin{vmatrix} -3 & -4 \\ 6 & -2 \end{vmatrix}}$$

$$= \frac{5(62) + 7(-41) + 6(30)}{11(62) + 3(-41) - 4(30)}$$

$$= \frac{203}{439} = 0.462 \text{ V}$$

Similarly,

$$v_2 = \frac{\begin{vmatrix} 11 & 5 & -4 \\ -3 & -7 & -2 \\ -4 & 6 & 11 \end{vmatrix}}{439} = \frac{-326}{439} = -0.743 \text{ V}$$

and

$$v_3 = \frac{\begin{vmatrix} 11 & -3 & 5 \\ -3 & 6 & -7 \\ -4 & -2 & 6 \end{vmatrix}}{439} = \frac{254}{439} = -0.579 \text{ V}$$

$$i_{13}(0.25\ \Omega) = 4(0.462 - 0.579) = -0.468 \text{ A}$$

$$i_{12}(1/3\ \Omega) = 3(0.462 + 0.743) = 3.615 \text{ A}$$

Example 2.7

For the circuit of Fig. 2.17(a), determine v_x using nodal analysis.

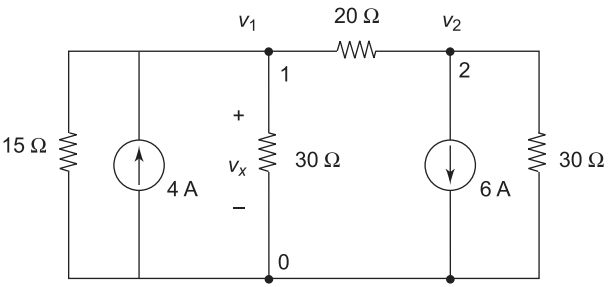


Fig. 2.17(a)

Solution The two nodes are identified as 1 and 2 with *datum* node as 0.

Combining resistances 15 Ω and 30 Ω, which are in parallel, gives the equivalent resistance

$$\frac{15 \times 30}{15 + 30} = 10\ \Omega$$

The circuit is redrawn in Fig. 2.17(b). The nodal equations are

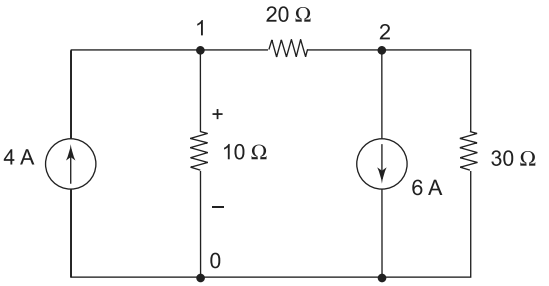


Fig. 2.17(b)

$$-4 + \frac{v_1}{10} + \frac{v_1 - v_2}{20} = 0$$

$$\left(\frac{1}{10} + \frac{1}{20}\right)v_1 - \frac{1}{20}v_2 = 4$$

$$3\,v_1 - v_2 = 80 \qquad \text{(i)}$$

Node 2

$$6 + \frac{v_2 - v_1}{20} + \frac{v_2}{30} = 0$$

$$-\frac{v_1}{20} + \left(\frac{1}{20} + \frac{1}{30}\right)v_2 = -6$$

$$-3\,v_1 + 5\,v_2 = 360 \qquad \text{(ii)}$$

Solving Eqs (i) and (ii), we get

$$v_1 = 3.333\ \text{V},\ v_2 = -70\ \text{V}$$

$$v_x = v_1 = 3.33\ \text{V}$$

Example 2.8

For the circuit of Fig. 2.18(a), determine the nodal voltages and current through the 2 Ω resistance.

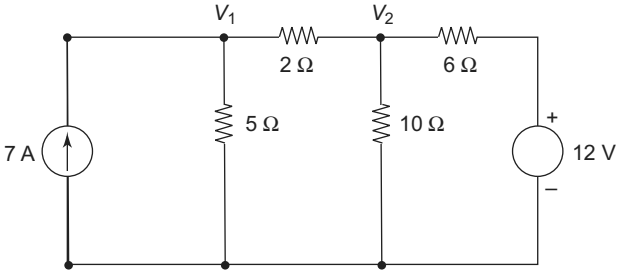


Fig. 2.18(a)

Solution Converting voltage source (practical) to current source, the circuit modifies as in Fig. 2.18(b).

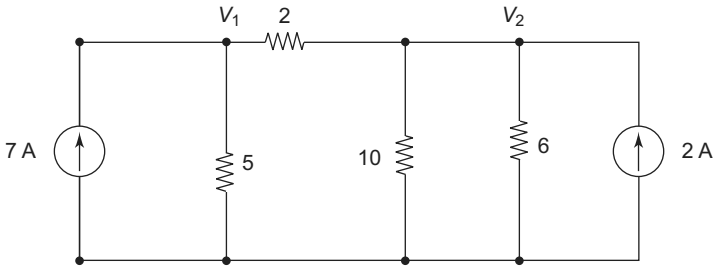


Fig. 2.18(b)

Nodal equations are

$$\left(\frac{1}{5}+\frac{1}{2}\right)V_1-\frac{1}{2}V_2=7 \quad \text{(i)}$$

$$-\frac{1}{2}V_1+\left(\frac{1}{10}+\frac{1}{6}+\frac{1}{2}\right)V_2=2 \quad \text{(ii)}$$

or $$0.7\,V_1-0.5\,V_2=7$$

$$-0.5\,V_1+0.767\,V_2=2$$

Solving, we get

$$V_1 = 22.2 \text{ V}, V_2 = 17.1\text{V}$$

$$I_{12} = (22.2 - 17.6)/2 = 2.55 \text{ A}$$

Example 2.9

For the circuit of Fig. 2.19, find the values of V_1 and V_2. Also, find the power input/output of the current and voltage sources.

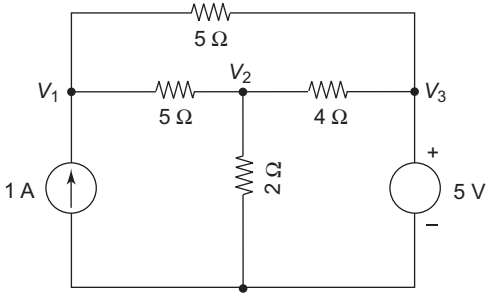


Fig. 2.19

Solution To apply nodal analysis, the 5 V source cannot be and need not be converted to current source as voltage V_3 is known to be + 5 V.

Node V_1

$$-1+\left(\frac{1}{5}+\frac{1}{5}\right)V_1-\frac{1}{5}V_2-\frac{1}{5}\times 5=0$$

Node *V*

$$-\frac{1}{5}V_1 + \left(\frac{1}{2}+\frac{1}{5}+\frac{1}{4}\right)V_2 - \frac{1}{4}\times 5 = 0$$

These equations are rewritten as

$$2V_1 - V_2 = 10$$

$$-4V_1 + 19V_2 = 25$$

Solving, we get

$$V_1 = 6.325 \text{ V}, V_2 = 2.65 \text{ V}$$

Current source output = $1 \times 6.325 = 6.325$ W
Current output of voltage source

$$= (5 - 2.65)/2 + (5 - 6.325)/5$$

$$= 0.91 \text{ A}$$

Output of voltage source = $5 \times 0.91 = 4.55$ W

Example 2.10

For the circuit of Fig. 2.20(a), use nodal analysis to determine V_x and V_s. What is the power consumed by the 6 Ω resistance?

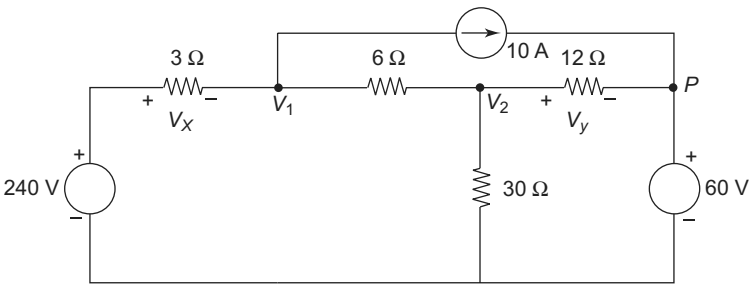


Fig. 2.20(a)

Solution At the node P, the voltage is fixed at +60 V, so there are two independent nodes V_1 and V_2. Convert voltage source of 240 V to a current source resulting in the circuit presented in Fig. 2.20(b).

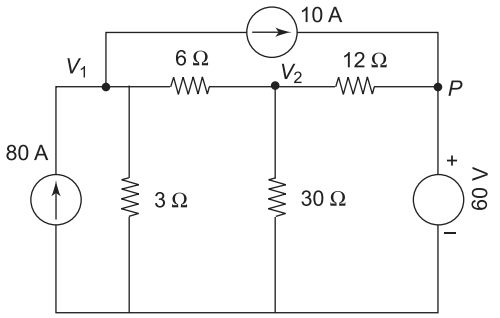


Fig. 2.20(b)

At Node V_1, $$-80 + \frac{V_1}{3} + 10 + \frac{V_1 - V_2}{6} = 0 \quad \text{(i)}$$

At Node V_2, $$\frac{V_2 - V_1}{6} + \frac{V_2 - 60}{12} + \frac{V_2}{30} = 0 \quad \text{(ii)}$$

Rewriting, $$\left(\frac{1}{3} + \frac{1}{6}\right)V_1 - \left(\frac{1}{6}\right)V_2 = 70 \quad \text{(iii)}$$

$$-\left(\frac{1}{6}\right)V_1 + \left(\frac{1}{6} + \frac{1}{12} + \frac{1}{30}\right)V_2 = 5 \quad \text{(iv)}$$

Solving, we get

$V_1 = 181.5$ V, $V_2 = 124.4$ V

$V_x = V_1 - 181.5$ V

$V_y = V_2 - 60 = 64.4$ V

Power consumed in the 6 Ω resistance

$$V(6\ \Omega) = V_2 - V_1 = 57.1 \text{ V}$$

$$\text{Power } (6\ \Omega) = \frac{(57.1)^2}{6} = 543.4 \text{ W}$$

2.7 MESH ANALYSIS

This is an alternative method of circuit analysis. The mesh-analysis algorithm is given below and is explained through the simple circuit of Fig. 2.21.

- Identify independent-circuit meshes. There are two such meshes in the circuit of Fig. 2.21.
- Assign a circulating current to each mesh (i_1, i_2 in Fig. 2.20). As each mesh current enters as well as leaves the mesh elements, the mesh currents implicitly satisfy KCL. It is preferable to assign the same direction to the mesh currents—usually clockwise.
- Write KVL equations for each mesh (as many as mesh currents). It is observed here that no circuit branch can carry more than two mesh currents.
- It is assumed that all circuit sources are voltage sources. Practical current sources, if any, are first converted to equivalent voltage sources.

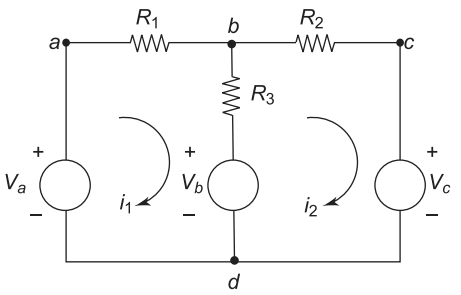


Fig. 2.21

Let us write KVL equations for the two meshes of Fig. 2.21.

Mesh 1: $R_1 i_1 + R_3(i_1 - i_2) + v_b - v_a = 0$ (2.19)

Mesh 2: $R_3(i_2 - i_1) + R_2 i_2 + v_c - v_b = 0$ (2.20)

These equations can be organised in the form below:

Mesh 1: $(R_1 + R_3)i_1 - R_3 i_2 = v_a - v_b$ (2.21)

Mesh 2: $-R_3 i_1 + (R_2 + R_3)i_2 = v_b - v_c$ (2.22)

Equations (2.19) and (2.20)* can be generalised and written down by inspection.

Example 2.11

Analyse the circuit of Fig. 2.22(a) by the mesh method. From the results, calculate the current in the 50 Ω resistance.

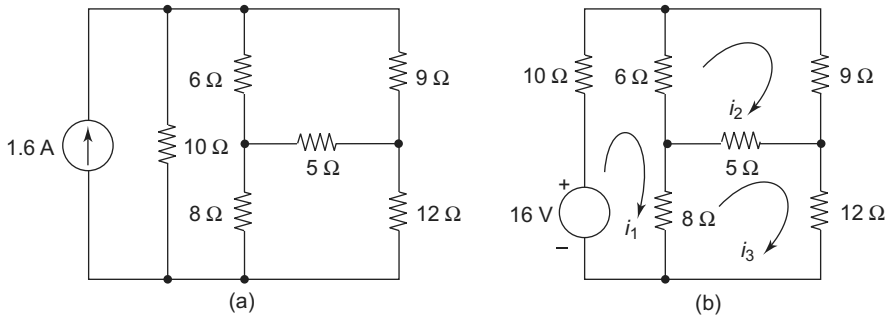


Fig. 2.22

Solution The practical current source of Fig. 2.22(a) is first converted to a voltage source as in Fig. 2.22(b). Three meshes are immediately identified with associated currents i_1, i_2 and i_3. KVL equations for the three meshes are written as follows (directly in organised form).

Mesh 1: $(10 + 6 + 8)i_1 - 6i_2 - 8i_3 = 16$

or $24\, i_1 - 6\, i_2 - 8\, i_3 = 16$ (i)

Mesh 2: $-6\, i_2 + (6 + 9 + 5)i_2 - 5\, i_3 = 0$

or $-6\, i_1 + 20\, i_2 - 5\, i_3 = 0$ (ii)

---

*Equations (2.19) and (2.20) can be written in the matrix form as

$$\begin{bmatrix} (R_1 + R_3) & -R_3 \\ -R_3 & (R_2 + R_3) \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} (v_a - v_b) \\ (v_b - v_c) \end{bmatrix}$$

or $[\mathbf{R}]\,[\mathbf{i}] = [\mathbf{v}]$

where $[\mathbf{R}]$ = mesh resistance (in general impedance) matrix whose
diagonal elements = sum of all resistances round the loop
off-diagonal elements = minus the sum of all resistances common to the loops (ij)
mesh resistance matrix is symmetric matrix

$[\mathbf{i}]$ = mesh currents vector

$[\mathbf{v}]$ = vector of algebraic sum of voltages of all voltage sources round the loop.

Mesh 3: $-8\,i_3 - 5\,i_2 + (8 + 5 + 12)i_3 = 0$

or $-8\,i_1 - 5\,i_2 + 25\,i_3 = 0$ (iii)

Solving Eqs. (i), (ii) and (iii),

$i_1 = 0.869$ A, $i_2 = 0.348$ A and $i_3 = 0.348$ A

Current through the 50 Ω resistance $= i_2 - i_3$
$= 0$ A

Resistances 6 Ω, 8 Ω, 9 Ω and 12 Ω form a *bridge*. When any resistance is connected across a *balanced bridge*, it will not carry any current. Also, observe

$$\frac{6\ \Omega}{8\ \Omega} = \frac{2}{3} = \frac{9\ \Omega}{12\ \Omega} = \text{(equal bridge arms ratio)}$$

Example 2.12

For the circuit of Fig. 2.23(a), determine the voltage across the 20 Ω resistance using mesh analysis.

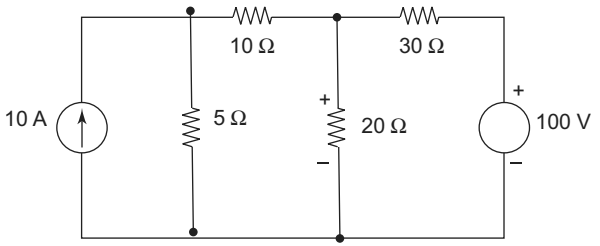


Fig. 2.23(a)

Solution Converting the practical current to a voltage source, we draw the circuit as in Fig. 2.23(b). Writing the two mesh equations,

$$-50 + 15i_1 + 20\,(i_1 - i_2) = 0 \quad \text{(i)}$$

or $$35\,i_1 - 20\,i_2 = 50 \quad \text{(ii)}$$

$$20\,(i_2 - i_1) + 30\,i_2 + 100 = 0 \quad \text{(iii)}$$

or $$-20\,i_1 + 50\,i_2 = -100 \quad \text{(iv)}$$

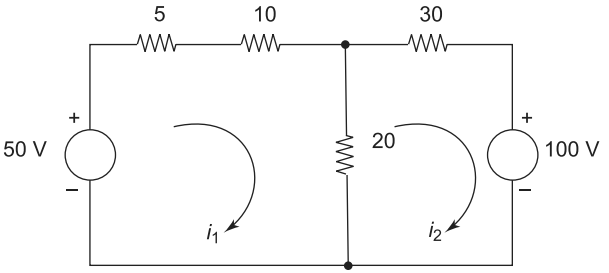


Fig. 2.23(b)

Solving Eqs (ii) and (iv), we get

$$i_1 = 0.37 \text{ A}, \; i_2 = -1.85 \text{ A}$$

Voltage across the 20 Ω resistance

$$v = 20\,(i_1 - i_2) = 20 \times 2.22 = 44.4 \text{ V}$$

Example 2.13

For the circuit of Fig 2.24, determine the value of resistance R such that $i_1 = 0.37$ A.

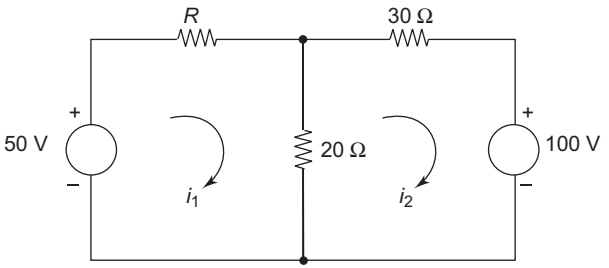


Fig. 2.24

Solution Mesh equations

$$-50 + Ri_1 + 20\,(i_1 - i_2) = 0$$

$$20\,(i_2 - i_1) + 30i_2 + 100 = 0$$

or

$$(R + 20)i_1 - 20i_2 = 50$$

$$-20i_1 + 50i_2 = -100$$

Eliminating i_2 and substituting $i_1 = 0.37$ A, we get

$$R = 15 \; \Omega$$

Example 2.14

Using mesh analysis, find currents I_1, I_2 and I_3 in the circuit of Fig. 2.25(a). Find also the power supplied by each ideal current source.

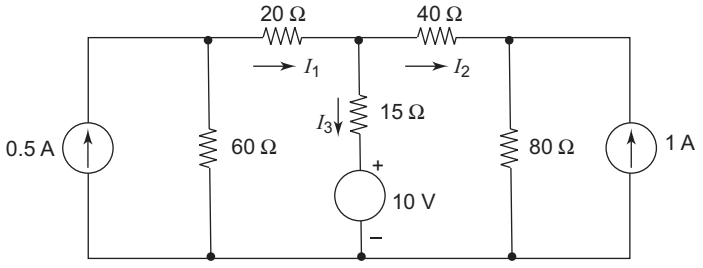


Fig. 2.25(a)

Solution Converting current sources to voltage source, the circuit diagram is drawn in Fig. 2.25(b).

The mesh equations are

$$-30 + 80\,i_1 + 15(i_1 - i_2) + 10 = 0$$

$$-10 + 15(i_2 - i_1) + 120\, i_2 + 80 = 0$$

or $$95\, i_1 - 15\, i_2 = 20 - 15\, i_1 + 135\, i_2 = -70$$

Solving, we get

$$i_1 = 0.13095 \text{ A}$$
$$i_2 = -0.504 \text{ A}$$
$$I_1 = i_1 = 0.13095 \text{ A}$$
$$I_2 = i_2 = -0.504 \text{ A}$$
$$I_3 = I_1 - I_2 = 0.63492 \text{ A}$$

Power supplied by current sources

0.5 A source

In Fig. 2.25(a), current through 60 Ω is 0.5 – 0.13095 = 0.36905

$$\text{Power} = (60 \times 0.36905) \times 0.5 = 11.0715 \text{ W}$$

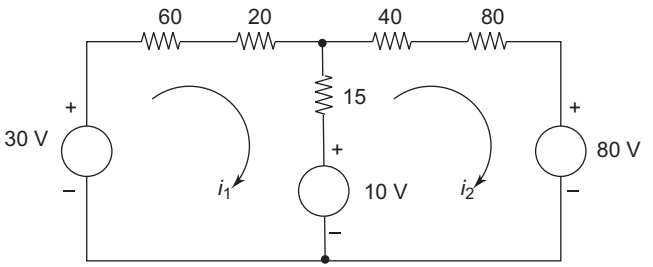


Fig. 2.25(b)

1 A source

In Fig. 2.25(b), current through 80 Ω is (1 + 72) = 1 – 0.504 = 0.496 A

$$\text{Power} = (80 \times 0.52) \times 1 = 39.68 \text{ W}$$

2.8 DEPENDENT SOURCES

The techniques of nodal and mesh analysis apply equally for circuits in which dependent sources are present. This will be demonstrated through two examples.

Example 2.15

For the circuit of Fig. 2.26, find the voltage v_{12} by the technique of nodal analysis.

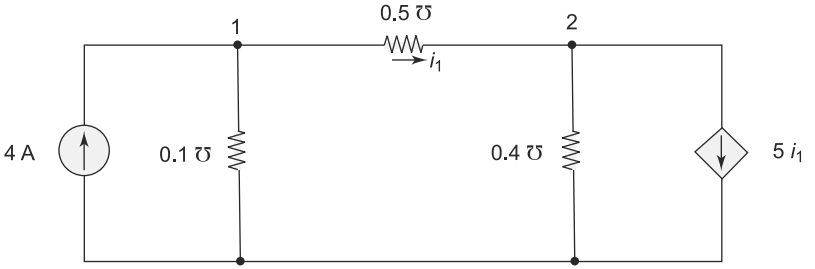


Fig. 2.26

Solution Writing nodal equations for nodes 1 and 2:

Node l: $-4 + 0.1\ v_1 + 0.5(v_1 - v_2) = 0$

or $0.6\ v_1 - 0.5\ v_2 = 4$ (i)

Node 2: $5\ i_1 + 0.4\ v_2 + 0.5(v_2 - v_1) = 0$

But $i_1 = 0.5\ (v_1 - v_2)$

$2.5\ (v_1 - v_2) + 0.4\ v_2 + 0.5\ (v_2 - v_1) = 0$

or $2\ v_1 - 1.6\ v_2 = 0$ (ii)

Solving Eqs (i) and (ii),

$v_1 = -160$ V; $v_2 = -200$ V

$v_{12} = -160 - (-200) = 40$ V

Example 2.16

For the circuit of Fig. 2.27, find v_1 using mesh analysis technique.

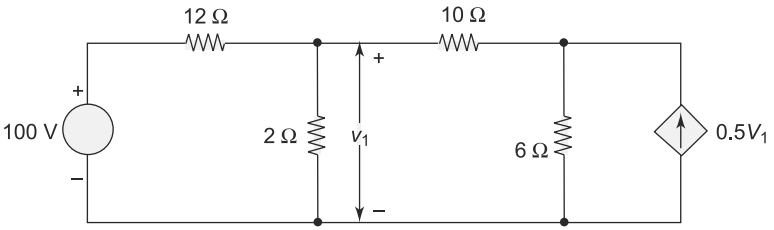


Fig. 2.27

Solution Converting the dependent current source with parallel resistance of 6 Ω to dependent voltage source, we can redraw the circuit of Fig. 2.27 as in Fig. 2.28.

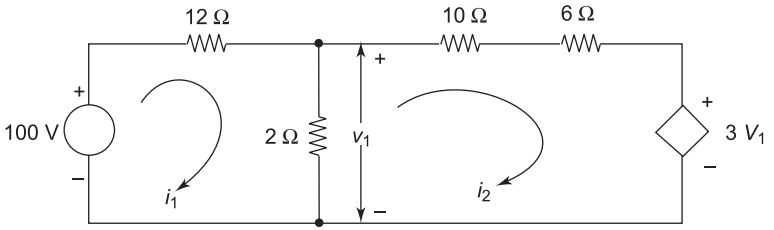


Fig. 2.28

Writing mesh equations for the circuit of Fig. 2.28,

Mesh 1: $14\ i_1 - 2\ i_2 = 100$ (i)

Mesh 2: $-2\ i_1 + 18\ i_2 = -3\ v_1$

But $v_1 = 2(i_1 - i_2)$

$\therefore$ $-2\ i_1 + 18\ i_2 = -6(i_1 - i_2)$

or $4\ i_1 + 12\ i_2 = 0$

Solving Eqs (i) and (ii),

$$i_1 = 6.82 \text{ A}; \; i_2 = -2.27 \text{ A}$$

$$v_1 = 2(i_1 - i_2)$$

$$= 2(6.82 + 2.27) = 18.2 \text{ V}$$

Comparison—Nodal vs Mesh Analysis

The choice between nodal or mesh analysis of a circuit depends upon the following factor:

- Number of simultaneous equations to be solved.
- If we need the answer in terms of voltage, the choice would be the nodal analysis. When the answer is needed in terms of current, the obvious choice is the mesh analysis. This not a rigid rule as by use of Ohm's law the answer in voltage can be converted to desired currents and vice versa.

We will illustrate by an example.

Example 2.17

Analyse the circuit of Fig. 2.29 by (a) nodal method, and (b) by mesh method. Compare the two.

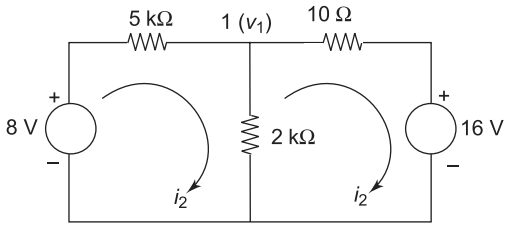


Fig. 2.29

Solution

(a) ***Nodal Method:*** There is only one independent node (1), the other (0) being the datum node. Note that the connections between voltage source and resistance need not be considered as node as voltages at these are known.

Nodal equation

$$\frac{(v_1 - 8)}{5} + \frac{v_1}{2} + \frac{v_1 - 16}{10} = 0$$

$$\left(\frac{1}{5} + \frac{1}{2} + \frac{1}{10}\right) v_1 = \frac{8}{5} + \frac{16}{10}$$

or $$(2 + 5 + 1)\, v_1 = 16 + 16 = 32$$

$$v_1 = \frac{32}{8} = 4 \text{ V}$$

If we need the current through (say) the 5 Ω resistance, it is found by Ohm's law.

$$i(5 \text{ k}\Omega) = \frac{8 - 4}{5} = 0.8 \text{ mA (source to Node 1)}$$

(b) Mesh Method: There are two meshes as shown in Fig. 2.29.

Mesh equation

$$-8 + 5\,i_1 + 2(i_1 - i_2) = 0$$

$$16 + 2\,(i_2 - i_1) + 10\,i_2 = 0$$

or

$$7\,i_1 - 2\,i_2 = 8$$

$$-2\,i_1 + 12\,i_2 = -16$$

Solving

$$i_1 = 0.8 \text{ mA}, \; i_2 = -1.2 \text{ mA}$$

Let us say we need the voltage at Node 1

$$v_1 = 2 \times (i_1 - i_2) = 2 \times 2 = 4 \text{ V}$$

Based on the number of equations, the choice here is in favour of the nodal method.

2.9 NETWORK THEOREMS—SUPERPOSITION THEOREM

Certain network theorems are very helpful in circuit analysis and give a simplified way of visualising the response of a complex network when connected to another network (usually simpler of the two).

Superposition Theorem

The response of a network (voltage across or current through an element) with several independent sources can be obtained as the sum of the responses to sources, taken one at a time as a consequence of circuit linearity. In removing sources other than one, voltage sources are short-circuited and current sources are open-circuited.

This will be illustrated with the help of an example. It may also be noted that sources are often called *forcing functions* (excitations or generators) and voltage and/or current desired are known as *responses*.

Example 2.18

In the circuit of Fig. 2.30(a), find the node voltages v_1 and v_2 using the *superposition theorem*.

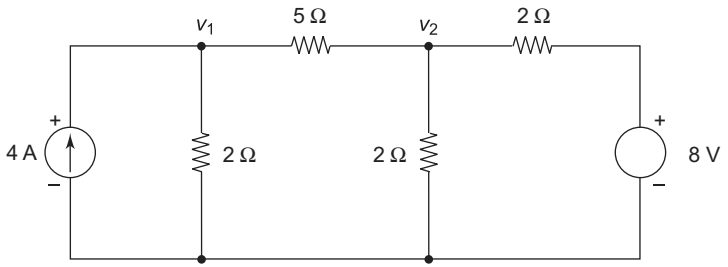


Fig. 2.30(a)

Solution

(a) Only the current source is applied and the voltage source is shorted. The resultant circuit is presented in Fig. 2.30(b).

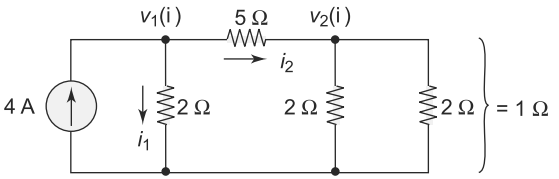


Fig. 2.30(b)

Solving, we get

$$i_1 = 4 \times \frac{6}{8} = 3 \text{ A}, \; v_1(\text{i}) = 3 \times 2 = 6 \text{ V}$$

$$i_2 = 4 \times \frac{2}{8} = 1 \text{ A}, \; v_2(\text{i}) = 1 \times 1 = 1 \text{ V}$$

(b) Voltage source only is applied with the current source open-circuited. The resultant circuit is represented in Fig. 2.31. Using series-parallel combination, the equivalent resistance in series with the source is

$$\frac{2 \times 7}{2+7} = \frac{14}{9}$$

$$v_2(\text{i}) = 8 \times \left(\frac{14/9}{2+14/9} \right) = \frac{7}{2} \text{V}$$

$$v_1(\text{ii}) = \frac{7}{2} \times \frac{2}{2+5} = 1 \text{ V}$$

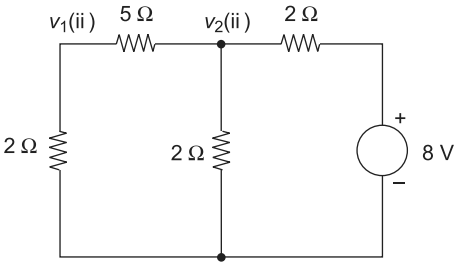


Fig. 2.31

Using the superposition theorem,

$$v_1 = v_1 \text{ (i)} + v_1 \text{ (ii)} = 6 + 1 = 7 \text{ V}$$

$$v_2 = v_2 \text{ (i)} + v_2 \text{ (ii)} = 1 + \frac{7}{2} = \frac{9}{2} \text{V}$$

2.10 THEVENIN AND NORTON THEOREMS

These theorems reduce a complex network as seen from two terminals into a simple circuit so that when another network (load) is connected at these terminals, its responses can be easily determined.

This situation is illustrated in Fig. 2.32. *Thevenin* and *Norton* equivalents of N_1 as seen from terminals *ab* are given in Fig. 2.33(a) and (b) respectively. Here,

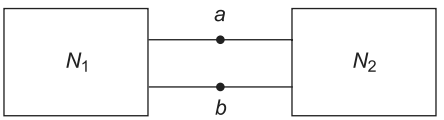


Fig. 2.32

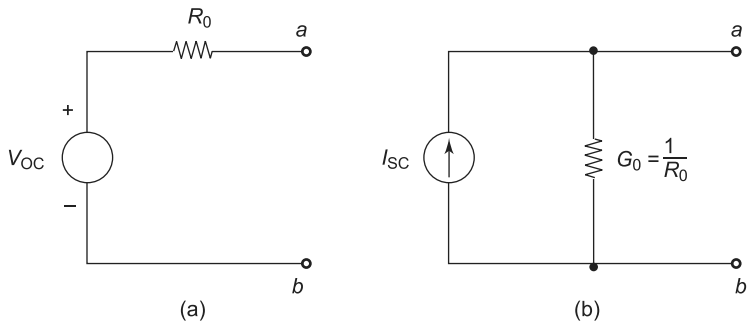


Fig. 2.33 *(a) Thevenin equivalent (b) Norton equivalent*

V_{oc} = *open-circuit* voltage at *ab* (when network N_2 is disconnected); voltage of *a* with respect to *b*.

R_0 = equivalent resistance (of N_1) as seen from *ab* with all voltage sources short-circuited and all current sources open-circuited.

I_{sc} = short-circuit current which flows from *a* to *b* when terminals *ab* are shorted after disconnecting N_2. Observe that the direction of current in Norton equivalent is such as to produce the same open-circuit polarity as in the Thevenin's equivalent.

It is easily seen that the Norton equivalent follows from the Thevenin equivalent by source conversion and also vice versa. In the Thevenin equivalent, we will write

$$V_{oc} = V_{TH}, \text{ the Thevenin voltage}$$

$$R_0 = R_{TH}, \text{ the Thevenin resistance}$$

In the Norton equivalent, we will write

$$R_0 = R_N, \text{ the Norton resistance}$$

Obviously,

$$R_N = R_{TH}$$

From the source conversion results of Section 2.5, it immediately follows that

$$I_{SC} = \frac{V_{OC}}{R_0} = \frac{V_{TH}}{R_{TH}} \tag{2.23}$$

When N_2 is connected at terminals *ab* of the Thevenin/Norton equivalent, it will yield an identical response. However, the information on currents and voltages in the elements of N_1 prior to connecting N_2 is lost.

When dependent sources are present, the above equivalents assume that a dependent source and its associated current/voltage are both located in N_1. The Thevenin theorem is particularly useful when the load is to take on a series of values.

When dependent sources are present in N_1, it is convenient to obtain R_{TH} from Eq. (2.23) as

$$R_{TH} = \frac{V_{OC}}{I_{SC}} \tag{2.24}$$

Thus, in a practical circuit, R^*_{TH} can be obtained from two measurements, open-circuit voltage and short-circuit current. However, care should be taken in short-circuiting the output terminals.

---

*Thevenin resistance is found experimentally on similar lines. Where the output cannot be short-circuited, some external resistance may be used. Thevenin resistance is the output resistance of some circuits like amplifiers.

Example 2.19

Find the Thevenin and Norton equivalents of the circuit of Fig. 2.34 as seen at terminal *ab*.

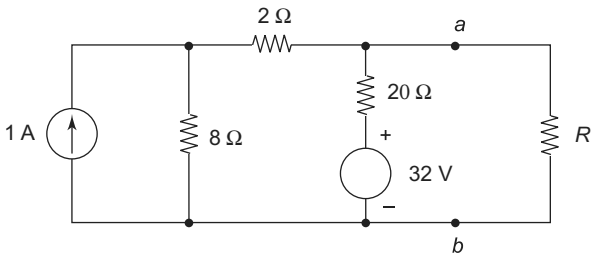


Fig. 2.34

Solution *Thevenin Equivalent*

- Remove load resistance R causing open-circuit at *ab*.
- Replace the 1 A source and 80 Ω resistance in parallel with it by its equivalent voltage source. The circuit is drawn in Fig. 2.35.

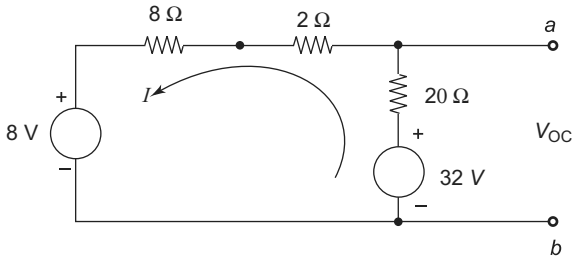


Fig. 2.35

In Fig. 2.35,

$$I = \frac{32 - 8}{30} = 0.8 \text{ A}$$

$$V_{OC} = 32 - 20 \times 0.8 = 16 \text{ V}$$

Open-circuit the 1 A source and short-circuit the 32 V source. The resulting circuit is drawn in Fig. 2.36.

$$R_0 = \frac{20 \times 10}{20 + 10} = \frac{20}{3} \Omega$$

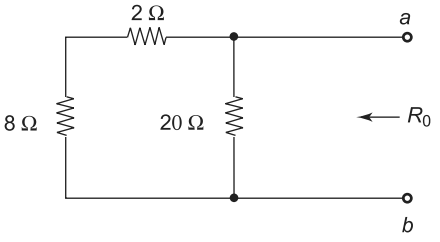


Fig. 2.36

The Thevenin equivalent is drawn in Fig. 2.37.

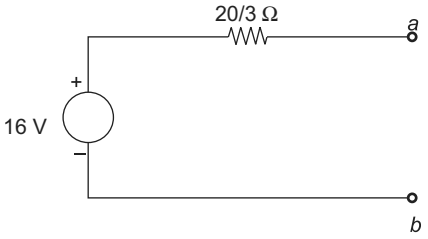


Fig. 2.37

Norton Equivalent

Short circuit at *ab* as shown in Fig. 2.38.

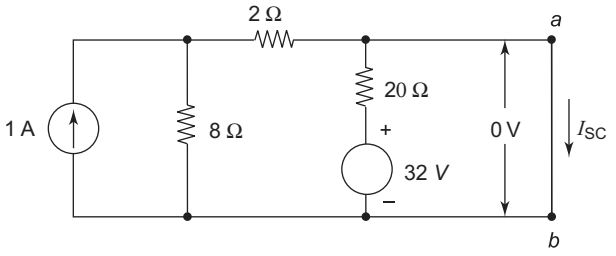


Fig. 2.38

As before, the circuit of Fig. 2.38 modifies to that of Fig. 2.39.

$$I_{SC} = \frac{32}{20} + \frac{8}{10} = \frac{48}{20} = 2.4\,\text{A}$$

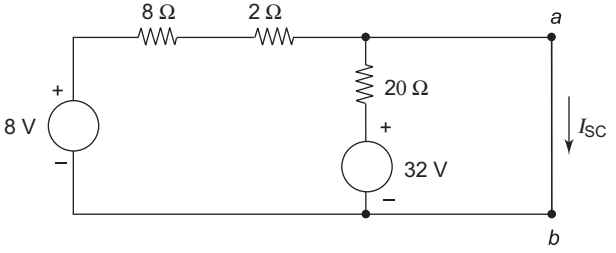


Fig. 2.39

As calculated in Thevenin equivalent,

$$R_0 = \frac{20}{3}\,\Omega$$

Norton equivalent is drawn in Fig. 2.40.

Check: $V_{OC} = 2.4 \times 20/3 = 16$ V (same as in Thevenin equivalent)

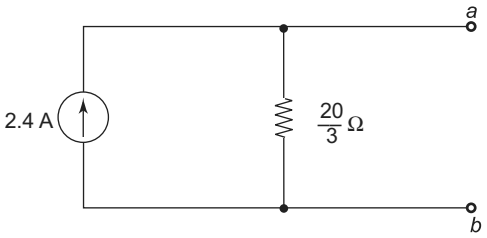


Fig. 2.40

Example 2.20

For the circuit of Fig. 2.34, find the Thevenin voltage and Norton current using the principle of superposition.

Solution **Thevenin voltage source**

(a) *Open-circuit current source:* The circuit is now drawn in Fig. 2.41(a).
With terminals *a*, *b* open

$$V_{OC_1} = \frac{32}{20+2+8} \times (8+2) = \frac{32}{3} \text{ V}$$

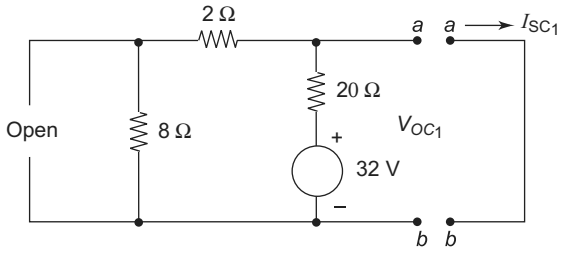


Fig. 2.41(a)

With terminals *a*, *b* shorted,

$$I_{SC_1} = \frac{32}{20} = 1.6 \text{ A}$$

(b) *Short-circuit voltage source:* The circuit is now drawn in Fig. 2.41(b).

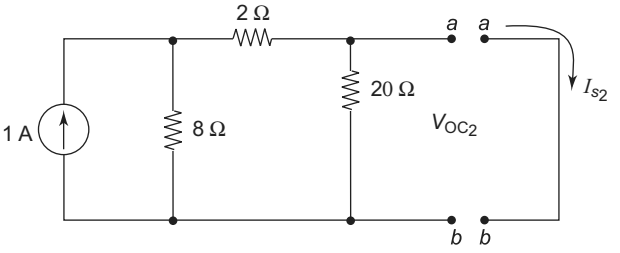


Fig. 2.41(b)

$$V_{OC_2} = 1 \times \frac{8}{8+2+20} \times 20 = \frac{16}{3} \text{ V}$$

$$I_{SC_2} = 1 \times \frac{8}{8+2} = 0.8 \text{ A}$$

By superposition,

$$V_{OC} = V_{OC_1} + V_{OC2} = \frac{32}{3} + \frac{16}{3} = 16 \text{ V}$$

$$I_{SC} = I_{SC_1} + I_{SC2} = 1.6 + 0.8 = 2.4 \text{ A}$$

2.11 MAXIMUM POWER TRANSFER THEOREM

When a network is loaded by a resistance at two of its terminals, the situation can be represented by the Thevenin equivalent as in Fig. 2.42. We want to investigate the power delivered to load resistance R_L as it is varied.

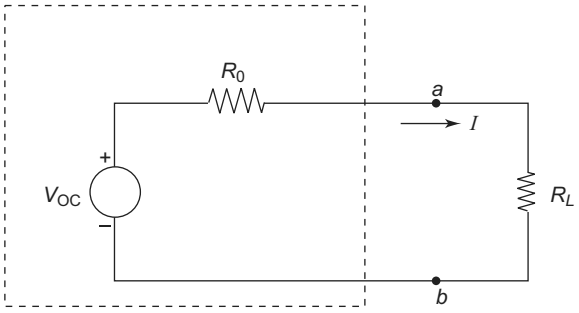


Fig. 2.42

Load power, $P_L = I^2 R_L$

$$= \left(\frac{V_{OC}}{R_0 + R_L} \right)^2 R_L$$

Maximum power delivered to the load is found from the condition

$$\frac{dP_L}{dR_L} = 0$$

which gives the result

$$R_L = R_0 \tag{2.25}$$

The condition of Eq. (2.24) which states that *power delivered (transferred) to load is maximum when load resistance equals the Thevenin resistance of the source is known as the maximum power transfer theorem.*

With reference to the circuit of Fig. 2.42, under conditions of maximum power transfer.

Power output by source $$P_S = V_{OC} \times \frac{V_{OC}}{2R_L}$$

$$= \frac{V_{OC}^2}{2R_L}$$

But $$P_L = \left(\frac{V_{OC}}{2R_L}\right)^2 R_L = \frac{V^2{}_{OC}}{4R_L}$$

Hence, the efficiency of power transfer

$$\eta = \frac{P_L}{P_S} = \frac{1}{2} \text{ or } 50\%$$

This is too low an efficiency for energy-conversion devices. Such devices must have load resistance far larger than that corresponding to the condition of maximum power transfer. However, in electronic devices, the objective is to obtain maximum power output irrespective of device efficiency and hence the condition is always used at the power stage of an electronic system. Of course, the 50% power lost in the system (devices and components) must be suitably dissipated to limit temperature rise.

Example 2.21

For the network of Fig. 2.43, find the value of the battery current (I) using network-reduction techniques.

Solution With reference to Fig. 2.43, convert delta ABD to star, so that the circuit takes the form of Fig. 2.44 where

$$R_{AN} = (8 + 12)/(8 + 12 + 4) = 4\ \Omega$$

$$R_{BN} = (8 + 4)/24 = 1.33\ \Omega$$

$$R_{DN} = (4 \times 12)/24 = 2\ \Omega$$

Using the series-parallel reduction technique, we get

$$R_{eq} = 10 + 4 + (1.33 + 15) \parallel (2 + 16) = 22.56\ \Omega$$

$$I = 12/22.56 = 0.532\ \text{A}$$

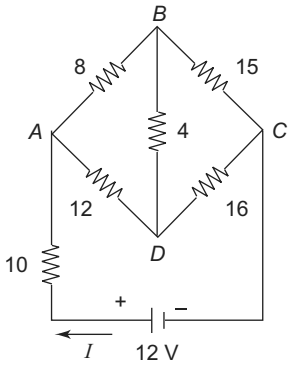


Fig. 2.43

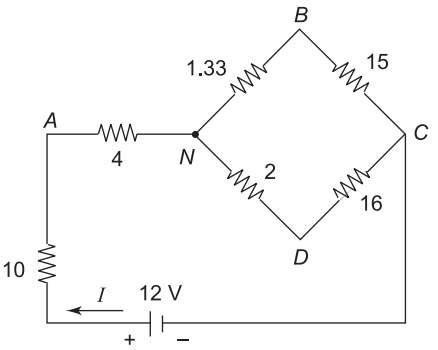


Fig. 2.44

Example 2.22

Find the Norton equivalent of the circuit of Fig. 2.45 at *ab*.

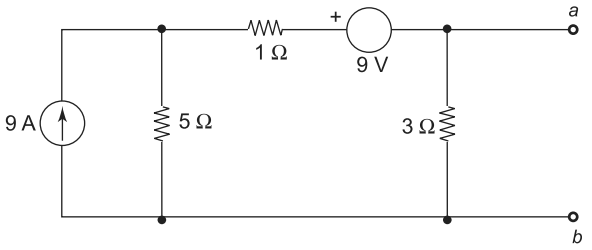


Fig. 2.45

Solution Short-circuiting *ab* and converting the current source to a voltage source as in Fig. 2.46 (a), we get

$$I_{SC} = (45 - 9)/6 = 6 \text{ A}$$

Short-circuiting the voltage source and open-circuiting the current source as in Fig. 2.46 (b), we obtain

$$R_0 = (5 + 1) \parallel 3 = 2\ \Omega$$

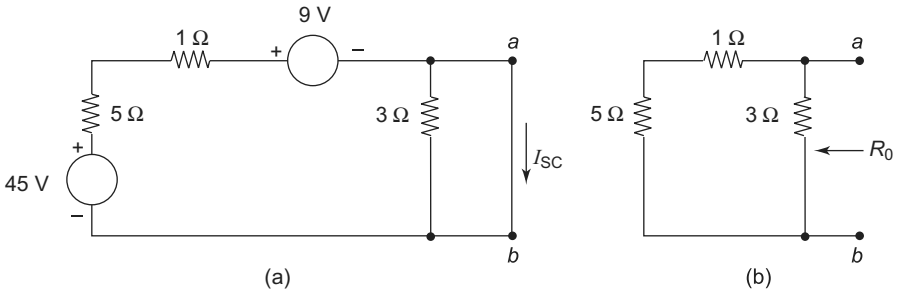


Fig. 2.46

The Norton equivalent is drawn in Fig. 2.47. Notice that the direction of the current in the current source in the equivalent is such, as to cause the short-circuit current at *ab* in the same direction as shown in Fig. 2.46.

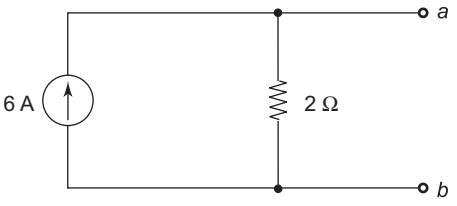


Fig. 2.47

Example 2.23

In the circuit of Fig. 2.48(a), determine the power dissipated in resistor *R*.

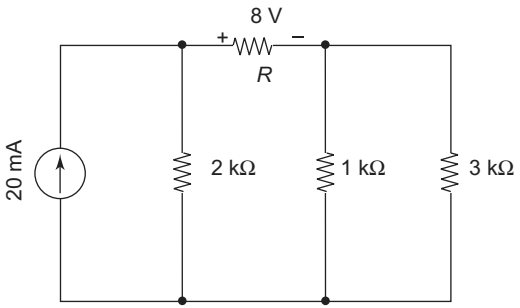


Fig. 2.48(a)

Solution To begin with, we will take two steps:

$\Rightarrow \quad 1 \parallel 3 = 0.75\ \Omega$

$\Rightarrow$ Convert current source to voltage source

$$V = 20 \times 2 = 40\ \text{V}$$

The circuit is now drawn as in Fig. 2.48(b).

$$I = \frac{40 - 8}{2 + 0.75} = 11.64\ \text{mA}$$

Power dissipated in *R*

$$P = VI = 8 \times 11.64 = 93.12\ \text{mW}$$

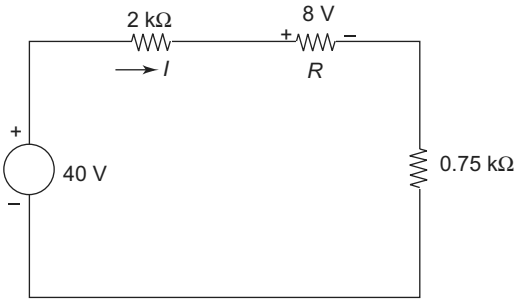


Fig. 2.48(b)

Example 2.24

In the resistance circuit of Fig. 2.49, find

(a) I_s if I_1 = 12 mA (b) I_s if I_2 = 20 mA

(c) I_2 if I_x = 6 mA (d) I_x if I_s = 45 mA

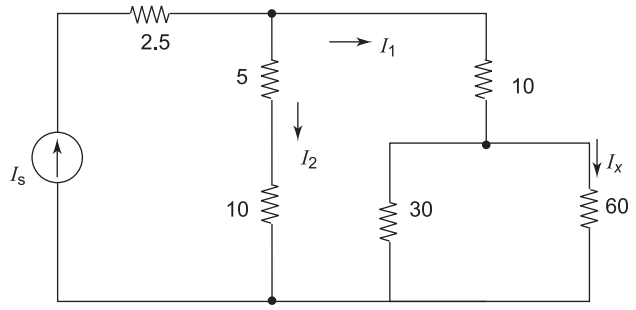


Fig. 2.49

Solution

(a) By current division,

$$I_x = 12 \times \frac{30}{30+60} = 4 \text{ mA}$$

(b) Voltage across (5 + 10) = 15 Ω

$$V_2 = 15\, I_2 = 15 \times 20 = 300 \text{ mV}$$

$$R_1 = (30 \parallel 60) + 10 = 30\ \Omega$$

$$\therefore \quad I_1 = \frac{V_2}{R_1} = \frac{300}{30} = 10 \text{ mA}$$

Then $$I_x = 10 \times \frac{30}{30+60} = \frac{10}{3} = 10 \text{ mA}$$

(c) $$I_x = I_1 \times \frac{30}{30+60}$$

or $$I_x = \frac{90}{30} \cdot I_x = 3 \times 6 = 18 \text{ mA}$$

(d) The current I_s flows through 2.5 Ω and then divides as I_1 and I_2.

$$I_1 = I_s \times \frac{R_2}{R_1 + R_2};\ R_1 = 5 + 10 = 15\ \Omega,\ R_2 = 30\ \Omega$$

$$I_1 = 45 \times \frac{30}{15+30} = 30 \text{ mA}$$

Again by current division,

$$I_x = 30 \times \frac{30}{30+60} = 10 \text{ mA}$$

Summary

- The equivalent resistance of N series resistors is $R_{eq} = R_1 + R_2 + \cdots + R_N$.
- The equivalent resistance of N parallel resistors is $\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_N}$.
- Star/delta conversion of three resistors aids in reduction of passive resistor network.
- Before applying general methods of network analysis, if possible, the passive part of the network should be reduced by the above three ways.
- The general methods of circuit analysis are the nodal method and mesh method. These have been well summarised in the text.
- Superposition is often used when the contribution of individual sources to the complete response of the circuit is required.
- Circuit model of a practical voltage source is an ideal voltage source with a series resistance.
- Circuit model of a practical current source is an ideal current source with a resistance in parallel to it.

- A practical voltage source can be converted to practical current source and vice versa. The same is not possible for ideal voltage and current sources.
- Inter-conversion of sources (sometimes repeatedly) greatly simplifies circuit analysis.
- The Thevenin equivalent of a network at two of its terminals is an independent voltage source with a resistance in series with it.
- The Norton equivalent of a network at two of its terminals is an independent current source with a resistance in parallel with it.
- At two terminals of a network, $V_{TH} = V_{OC}$ and R_{TH} is the resistance seen from the terminals with all voltage sources in the network short-circuited and all current sources open-circuited. The dependent sources are left as they are.
- The Norton equivalent current is I_{sc}, the short-circuit current at the terminals. The Norton resistance $R_N = R_{TH}$. Also $I_{SC} = V_{TH}/R_{TH}$.

$$R_{TH} = \frac{V_{OC}}{I_{SC}}$$

- Maximum power is transferred to a load at two of a network when $R_L = R_{TH}$.

Exercises

Review Questions

1. In the voltage dividing circuits of Fig. 2.4, investigate the effect of load R_L across R_2 on the voltage division ratio K.
2. In the current dividing circuit of Fig. 2.7, investigate the effect of connecting load resistance R_L across the current divider.
3. Define a mesh.
4. A node where only two elements meet does not require a nodal equation. Explain why.
5. Give one important basis for the choice between nodal and mesh analysis of a circuit.
6. Superposition theorem is applicable only for which circuits?
7. As seen from two terminals of a circuit, how are V_{OC} and I_{SC} related to the Thevenin resistance R_{TH}?
8. Show that the Thevenin and Norton equivalents of a network have the same value of the resistance.
9. Explain how a practical voltage source is converted to a current source.
10. Explain how a practical current source is converted to a voltage source.
11. Prove the maximum power transfer theorem.

Problems

1. For the resistive circuit of Fig. 2.50, using the method of series-parallel combination, find V_1 and I_2.

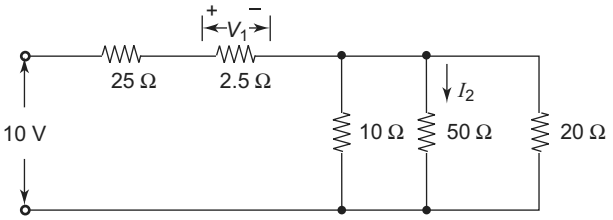


Fig. 2.50

2. In the circuit of Fig. 2.51, each resistance is l Ω. Find the value of V_1.

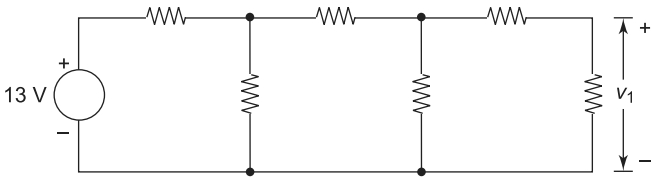


Fig. 2.51

3. In Fig. 2.52, find the value of R_{eq}.
4. For the circuit shown in Fig. 2.53, find the equivalent resistance between (a) *A* and *B,* and (b) *A* and *N*.

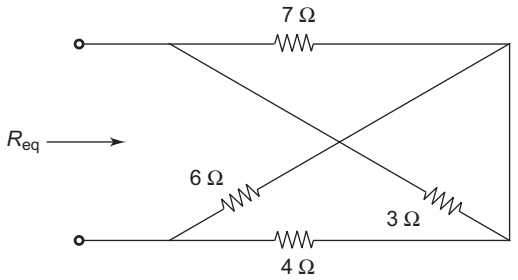


Fig. 2.52

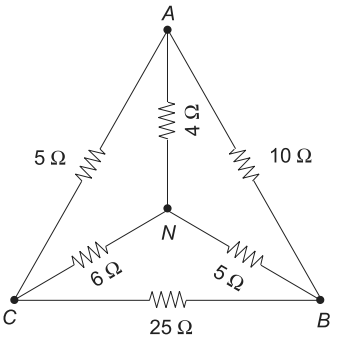


Fig. 2.53

5. For the circuit of Fig. 2.54, find the nodal voltages and the current through the 2 Ω resistance.

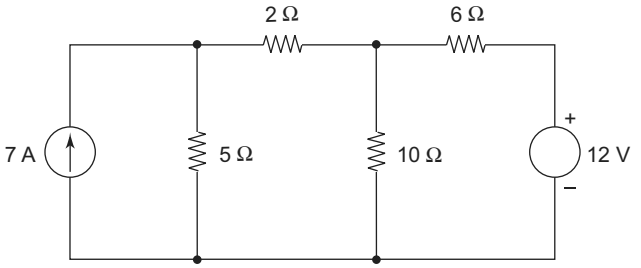


Fig. 2.54

6. For the circuit of Fig. 2.55, find the nodal voltages. From the symmetry of nodal equations, attempt to draw generalised conclusions.

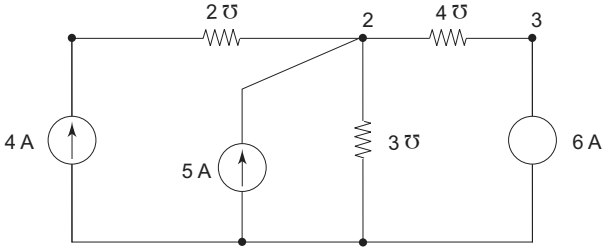


Fig. 2.55

7. In the circuit of Fig. 2.56, find the voltage V_1 across the 6 Ω resistance using (a) nodal method, and (b) mesh method of circuit analysis.
8. In the bridge circuit of Fig. 2.57, find the current through the 10 Ω resistance across *BD*. It is suggested that you use mesh method of analysis.

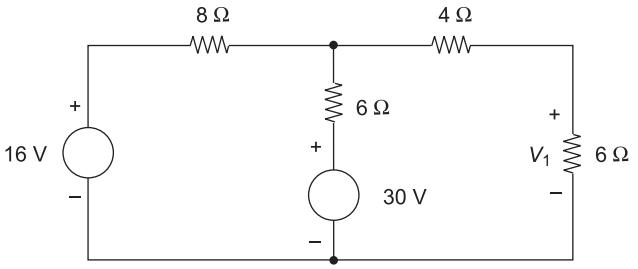


Fig. 2.56

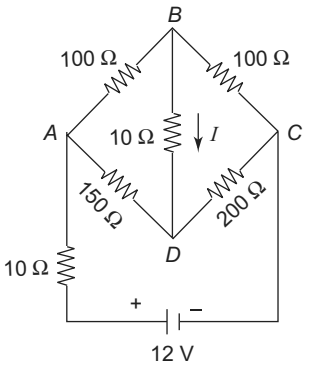


Fig. 2.57

9. For the circuit of Fig. 2.58, determine the currents in all the elements.

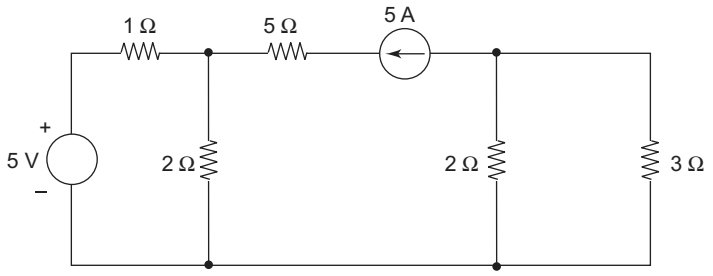


Fig. 2.58

10. For the circuit of Fig. 2.59, write the nodal equations in terms of node to datum voltages V_1 and V_2. Solve for V_1 and V_2. Hence, find
    (a) Direction and magnitude of current through 5 Ω, resistance
    (b) Power output/input to the current and voltage sources

    Hint: Voltage source being ideal cannot be converted to current source.

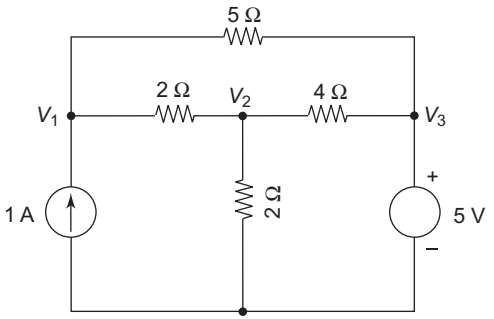


Fig. 2.59

11. Using mesh analysis, find currents I_1, I_2 and I_3 in the circuit of Fig. 2.60. Also, find the power supplied by the two current sources.

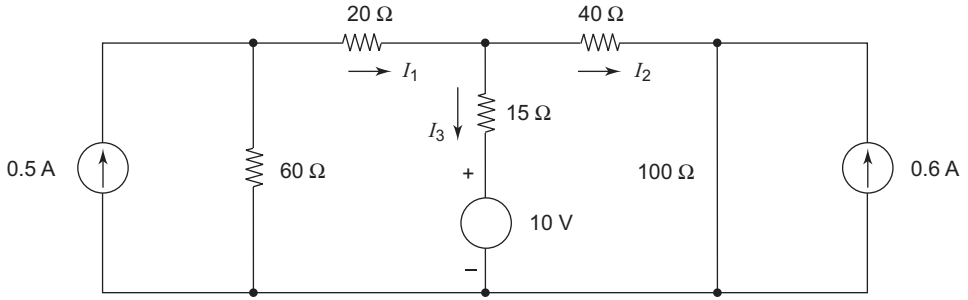


Fig. 2.60

12. Find the voltage across the 10 Ω resistance in Fig. 2.61 using (a) nodal method, and (b) mesh method.

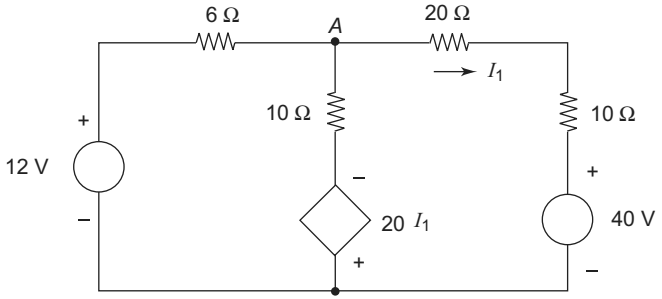


Fig. 2.61

13. Using nodal technique, determine I_1 in the circuit of Fig. 2.62.

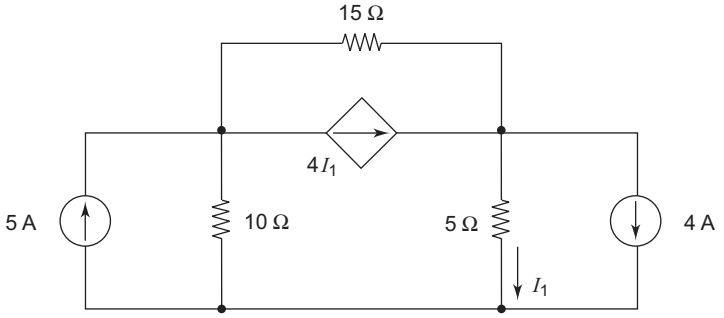


Fig. 2.62

14. In the circuit of Fig. 2.63, if
    (a) $V_s = 16$ V, find I_s for $I = 0$
    (b) $I_s = 16$ A, find V_s for $I = 0$

Use the principle of superposition.

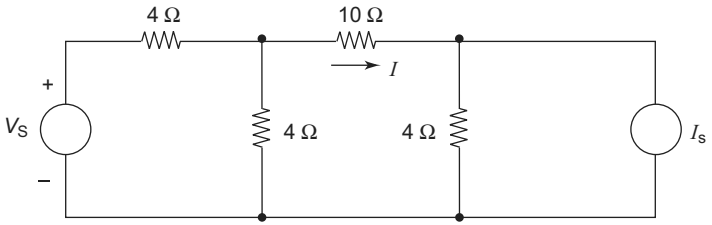


Fig. 2.63

15. For the circuit of Fig. 2.64, find V and I by using the principle of superposition.
16. For the bridge circuit shown in Fig. 2.65, find the galvanometer (G) current using Thevenin equivalent as seen at BD.

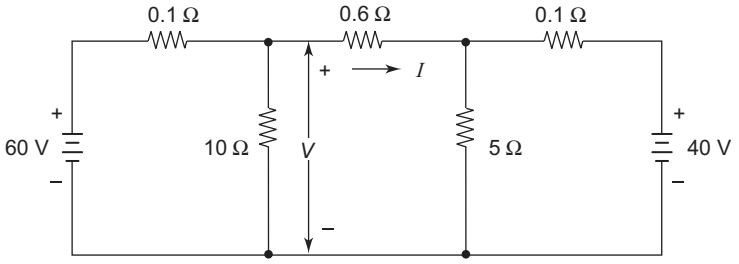


Fig. 2.64

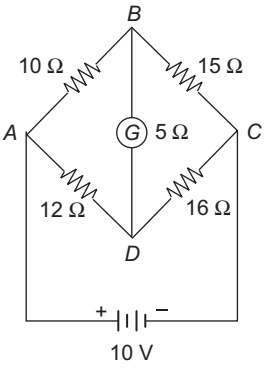


Fig. 2.65

17. For the circuit of Fig. 2.66, find the Thevenin equivalent as viewed by the resistance R. Find the value of R for maximum power dissipation in it and the value of this power.

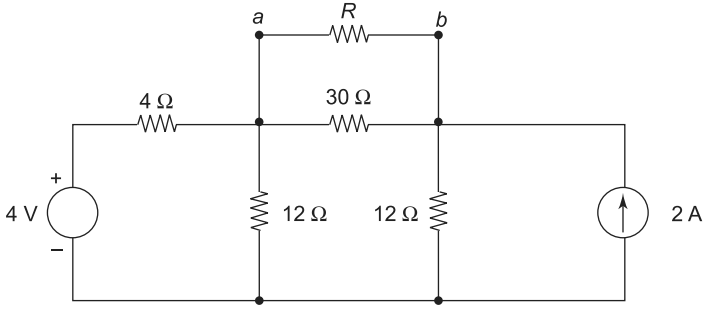


Fig. 2.66

18. Find the Thevenin equivalent of the circuit of Fig. 2.67 as seen at terminals *XY*.

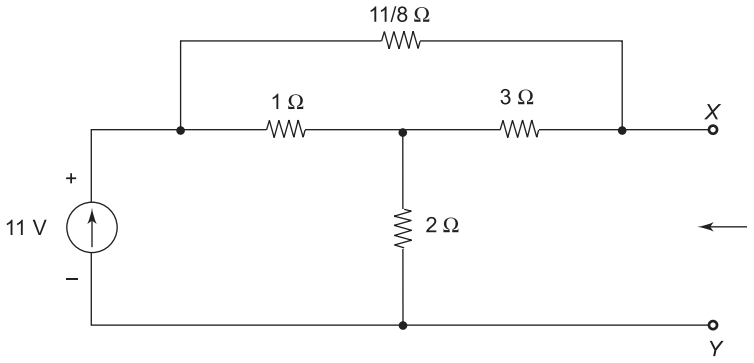


Fig. 2.67

19. In the circuit of Fig. 2.68, find the current I_1 using the principle of superposition.

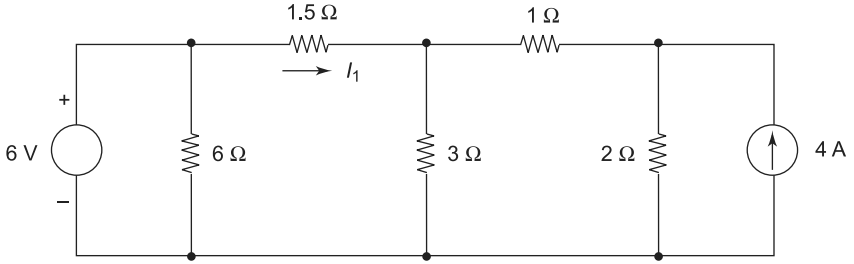


Fig. 2.68

20. Find the Thevenin equivalent of the circuit of Fig. 2.69 to the left of *XY*.

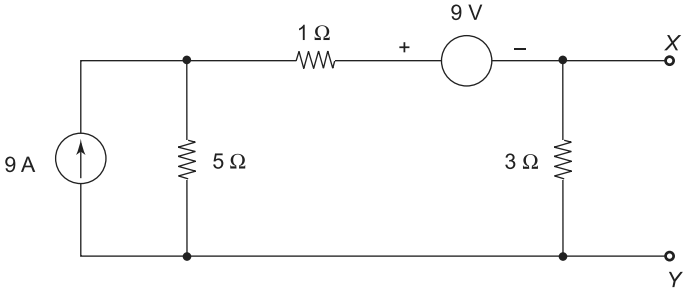


Fig. 2.69

Multiple-Choice Questions

1. In the circuit of Fig. 2.70, when $I = 1$ A, V_s is given by
   (a) 3 V (b) 4 V (c) 5 V (d) 7 V

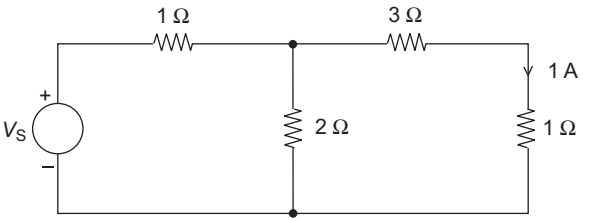


Fig. 2.70

2. For the circuit, the Thevenin voltage of resistance as seen at '*AB*' in Fig. 2.71 are
   (a) 5 V, 10 Ω (b) 10 V, 15 Ω (c) 10 V, 10 Ω (d) 5 V, 15 Ω

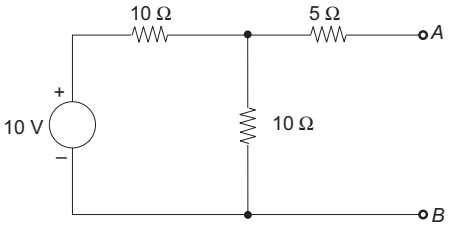


Fig. 2.71

3. The Thevenin/Norton equivalent of a network cannot be found if
   (a) it contains voltage source only
   (b) it contains current source only
   (c) it contains voltage/current sources but not dependent sources
   (d) even if it contains voltage/current sources and/or dependent source
4. In the circuit of Fig. 2.72, the value of I_S for $I = 0$ is
   (a) 4 A (b) 2 A (c) 2/5 A (d) 2/3 A

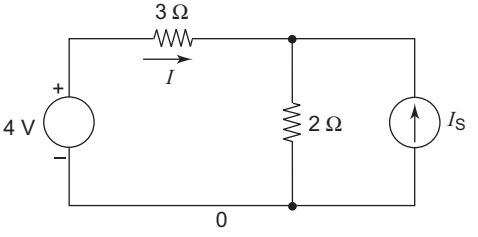


Fig. 2.72

5. For the circuit, the Thevenin voltage and resistance to the left of *AB* in Fig. 2.73 are
   (a) 2 V, 4 Ω (b) 4 V, 2 Ω (c) 2 V, 1 Ω (d) 4 V, 1 Ω

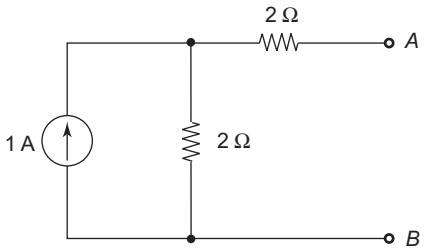


Fig. 2.73

6. Three resistances of value R ohms each are connected is star. Its equivalent delta will comprise three resistances of value
   (a) $R/3$ each (b) $3R$ each (c) R each (d) $3R, R, R/3$
7. The Thevenin voltage and resistance as seen at AB in Fig. 2.74 are as follows:

	Voltage	Resistance
(a)	4	0
(b)	4	∞
(c)	0	0
(d)	0	∞

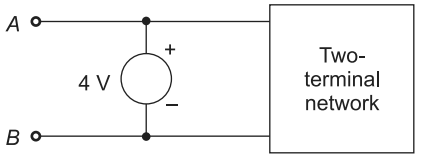


Fig. 2.74

8. Fort the circuit, the Norton equivalent as seen in Fig. 2.75 as from terminal AB is

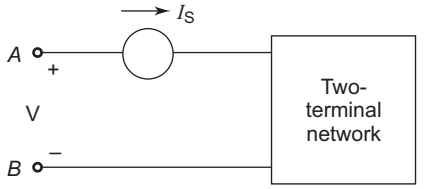


Fig. 2.75

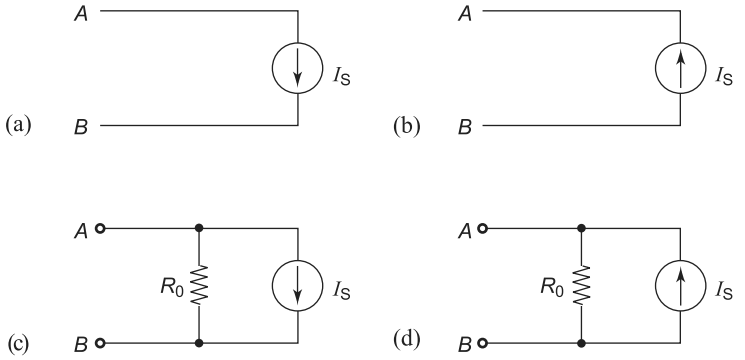


Fig. 2.76

9. The Norton equivalent of the circuit is drawn in Fig. 2.77; the values of I_{SC} and R_{eq} are

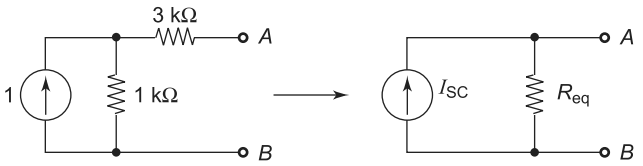


Fig. 2.77

10. In the circuit of Fig. 2.78, R_{eq} is given by
(a) 5 Ω (b) 2 Ω (c) 4 Ω (d) 6 Ω

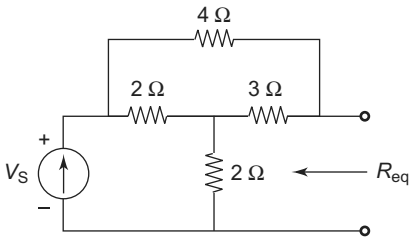


Fig. 2.78

11. In the resistive circuit of Fig. 2.79, V_s has a voltage of

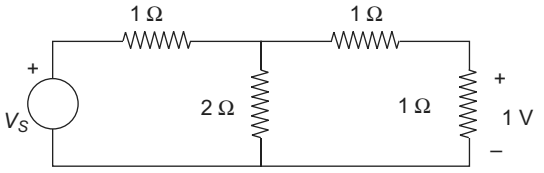


Fig. 2.79

(a) 8 V (b) 6 V (c) 4 V (d) 2 V

Answers

Multiple-Choice Questions

1. (d) 2. (a) 3. (d) 4. (b) 5. (a) 6. (b)
7. (a) 8. (a) 9. (b) 10. (b) 11. (d)

Steady-State Analysis for Sinusoidal Excitation

chapter 3

Goals & Objectives

- Concept of the phase difference of sinusoidal voltage/current
- Root mean square value (RMS)
- Phasor representation of sinusoidal qualities voltage/current
- Phasor diagram and computation thereof
- Concept of impedance/admittance complex quantities
- Power in sinusoidal steady state power factor watts (W)
- Application of modal and mesh analysis vars (VAR)
- Application of all network theorems, in phasor form
- Concept of resonance—series, parallels; quality factor half power frequencies, bandwidth

3.1 INTRODUCTION

So far we have studied the generalised techniques of nodal and mesh analysis of circuits along with certain theorems that help reduce the work involved in circuit analysis under special situations. The circuits studied were excited from dc (constant) sources.

In this chapter, we shall study the steady-state circuit behaviour to sinusoidal excitations. The powerful concept of phasor will be introduced and we shall discover that all the techniques of circuit analysis and theorems studied apply to phasor currents and voltages.

3.2 SINUSOIDAL FUNCTION

Waveform of sinusoidal function (voltage/current) was introduced in Chapter 1. Some of its attributes studied so far are summarised below.

- Waveform is periodic, repeats every time after period T (second) or after angle 2π. Periodicity is expressed as frequency f in Hz (cycles/second) or in angular frequency $\omega = 2\pi f$ rad/s.
- Sinusoidal waveform has half-wave and quarter-wave symmetries.
- Sinusoidal waveform has an associated phase, which depends upon the reference time selected.

3.2.1 Phase Difference

Consider two sinusoidal waveforms, one voltage and one current.

$$v = V_m \cos(\omega t + \alpha) \tag{3.1}$$

$$i = I_m \cos(\omega t + \beta) \tag{3.2}$$

where V_m and I_m are maximum or *peak* values of the respective voltage and current.

These waveforms are sketched in Fig. 3.1 with the assumption of $\beta < \alpha$. From this sketch, it is observed that, waveform of i is displaced in time (or angle) from that of v, i.e. v and i *differ in phase*. Positive peaks (or other corresponding instantaneous values) of i occur later than those of v by an angle $\theta = \alpha - \beta$. This fact is expressed by stating that i lags v by angle θ, or v leads i by angle θ. The situation could also be reversed.

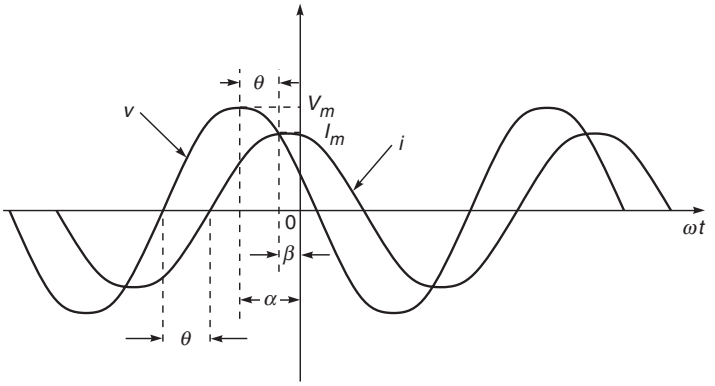


Fig. 3.1 *Sinusoidal current and voltage waveforms with a phase difference*

By shifting the reference time (angle), the waveforms of Eqs (3.1) and (3.2) could be expressed as

$$v = V_m \cos w_t \tag{3.3}$$

$$i = I_m \cos(w_t - \theta) \tag{3.4}$$

which also indicate the fact that i lags v by angle θ with the difference that v has a phase angle of zero. Such a waveform is known as a *reference*. It is convenient to use a reference waveform (voltage/current) with respect to which the phases of other voltages/currents in the circuit are expressed.

3.2.2 RMS (Effective) Value

The alternating voltage or current waveshape completes a certain number of cycles in one second, each cycle comprising an identical positive and negative half cycle. The value of the quantity varies from instant to instant, peaking at a certain instant only. In specifying a varying voltage or current, its maximum or peak value is normally not used. The *root mean square (rms)* value of the alternating voltage or current is often used in practice to specify the quantity. It is also called the *effective* or *virtual* value of the alternating quantity. During measurements, ammeters and voltmeters register only this quantity for all types of alternating voltage or current waves. The rms value also specifies the 'rating' of an electric motor for a varying duty cycle.

The general expression for calculation of rms value of a periodic wave is

$$I_{\text{eff}} = I_{\text{rms}} = \sqrt{\text{average } i^2(t)}$$

$$= \sqrt{\left(\frac{i_1^2 + i_2^2 + \cdots + I_n^2}{n}\right)}$$

= square root of the mean of the squares of the instantaneous currents over one cycle

The general expression for the average value of a current wave is

$$I_{\text{av}} = \frac{i_1 + i_2 + \cdots + i_n}{n}, \text{ over positive half cycle}$$

Instantaneous power dissipation in a resistance is

$$p = i^2 R$$

Average power dissipation over one cycle (time period T) is

$$P = \left(\frac{1}{T}\int_0^T i^2 R\,\mathrm{d}t\right)$$

$$= I^2 R \tag{3.5}$$

where $I = I_{(\text{rms})} = \left[\frac{1}{T}\int_0^T i^2\,\mathrm{d}t\right]^{1/2}$ root mean square (rms) current

Consider an alternating current (ac) of sinusoidal waveform.

$$i = I_m \cos w_t = I_m \cos \frac{2\pi}{T} t$$

$$I_{(\text{rms})} = \left[\left(\frac{1}{T}\int_0^T I_m^2 \cos^2 \frac{2\pi}{T} t\right) dt\right]^{1/2}$$

$$= \frac{I_m}{\sqrt{2}} \tag{3.6a}$$

$$I_{av} = 2\, I_m/t \text{ (average}^1 \text{ is taken over positive half cycle)} \tag{3.6b}$$

The *form factor* = I (rms)/I_{av}; indicative of any periodic waveform

$$= \pi/2\sqrt{2} = 1.11 \text{ for the sinusoidal current/voltage}$$

The *peak factor* = I_m/I (rms); indicative of any periodic waveform

$$= \sqrt{2} \text{ for the sinusoidal current/voltage}$$

This is also called *crest factor* or *amplitude factor*.

In fact, as per Eq. (3.5), an alternating current will deliver to a resistance the same power as a direct current of value equal to the rms (or *effective*) value of the alternating current.

The rms value of an alternating voltage is similarly defined and the average power delivered to a resistance would be

$$P = \frac{V^2}{R} \tag{3.7}$$

where $V = \dfrac{V_m}{\sqrt{2}}$; $v = V_m \cos \omega t$

Because of the average, power relationship of Eqs (3.5) and (3.7), it is customary to express the magnitude of alternating current/voltage in terms of rms value. An ac ammeter at voltmeter would read such a value.

In terms of rms values, the instantaneous current and voltage are expressed as

$$i = \sqrt{2}\, I \cos(\omega t + \alpha) \tag{3.8}$$

$$v = \sqrt{2}\, V \cos(\omega t + \beta) \tag{3.9}$$

Example 3.1

Controlled rectifiers are employed to convert ac to dc. The output of a controlled rectifier has waveform as shown in Fig. 3.2. Find (a) the average value, and (b) the rms value.

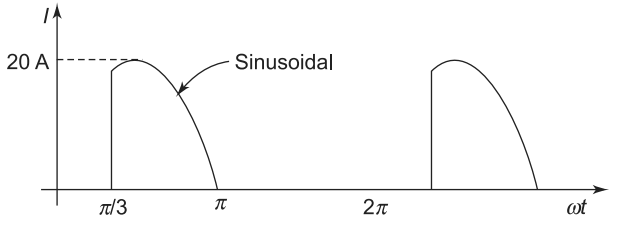


Fig. 3.2

Solution

(a) $$I_{av} = \frac{1}{2\pi} \int_{\pi/3}^{\pi} 20 \sin \omega t \, \mathrm{d}(\omega t)$$

$$= 3.775 \text{ A}$$

[1] The average of a sinusoidal current over one cycle is zero. The average over half positive cycle is meaningful when we deal with rectification of sinusoidal current.

(b) $$I_{\text{rms}} = \left[\frac{1}{2\pi}\int_{\pi/3}^{\pi} 20^2 \sin^2 \omega t \, \mathrm{d}(\omega t)\right]^{1/2}$$
$$= 8.97 \text{ A}$$

Example 3.2

Find the average value of the full-wave rectified sine wave shown in Fig. 3.3.

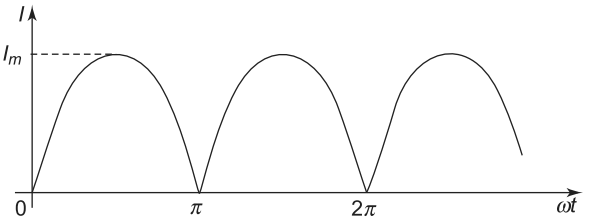


Fig. 3.3

Solution

$$i = I_m \sin \omega_t \; 0 < \omega_t < \pi$$
$$= -I_m \sin \omega t \; \pi < \omega t < 2\pi$$

$$I_{\text{av}} = \frac{1}{2\pi}\int_{\pi/3}^{\pi} I_m \sin \omega t \, \mathrm{d}(\omega t)$$

$$= \frac{I_m}{\pi} \tag{3.10}$$

3.2.3 Phasor Representation

Consider a sinusoidal waveform represented as

$$a = \sqrt{2} A \cos(\omega t + \theta) \tag{3.11}$$

where A = rms amplitude,
$\omega = 2\pi f$ rad/s (frequency),
θ = phase angle

Equation (3.11) can be written as[2]

$$a = \text{Re}[\sqrt{2}\, A e^{j\theta} e^{j\omega t}] \text{ ; Re means 'take the real part of'}$$

---

[2] If sine wave is used as a reference, say

$$a = \sqrt{2}\, A \sin(\omega t + \theta)$$

we can also write it as

$$a = \text{Im}\left[\sqrt{2}\, A e^{j\theta} e^{j\omega t}\right]\text{; where Im means 'take the imaginary part of'}$$

or $$a = \text{Im}[\bar{A} e^{j\omega t}]$$

where $$\bar{A} = A e^{j\theta} = A \angle \theta$$

Instantaneous value could now correspond to projection of phasor tip on the imaginary axis. We shall mostly employ cosine as reference.

or $$a = \text{Re}[\sqrt{2}\,\bar{A}\,e^{j\omega t}] \tag{3.12}$$

where $$\bar{A} = Ae^{j\theta} = A \angle \theta \tag{3.13}$$

The representation $\bar{A}$ [as in Eq. (3.13)] from which, sinusoidal waveform can be reconstructed as per operation of Eq. (3.12) (multiply by $\sqrt{2}\ e^{j\omega t}$ and take real part of) is known as a *phasor*. The expression $e^{j\omega t}$ imparts rotation to the phasor in the complex plane as shown in Fig. 3.4. The projection of the phasor tip on the real axis when multiplied by $\sqrt{2}$ yields the instantaneous value of the original sine wave.

When dealing with addition and subtraction operation of sine waves of the same frequency represented as phasors, it is immediately seen that these would remain fixed relative to each other so that the rotation idea can be kept in the background.

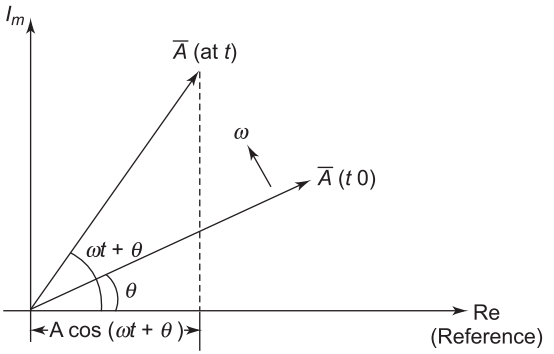


Fig. 3.4 *Phasor representation of sine wave*

Consider the addition of two waves

$$\sqrt{2}\,A_1\cos(\omega t + \theta_1) + \sqrt{2}A_2\cos(\omega t + \theta_2) = \sqrt{2}\,A\cos(\omega t + \theta) \tag{3.14}$$

In phasor form,

$$\bar{A}_1 e^{j\theta_1} + \bar{A}_2 e^{j\theta_2} = \bar{A}e^{j\theta} \tag{3.15}$$

or $$\bar{A}_1 + \bar{A}_2 = \bar{A} \tag{3.16}$$

This operation is shown in Fig. 3.5(a). Operation $\bar{A}_1 - \bar{A}_2$ is shown in Fig. 3.5(b).

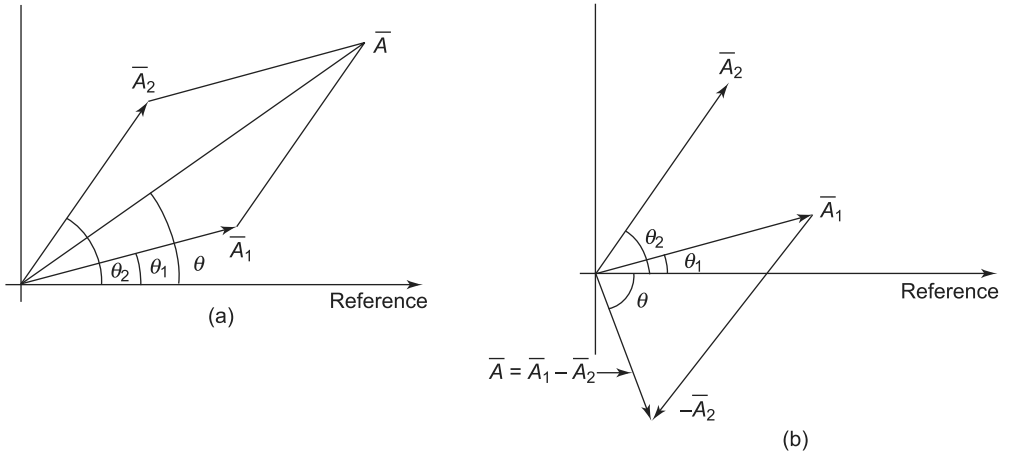


Fig. 3.5 *(a) Phasor addition (b) Phasor subtraction*

Example 3.3

Evaluate the expression below using the phasor method

$$e(t) = 100\sqrt{2}\ \cos(314t - 30^\circ) \pm 200\sqrt{2}\ \sin(314t - 60^\circ)$$

Solution

$$e(t) = 100\sqrt{2}\ \cos(314t - 30^\circ) + 200\sqrt{2}\cos(314t - 60^\circ)$$

$$= \sqrt{2}\,E\cos(314t + \theta)$$

We need to find E and θ. Representing the sine waves as phasors,

$$\bar{E} = 100\angle -30^\circ + 200\angle -60^\circ$$
$$= (86.6 - j50) + (100 - j173.2)$$
$$= 186.6 - j223.2$$
$$= 290.9\angle -50.1^\circ$$

Hence,

$$e(t) = 290.9\ \sqrt{2}\ \cos(314t - 50.1^\circ)$$

In the second case,

$$\bar{E} = 100\angle -30^\circ - 200\angle -60^\circ$$
$$= (86.6 - j50) - (100 - j1.73.2)$$
$$= -13.4 + 7123.2$$
$$= 123.9\angle 96.20^\circ$$

Hence, $e(t) = 123.9\sqrt{2}\cos(314\text{t} + 96.2^\circ)$

3.3 SINUSOIDAL STEADY-STATE ANALYSIS

As the derivative and integration of a sinusoid are also sinusoidal, the steady-state solution can be directly obtained from the differential equation of a circuit by substituting in it an assumed sinusoidal solution with unknown amplitude and phase. The amplitude and phase of the solution can then by determined by trigonometric combinations. The process through the straightforward way is quite cumbersome and becomes intractable even for any reasonably size network.

We shall study here the *phasor method* of steady-state sinusoidal circuit analysis, which in effect reduces the circuit differential equation to algebraic form (with complex numbers); which can be easily manipulated to obtain the desired solution.

We shall consider one by one the ideal circuit elements R, L, C excited by voltage

$$v(t) = \sqrt{2}\,V\cos(\omega t + \theta) \tag{3.17}$$

We can write

$$v(t) = \text{Re}\left[\sqrt{2}\,Ve^{j\theta}\,e^{j\omega t}\right], \text{ Re is 'real part of'} \tag{3.18}$$

Operator Re can be performed on the end result to write the excitation voltage or response current in time form, i.e. in time domain. Thus,

$$v(t) \xrightarrow{\text{transforms to}} \sqrt{2}\,V\,e^{j\theta}\,e^{j\omega t} = \sqrt{2}\,\bar{V}\,e^{j\omega t} \tag{3.19}$$

Time domain Frequency domain

where $\bar{V} = Ve^{j\theta}$; a phasor (3.20)

Consider now a resistance, excited by sinusoidal voltage as in Fig. 3.6(a).

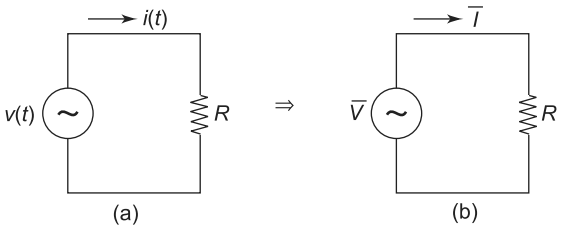


Fig. 3.6 *(a) In time domain (b) In frequency domain-phasor form*

In time domain,

$$v(t) = Ri(t) \tag{3.21a}$$

In frequency domain,

$$\bar{V}e^{j\omega t} = R\bar{I}e^{j\omega t}$$

or in phasor form, $\bar{V} = R\bar{I}$ (3.21b)

or $\bar{I} = G\bar{V}$ (3.21c)

Its graphical representation, called *phasor diagram*, is shown in Fig. 3.7 wherein it is obvious that $\bar{V}$ and $\bar{I}$ are in phase.

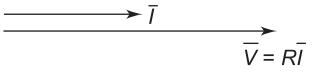


Fig. 3.7 $\bar{V}$–$\bar{I}$ *relationship for resistance*

Consider now a capacitance *excited* by sinusoidal voltage as in Fig 3.8(a).

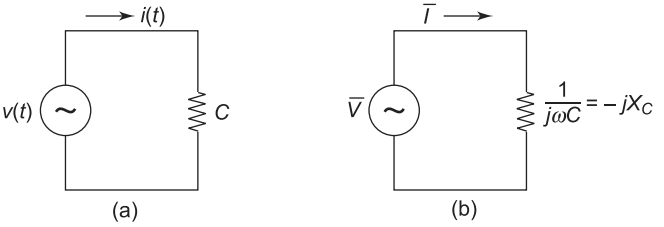


Fig. 3.8 *(a) In time domain (b) In frequency domain-phasor form*

$$v(t) = \frac{1}{C}\int i(t)dt \tag{3.22}$$

In frequency domain,

$$\bar{V}e^{j\omega t} = \frac{1}{C}\int \bar{I}e^{j\omega t}dt = \frac{1}{j\omega C}\bar{I}e^{j\omega t} \tag{3.23}$$

In phasor form,

$$\bar{V} = \frac{1}{j\omega C}\bar{I} = -j\frac{1}{\omega C}\bar{I} = -jX_C\bar{I} \tag{3.24}$$

where

$$X_C = \frac{1}{\omega C}\text{; } \textit{capacitive reactance } (\Omega) \tag{3.25}$$

Equation (3.24) is also expressed as

$$\bar{I} = j\omega C\bar{V} = jB_C\bar{V} \tag{3.26}$$

where $B_c = \omega C = \textit{capacitive susceptance}$ ($\mho$)

The phasor diagram of Eqs (3.24) and (3.26) are drawn in Fig. 3.9. Observe that $\bar{I}$ leads $\bar{V}$ by 90°. Consider now an inductance excited by sinusoidal voltage as in Fig. 3.10(a).

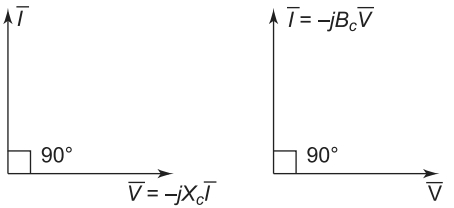


Fig. 3.9 *$\bar{V}$–$\bar{I}$ relationship for capacitance*

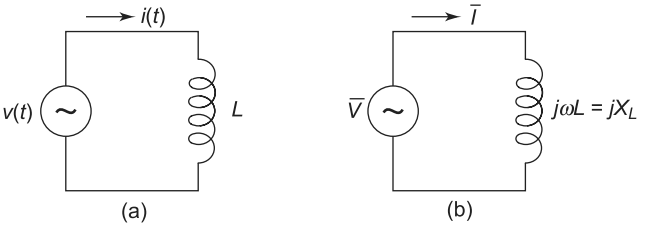


Fig. 3.10 *(a) In time domain (b) In frequency domain-phasor form*

In time domain,

$$v(t) = L\frac{\mathrm{d}i}{\mathrm{d}t}$$

In frequency domain,

$$\bar{V}e^{jwt} = L\frac{\mathrm{d}}{\mathrm{d}t}[\bar{I}e^{j\omega t}] = j\omega L\bar{I}\,e^{j\omega t} \tag{3.27}$$

In phasor form,

$$\bar{V} = j\omega L\bar{I} = jX_L I \tag{3.28}$$

where $X_L = \omega_L = 2\pi fL$; *inductive reactance* Ω (3.29)

In alternative form,

$$\bar{I} = \frac{1}{j\omega L}\bar{V} = -j\frac{1}{X_L}\bar{V} = -jB_L\bar{V} \tag{3.30}$$

where $B_L = \dfrac{1}{\omega L} = \dfrac{1}{X_L}$; *inductive susceptance* (℧) (3.31)

The phasor diagrams for Eqs (3.28) and (3.30) are drawn in Fig. 3.11.

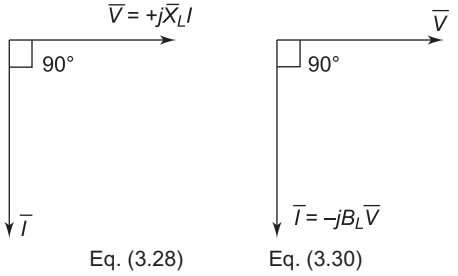
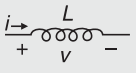
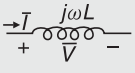
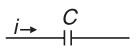
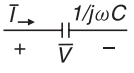


Fig. 3.11 *$\overline{V}$–$\overline{I}$ relationship for inductance*

For the three circuit elements, the time-domain *v–i* relationships and corresponding frequency domain $\overline{V} - \overline{I}$ relationships are summarised in Table 3.1.

Table 3.1 *Voltage-current relationships in time and frequency domains*

Time domain		*Frequency domain*	
	$v = Ri$	$\overline{V} = R\overline{I}$	
	$v = L\dfrac{di}{dt}$	$\overline{V} = j\omega L\overline{I}$	
	$v = \dfrac{1}{C}\int i\,dt$	$\overline{V} = \dfrac{1}{j\omega C} I$	

Consider now an *RLC* series circuit excited by sinusoidal voltage as shown in Fig. 3.12(a).

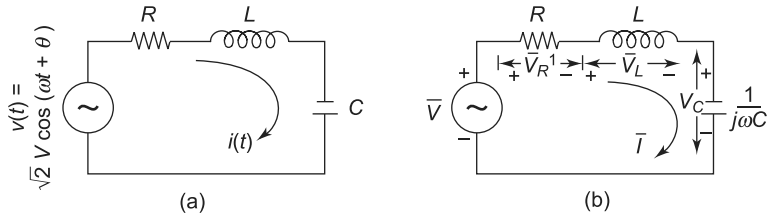


Fig. 3.12 *(a) In time domain (b) In frequency domain-phasor form*

Figure 3.12(a) is redrawn in phasor form (element by element) in Fig. 3.12(b). We can write the phasor equation of the circuit as

$$\overline{V} = \overline{V}_R + \overline{V}_L + \overline{V}_C$$

$$\overline{V} = R\overline{I} + j\omega L\overline{I} + \frac{1}{j\omega C}\overline{I} \tag{3.32}$$

or $$\bar{V} = (R + jX_L - jX_C)\bar{I}$$

or $$\bar{V} = [R + j(X_L - X_C)]\bar{I} \tag{3.33}$$

Let $$X = X_L - X_C$$

Then $$\bar{V} = (R + jX)\bar{I} \tag{3.34}$$

or $$\bar{V} = \bar{Z}\bar{I} \quad (\textit{Ohm's law} \text{ in phasor form}) \tag{3.35}$$

3.3.1 Impedance/Admittance

Define

$$\bar{Z} = R + jX = \textit{impedance} \text{ (complex number)} \tag{3.36a}$$

$$= Z \angle \theta \tag{3.36b}$$

where $$Z = \sqrt{R^2 + X^2}$$

$$\theta = \tan^{-1}\frac{X}{R}$$

The impedance triangle corresponding to Eq. (3.36a) is drawn in Fig. 3.13.

It must be observed here that *impedance is a complex number and not a phasor*.

Equation (3.35) can also be written as

$$\bar{I} = \bar{Y}\bar{V} \tag{3.37}$$

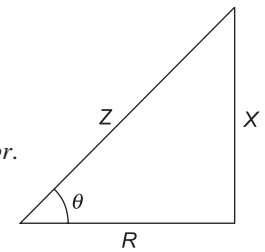


Fig. 3.13

where $$\bar{Y} = \frac{1}{\bar{Z}} = \textit{admittance } (\mho) \tag{3.38}$$

$$= \frac{1}{R + jX} = \frac{R}{R^2 + X^2} - j\frac{X}{R^2 + X^2}$$

$$= G - jB$$

where G = *conductance* and B = *susceptance*

The phasor diagram of the circuit of Fig. 3.12 is drawn in Fig. 3.14. This corresponds to KVL Eq. (3.33).

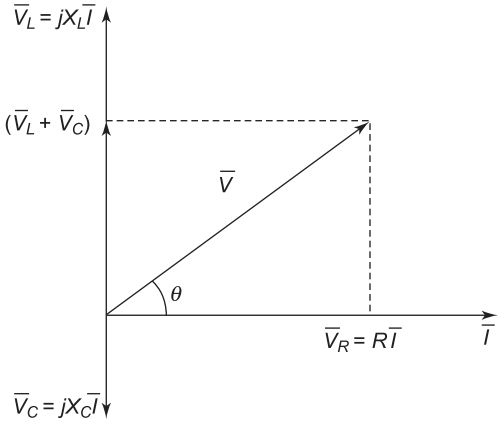


Fig. 3.14 *Phasor diagram of RLC series circuit of Fig. 3.12(b)*

3.3.2 Series/Parallel Combination of Impedances/Admittances

The same rules apply for resistances/conductances except that complex number computation is involved.

1. Impedances in Series

$$\bar{Z} = \bar{Z}_1 + \bar{Z}_2 + \cdots \text{(convenient form)} \tag{3.39}$$

or

$$\frac{1}{\bar{Y}} = \frac{1}{\bar{Y}_1} + \frac{1}{\bar{Y}_2} + \cdots \tag{3.40}$$

2. Admittances in Parallel

$$\bar{Y} = \bar{Y}_1 + \bar{Y}_2 + \cdots \text{ (convenient form)} \tag{3.41}$$

or

$$\frac{1}{\bar{Z}} = \frac{1}{\bar{Z}_1} + \frac{1}{\bar{Z}_2} + \cdots \tag{3.42}$$

KVL and KCL

Equation (3.32) is the KVL phasor equation for the circuit of Fig. 3.12. Similarly, KCL applies in phasor form.

Parallel RLC Circuit

Figure 3.15 shows a parallel *RLC* circuit with element values expressed in admittance form. Applying KCL at the single node,

$$\begin{aligned}\bar{I} &= \bar{I}_R + \bar{I}_L + \bar{I}_C \\ &= G\bar{V} - jB_L\bar{V} + jB_C\bar{V}\end{aligned} \tag{3.43}$$

The corresponding phasor diagram is drawn in Fig. 3.16. It follows that

$$\theta = \tan^{-1}\left(\frac{B_L - B_C}{G}\right)$$

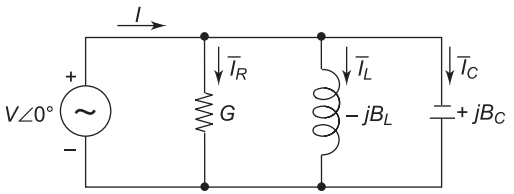


Fig. 3.15 *Parallel RLC circuit*

The current would lag voltage if $B_L > B_C$ and would lead if $B_C > B_L$, i.e. according to whether inductive susceptance or capacitive susceptance predominates.

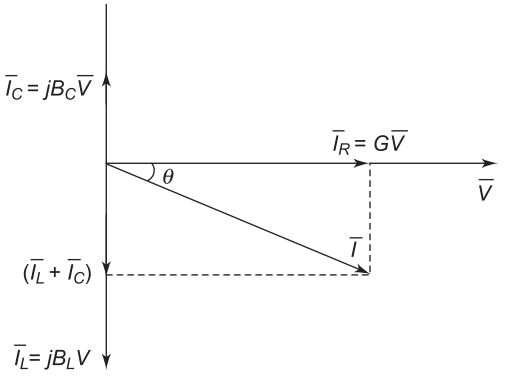


Fig. 3.16 *Phasor diagram of RLC parallel circuit*

Example 3.4

For the circuit of Fig. 3.17, $\bar{I} = 5 \angle 0^\circ$

(a) Find C if $\bar{V} = 100 + j200$ V, $\omega = 1.2$ k rad/s.

(b) Find C if $\omega = 200$ rad/s and $V = 100$ V.

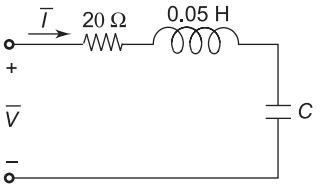


Fig. 3.17

Solution

(a) $\omega = 1.2\ k$ rad/s

$$X_L = 1200 \times 0.05 = 60\ \Omega$$

$$X_C = \frac{1}{1200C}$$

Now

$$\bar{Z} = \frac{\bar{V}}{\bar{I}}$$

$$20 + j60 - jX_C = \frac{100 + j200}{5 \angle 0^\circ}$$

$$= 20 + j40$$

or $$X_C = 20 = \frac{1}{1200C}$$

or $$C = \frac{1}{24000} = 41.67\ \mu\text{F}$$

(b) $\omega = 200$ rad/s

$$X_L = 200 \times 0.05 = 10\ \Omega$$

$V = 5$ Z (Ohm's law in magnitude form)

or $$100 = 5[(20)^2 + (10 - X_C)^2]^{1/2}$$

$$400 = 400 + (10 - X_C)^2$$

$$X_C = 10 = \frac{1}{200C}$$

or $$C = 500\ \mu\text{F}$$

Example 3.5

In the circuit of Fig. 3.18, find R and C. Given $V_b = 3\ V_a$ and V_b and V_a are in quadrature. Find also the phase relation between V, V_b, V_a and I.

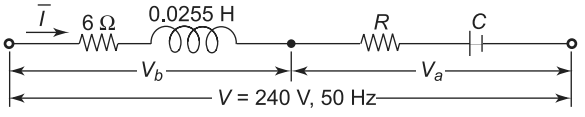


Fig. 3.18

Solution

$$X_L = \omega_L = 2\pi fL = 314 \times 0.0255 = 8\ \Omega$$

The frequency-domain circuit is drawn in Fig. 3.19. Since V_b and V_a are in quadrature,

$$V_a^2 + V_b^2 = V^2 = (240)^2$$

or $$V_a^2 + (3V_a)^2 = (240)^2$$

or $$V_a = 73.9\ \text{V}$$

or $$V_b = 227.7\ \text{V}$$

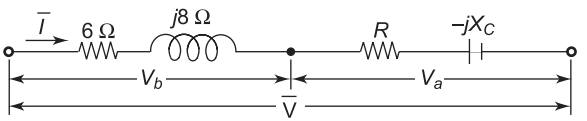


Fig. 3.19

Taking $\bar{I}$ as the reference phasor, the phasor diagram is drawn in Fig. 3.20.

$$\theta_1 = \tan^{-1} 8/6 = 53.1°$$

$$\theta_2 = 90° - 53.1° = 36.9°$$

Also, $$(6I)^2 + (8I)^2 = (227.7)^2$$

or $$I = 22.8\ \text{A}$$

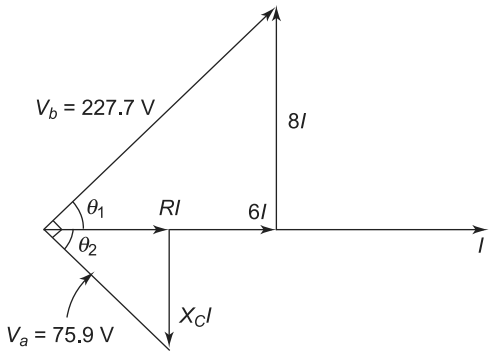


Fig. 3.20

For the *RC* part of the circuit,

$$\frac{X_C}{R} = \tan\theta_2 = \tan 36.9° = 0.75 \quad \text{(i)}$$

Also $$\sqrt{[R^2 + X_C^2]} \times 22.8 = 73.9$$

or $$R^2 + X^2{}_C = \left(\frac{75.9}{22.8}\right)^2 = 11.09 \quad \text{(ii)}$$

Solving Eqs (i) and (ii),

$$R^2 + (0.75)^2 R^2 = 11.09$$

or $$R = 2.664\ \Omega,$$

$$X_C = 2.664 \times 0.75 = \frac{1}{314C}$$

or $$C = 1.594\ \text{mF}$$

Example 3.6

Two circuits with impedances of $\bar{Z}_1 = 10 + j15\ \Omega$ and $\bar{Z}_2 = 6 - j8\ \Omega$ respectively are connected in parallel. If the total current supplied is 15 A; find each branch current and their phase angle w.r.t. the total current. What is the voltage across the combination and its phase angle?

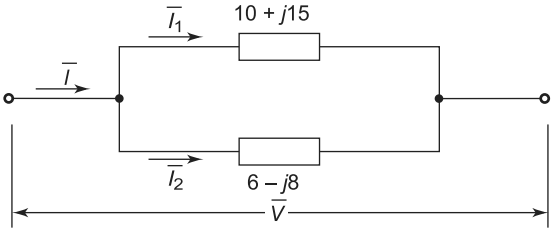


Fig. 3.21

Solution

$$\bar{I} = 15\angle 0°$$

The current will divide in the inverse ratio of the branch impedances.

$$\bar{I}_1 = 15 \angle 0° \times \frac{(6 - j8)}{(10 + j15) + (6 - j8)}$$

$$= 15 \times \frac{(6 - j8)}{(16 + j7)}$$

$$= 15 \times \frac{10 \angle -53.1°}{17.46 \angle 23.6°}$$

$$= 8.59 \angle -76.7° \text{A}$$

$$\bar{I}_2 = 15 \angle 0° \times \frac{(10 + j15)}{(16 + j7)}$$

$$= 15 \times \frac{18.03 \angle 56.3°}{17.46 \angle 23.6°}$$

$$= 15.49 \angle 32.7° \text{A}$$

$$\bar{V} = (10 + j15) \times 8.59 \angle -76.7°$$

$$= 18.03 \angle 56.3° \times 8.59 \angle -76.7°$$

$$= 154.9 \angle -20.4 V$$

The phasor diagram showing $\bar{I} = \bar{I}_1 + \bar{I}_2$ and $\bar{V}$ is drawn in Fig. 3.22.

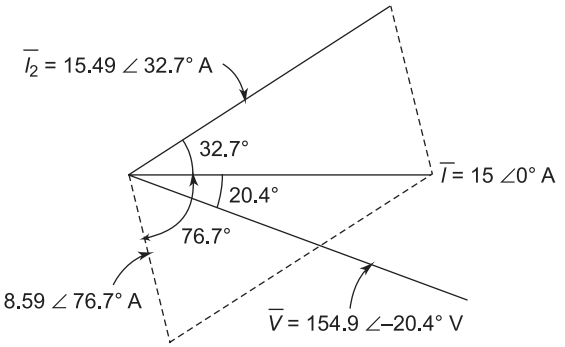


Fig. 3.22

Example 3.7

For the circuit of Fig. 3.23, find $\bar{Z}_{in}$ (input impedance or *driving point* impedance) with

(a) *AB* open-circuited,

(b) *AB* short-circuited, and

(c) *AB* connected through the 10 Ω resistance.

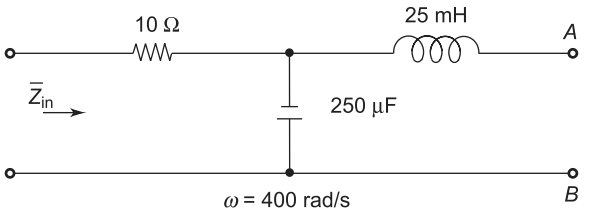


Fig. 3.23

Solution

$$X_L = 400 \times 25 \times 10^{-3} = 10\ \Omega$$

$$X_C = \frac{10^6}{400 \times 250} = 10\ \Omega$$

(a) *AB* open-circuited (Fig. 3.24)

$$\bar{Z}_{in} = (10 - j10) = 13.14\ \angle -45°\ \Omega$$

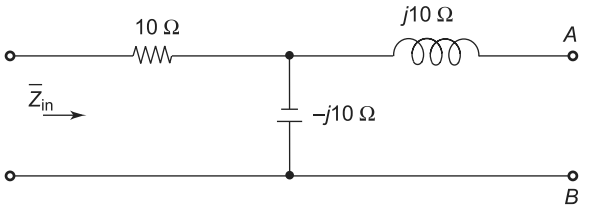


Fig. 3.24

(b) *AB* short-circuited (Fig. 3.25)

$$\bar{Z}_{in} = 10 + \frac{j10 \times -j10}{j10 - j10} = 10 + j\infty = \infty \angle 90°$$

(c) *AB* connected through the 10 Ω resistance (Fig. 3.26)

$$\bar{Z}_{in} = 10 + \frac{(10 + j10) \cdot (-j10)}{10 + j10 - j10}$$

$$= 20 - j10 = 22.36\ \angle -26.6°$$

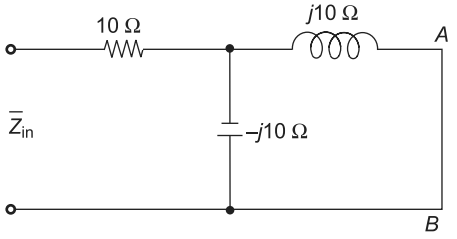


Fig. 3.25

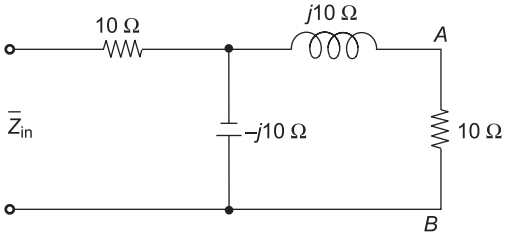


Fig. 3.26

Example 3.8

In the parallel circuit of Fig. 3.27, find

(a) $\bar{I}$ if $\bar{I}_R = 0.02 \angle 30°$ A, and

(b) $\bar{I}_R$ if $\bar{I} = 2 \angle 40°$; also find the applied voltage.

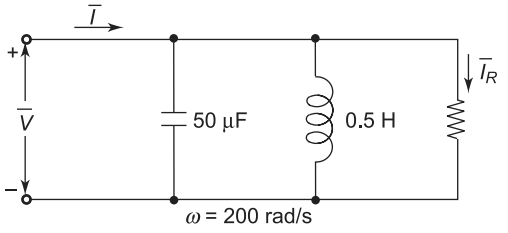


Fig. 3.27

Solution

(a) $\bar{I}_R = 0.02 \angle 30°$ A

$\bar{V}$ (applied voltage) $= 200 \times 0.02 \angle 30° = 4 \angle 30°$ V

$$\bar{I}_L = \frac{4 \angle 30° \text{ V}}{j200 \times 0.5} = 0.04 \angle -60° \text{ A}$$

$$\bar{I}_C = \frac{\dfrac{4 \angle 30°}{10^6}}{j200 \times 50} = 0.04 \angle -120° \text{ A}$$

$$\bar{I} = \bar{I}_R + \bar{I}_L + \bar{I}_C$$

$$= 0.02 \angle 30° + 0.04 \angle -60° + 0.04 \angle 120°$$

$$= (0.0173 + j0.01) + (0.02 - j0.0346) + (-0.02 + j0.0346)$$

$$= (0.0173 + j0.01) = 0.02 \angle 30° \text{ A}$$

The phasor diagram showing currents in the three elements, total current and applied voltage is drawn in Fig. 3.28. Observe that $\bar{I}_L$ and $\bar{I}_C$ cancel out so that $\bar{I} = \bar{I}_R$.

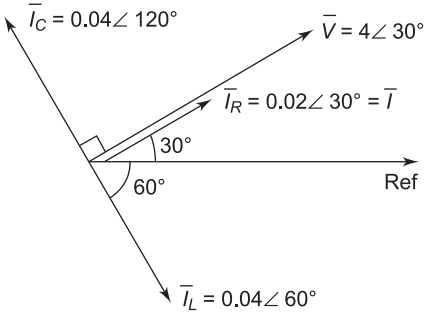


Fig. 3.28

(b) $$\frac{1}{Z_{in}} = \frac{1}{200} + \frac{L}{j200 \times 0.5} + \frac{1}{\frac{106}{j200 \times 50}}$$

$$= 0.005 - j0.01 + j0.01 = 0.005$$

or $$Z_{in} = 200\ \Omega,$$

$$\bar{V} = 200 \times 2 \angle -40° = 400 \angle -40° \text{A}$$

$$\frac{\bar{I}}{R} = \frac{400 \angle -40°}{200} = 2 \angle -40° \text{A}$$

3.4 POWER IN SINUSOIDAL STEADY STATE

Figure 3.29 shows an ac source (*single phase*) supplying a load of impedance $Z \angle \theta$. Then in instantaneous form,

$$v = \sqrt{2}\, V \sin \omega t$$

$$i = \sqrt{2}\, I \sin(\omega t - \theta)$$

where $I = V/Z$

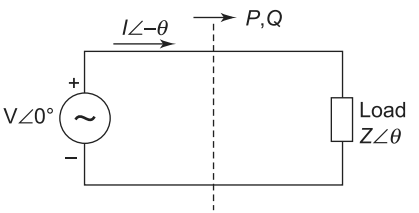


Fig. 3.29

The instantaneous power delivered to the load (or supplied by the source) is given by

$$p = vi = 2VI \sin \omega t \sin(\omega t - \theta)$$

$$= VI[\cos \theta - \cos(2\omega t - \theta)] \quad (3.44a)$$

The above equation can be written in the form

$$p = V[I \cos \theta (1 - \cos 2\omega t) + I \sin \theta \sin 2\omega t] \quad (3.44b)$$

The above equation identifies two components of current, which are marked on the phasor diagram of Fig. 3.31(a).

- $I \cos \theta$; current component in *phase* with voltage, and
- $I \sin \theta$; current component in *quadrature* (at 90°) to voltage.

The in-phase component $I \cos \theta$ is feeding *real* (or *active*) average power to load given by

$$P = VI \cos \theta\ W \quad (3.45a)$$

3.4.1 Power Factor

$\cos \theta$ is defined as the power factor abbreviated as pf. Real power can then be expressed as

$$P = VI \times \text{pf} \quad (3.45b)$$

$S = VI$, the volt-amperes fed to the load is called *apparent power*. We can then write

$$\text{pf} = \frac{P}{VI} \frac{\text{real power}}{\text{apparent power}} \quad (3.45c)$$

pf is lagging when $\bar{I}$ lags $\bar{V}$ and leading when $\bar{I}$ leads $\bar{V}$.

It is seen from Eq. 3.44(b) that $I \cos \theta$ has associated with it any oscillating component of power of frequency 2ω (twice the excitation frequency) with zero average value.

The quadrature component of current $I \sin \theta$ as per Eq. 3.44(b) feeds only oscillating power (frequency 2ω) to the load with zero average value. It is the *reactive power*.

$$Q = VI \sin \theta \text{ VAR} \tag{3.46}$$

the units being VAR, volt-ampere reactive.

The waveforms of $v(t)$, $i(t)$ and instantaneous power $p = vi$ are sketched in Fig. 3.30. The average real power is indicated by constant value P. It is easy to observe the total oscillating component of power having frequency 2ω.

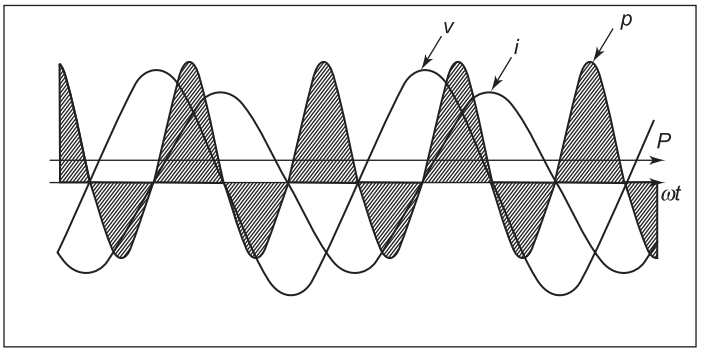


Fig. 3.30

Reactive power will be taken as *positive* for *lagging* and *negative* for *leading pf* (power factor) load. The complex power phasor diagram is drawn in Fig. 3.31(b) wherein

$$\overline{S} = P + jQ$$

Units for S are VA. Compare the complex power phasor diagram of Fig. 3.31(b) with the voltage and current phasor diagram of Fig. 3.31(a).

For large powers, unit for active power are kW/MW and those for reactive power are kVAR/MVAR and the complex power has the units of kVA/MVA.

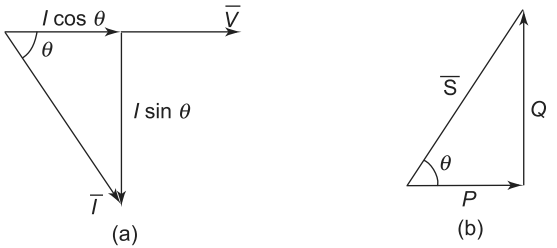


Fig. 3.31 *(a) In-phase and quadrature current components (b) Complex power*

3.4.2 Complex Power

It is convenient to express power in complex form:

$$\overline{S} = \overline{V}\,\overline{I}^{*} \tag{3.47}$$

Let $\overline{V} = Ve^{j0}, \overline{I} = Ie^{j(0-\theta)}$; $\overline{I}$ lags $\overline{V}$ by θ

Then
$$\overline{S} = Ve^{j0}\, Ie^{-j(0-\theta)}$$
$$= VI\, e^{j\theta} = VI \cos \theta + j\, VI \sin \theta \tag{3.48}$$
$$= P + jQ \tag{3.49}$$

It may be seen that Q is positive for lagging pf.

The phasor diagram of complex power corresponding to Eq. (3.49) is drawn in Fig. 3.31(b) wherein θ is reversed w.r.t. that of Fig. 3.31(a) because of conjugating of current in Eq. (3.47). It follows from the phasor diagram (or Eq. (3.49)) that

$$S = \sqrt{P^2 + Q^2}\ VA \tag{3.50}$$

and $\text{pf} = \cos\theta = \cos\tan^{-1} Q/P$; lagging for positive Q,

leading for negative Q (3.51)

For a series RL circuit (Fig. 3.32),

$$\bar{S} = \bar{V}\,\bar{I}^*$$

$$\bar{Z}\,\bar{I}\,\bar{I}^* = \bar{Z}\,\bar{I}^2$$

$$= (R + jX_L)I^2 = RI^2 + jX_L I^2 \tag{3.52}$$

Hence,

$P = RI^2$ = real power consumed in resistive element

$Q = X_L I^2$ = reactive power consumed in reactive (inductive) element

Analysing circuit in terms of complex powers is known as the *volt-ampere method* (Example 3.11).

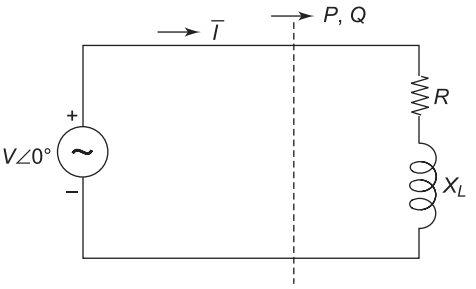


Fig. 3.32 *Series RL circuit*

Example 3.9

For the circuit of Fig. 3.33, $v_s(t) = \cos \omega t$

Find

(a) the *driving point admittance* $\bar{Y}(j\omega)$, and

(b) the value of the frequency at which the pf of the circuit would be unity.

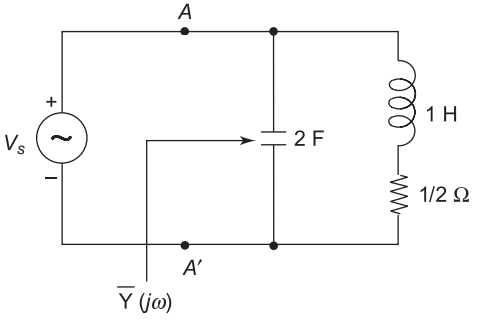


Fig. 3.33

Solution

(a) $$\bar{Y}(j\omega) = \frac{1}{\frac{1}{2} + j\omega} + 2\omega$$

(b) $\bar{I} = \bar{Y}(j\omega)V_s \angle 0°$

For unity power factor, the imaginary part of $\bar{Y}(j\omega)$ should be zero

$$\bar{Y}(j\omega) = \frac{\frac{1}{2} - j\omega}{\frac{1}{4} + \omega^2} + j2\omega$$

$$= \frac{2}{1+4\omega^2} - j\left[\frac{4\omega}{1+4\omega^2} - 2\omega\right]$$

$$\therefore \quad \frac{4\omega}{1+4\omega^2} = 2\omega$$

$$2 = 1 + 4\omega^2$$

$$\omega = \frac{1}{2}\text{rad/s}$$

Example 3.10

Find the average power fed to the circuit of Fig. 3.34 by the current source and the power factor.

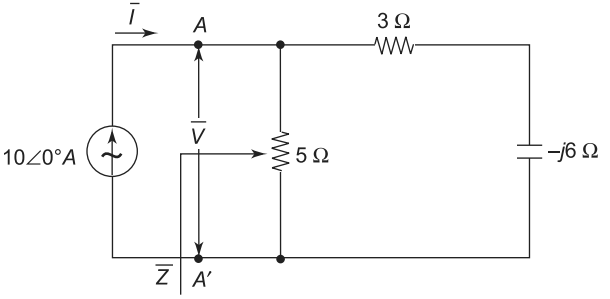


Fig. 3.34

Solution Driving point impedance

$$\bar{Z} = \frac{5 \times (3 - j6)}{5 + 3 - j6}$$

$$= \frac{5 \times (3 - j6)}{8 - j6} = 5\frac{(3 - j6)(8 + j6)}{100}$$

$$= \frac{60 - j30}{20} = 3 - j1.5$$

$$\bar{V} = (3 - j1.5) \times 10 \angle 0°$$

$$= 10(3 - j1.5) = 33.54 \angle -26.6° \text{ V}$$

I loads V by 26.6°. Therefore

$$P = 33.54 \times 10 \times 0.894 = 300 \text{ W}$$

$$p_f = \cos 26.6° = 0.894 \text{ loading}$$

3.4.3 Power Factor Improvement

Most electric loads are reactive in nature and have lagging power factor less than unity. Particularly, the industrial loads (with induction motor drives) have low pf, which may even be less than 0.8 if motors are not fully loaded. Transmission lines, transformers and generators of the electric power utility have to carry the lagging reactive power of the load so that their full real power capability is not exploited and further reactive current causes additional ohmic losses and large voltage drops. These factors cause operational financial loss to the utility. The utility, therefore, induces its industrial consumers to improve their power factor by imposing penalty through tariff for the reactive component of the consumer's load.

Industrial consumers thus find it economical to improve the pf of their individual motors and/or the total installation by installing shunt capacitors (static) which draw compensating leading current. The limit to which the pf must be improved is dictated by the balance of the yearly tariff saving against the yearly interest and depreciation cost of installing the capacitors. While these details are beyond the scope of this text, the effectiveness of shunt capacitors in pf improvement is illustrated in the Example 3.11.

Example 3.11

A 10 kVA load at 0.8 pf lagging is fed from 231 V, 50 Hz supply. Calculate the kVA capacity and the capacitance value of the shunt capacitor required to improve the overall pf (load + shunt capacitor) to 0.95 lagging. Compare the current drawn from the supply before and after installing the capacitors.

Solution Figure 3.35 shows the capacitor in parallel (shunt) to the load.

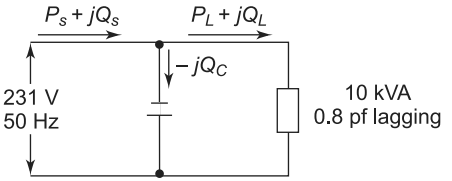


Fig. 3.35 *P_F improvement by shunt capacitor*

Load: $P_L + jQ_L = 10 \times 0.8 + j10 \times \sin \cos^{-1} 0.8$

$= 8 + j6$

Capacitor draws $= -jQ_C$ kVAR

Supply: $P_s + jQ_s = (8 + j6) - jQ_c$

New $p_f = \cos \tan^{-1} \dfrac{6 - Q_c}{8} = 0.95$ lagging

$\therefore$ $Q_c = 3.37$ kVAR

$$3.37 = \frac{(231)^2 \times 314 \times C}{1000}$$

or $C = 201$ μF

Supply current before pf improvement

$$10 = \frac{231 \times I_s}{1000}$$

or $I_S = I_L = 43.29$ A

Supply current after pf improvement

$$P_s + jQs = 8 + j(6 - 3.37) = 8 + j2.63 = 8.42 \angle 18.2°$$

$$I_S = \frac{8.42 \times 1000}{231} = 36.45 \text{ A}$$

Alternatively,

$$\bar{I}_L = 43.29 \times 0.8 - j43.29 \times 0.6 = 33.63 - 723.97 \text{ A}$$

$$\bar{I}_C = j\frac{3.37 \times 1000}{231} = j13.59 \text{ A}$$

$$\bar{I}_S = \bar{I}_L + \bar{I}_C = 33.63 - j(23.97 - 13.59) = 33.63 - j11.38$$

or $$I_s = 36.45 \text{ A}$$

It is seen that because of power-factor improvement, the current drawn from the supply reduces from 43.29 A to 36.43 A. This benefits the supplier as the line is real. Reactive power loss reduces as real power is $I_L^2 R_L$ and reactive loss is $I_L^2 X_L$.

3.5 NODAL AND MESH METHODS OF ANALYSIS

Nodal and mesh methods of analysis equally apply to sinusoidal steady-state analysis by converting the circuit into its frequency-domain equivalent—elements as impedances (admittances) in complex number form and source voltages/currents as phasors. These methods are best illustrated by examples.

Example 3.12

Figure 3.36 is the frequency-domain representation of a circuit. Determine the values (magnitude and angle) of the phasor voltages $\bar{V}_1$ and $\bar{V}_2$.

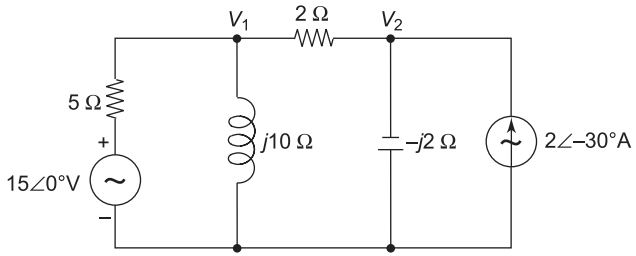


Fig. 3.36

Solution Converting the voltage source ($15 \angle 0°$) to current-source form, the circuit form changes to that in Fig. 3.37. Observe that all elemental values are in impedance form. Applying KCL at the two nodes:

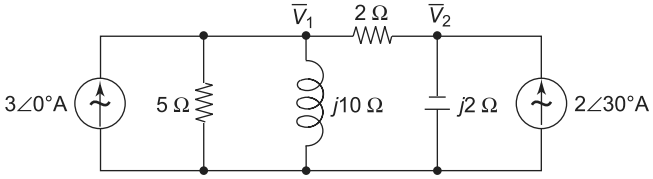


Fig. 3.37

Node 1: $$\frac{\bar{V}_1}{5}+\frac{\bar{V}_1}{j10}+\frac{\bar{V}_1-\bar{V}_2}{2}=3$$

or $$(0.7-j0.1)\,\bar{V}_1-0.5\bar{V}_2=3 \quad \text{(i)}$$

Node 2: $$\frac{\bar{V}_2}{-j^2}+\frac{\bar{V}_2-\bar{V}_1}{2}=2\angle -30°$$

or $$-0.5\bar{V}_1+(0.5+j0.5)\bar{V}_2=2\angle -30°=(1.732-j1) \quad \text{(ii)}$$

Let us now solve simultaneously Eqs (i) and (ii).

$$\Delta=\begin{vmatrix}(0.7-j0.1) & -0.5\\ -0.5 & (0.5+j0.5)\end{vmatrix}=(0.15+j0.3)=0.335\angle 63.4°$$

$$\Delta_1=\begin{vmatrix}3 & -0.5\\ (1.732-j1) & (0.5+j0.5)\end{vmatrix}=(2.366+j1)=2.569\angle 22.9°$$

$$\Delta_2=\begin{vmatrix}(0.7-j0.01) & 3\\ -0.5 & (1.732-j1)\end{vmatrix}2.613+j0.873=2.754\angle -18.5°$$

$$\bar{V}_1=\frac{\Delta_1}{\Delta}=\frac{2.569\angle 22.9°}{0.335\angle 63.4°}=7.669\angle -40.5°\,\text{V}$$

$$\bar{V}_2=\frac{\Delta_2}{\Delta}=\frac{2.754\angle 18.5°}{0.335\angle 63.4°}=8.221\angle -81.9°\,\text{V}$$

Currents in all the components can now be calculated; it is assumed above that both sources have the same frequency. It is only then that these can be represented as phasors with fixed phase difference (15 ∠ 0° V and 2 ∠–30°A).

Example 3.13

Draw the frequency-domain equivalent of the circuit of Fig. 3.38 at ω = 600 rad/s. Using the mesh method of analysis, find $\bar{V}_R$, i.e. phasor voltage across resistance and its time-domain expression.

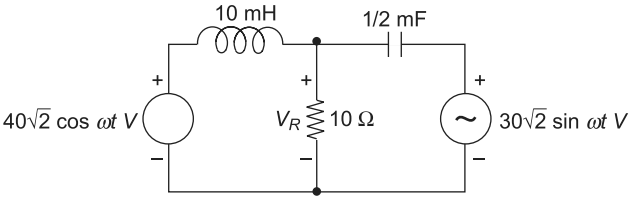


Fig. 3.38

Solution

$$X_L=\omega L=600\times 10\times 10^{-3}=6\ \Omega$$

$$X_C=\frac{1}{\omega C}=\frac{12\times 10^3}{600}=20\ \Omega$$

$$40\sqrt{2}\cos\omega t = \text{Re}[\sqrt{2}\times 40 e^{j0} e^{j\omega t}]$$

or $$\bar{V}_1 = 40\angle 0° \text{ V}$$

$$30\sqrt{2}\sin\omega t = 30\sqrt{2}\cos(\omega t - 90°) = \text{Re}[\sqrt{2}\times 30 e^{-j90°} e^{j\omega t}]$$

or $$\bar{V}_2 = 30\angle -90°$$

The frequency-domain equivalent of the circuit is drawn in Fig. 3.39. Writing down mesh equations,

$$j6\bar{I}_1 + 10(\bar{I}_1 - \bar{I}_2) = 40 \quad \text{(i)}$$

$$-j20\bar{I}_2 + 10(\bar{I}_2 - \bar{I}_1) = -j30 \quad \text{(ii)}$$

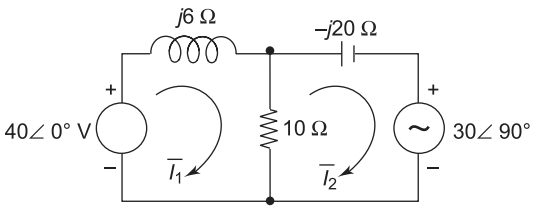


Fig. 3.39

Rearranging,

$$(10 + j6)\bar{I}_1 - 10\bar{I}_2 = 40 \quad \text{(iii)}$$

$$-10\bar{I}_1 + (10 - j20)\, I_2 = -j30 \quad \text{(iv)}$$

Solving Eqs (iii) and (iv) simultaneously,

$$\Delta = \begin{vmatrix} 10 + j6 & -10 \\ -10 & (10 - j20) \end{vmatrix} = 120 - j140 = 184.4\angle -49.4°$$

$$\Delta_1 = \begin{vmatrix} 40 & -10 \\ -j30 & (10 - j20) \end{vmatrix} = 400 - j1100 = 1170.5\angle -70°$$

$$\Delta_2 = \begin{vmatrix} (10 + j6) & 40 \\ -10 & -j30 \end{vmatrix} = 580 - j300 = 653\angle -27.3°$$

Now, $$\bar{I}_1 = \frac{\Delta_1}{\Delta} = \frac{1170.5\angle -70°}{184.4\angle -49.4°} = 6.35\angle -20.6° = 5.94\angle -j2.23\,\text{A}$$

$$\bar{I}_2 = \frac{\Delta_2}{\Delta} = \frac{653\angle -27.3°}{184.4\angle -49.4°} = 3.54\angle -22.1° = 3.28 + j1.33\text{ A}$$

Current through resistance = $\bar{I}_1 - \bar{I}_2$

$$= (3.94 - j2.23) - (3.28 + j1.33)$$

$$= 9.22 - j3.56 = 9.88\angle -21.1°\text{ A}$$

$$\bar{V}_R = 10\times 9.88\angle -22.1° = 91.54 - j3.72$$

$$v_R = 98.8\sqrt{2}\cos(600t - 22.1°)\text{ V}$$

3.6 NETWORK THEOREMS

All the network theorems advanced in Section 2.10 apply to frequency-domain circuits with phasor currents/voltages and complex number impedances/admittances. These theorems are Superposition Theorem, and the Thevenin and Norton theorems.

Maximum Power Transfer Theorem

The theorem is presented without proof (proof is not hard to establish). Consider a network represented by its Thevenin equivalent loaded at its terminals *AB* with load impedance $\overline{Z}_L = R_L + jX_L$ as shown in Fig. 3.40. Maximum power is transferred (absorbed) by the load if

$$X_L = -X_{\text{TH}}$$

$$R_L = R_{\text{TH}}$$

or $$\overline{Z}_L = \overline{Z}^*_{\text{TH}} \quad \text{*means complex conjugate of} \tag{3.53}$$

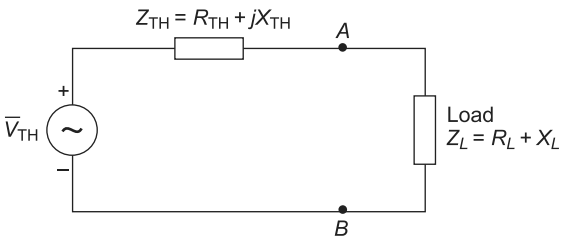


Fig. 3.40 *Maximum power transfer*

This technique of transferring maximum power to load is known as *impedance matching* and is of considerable importance in electronic circuits where output power is the chief concern though the power transfer efficiency is reduced to 50%. On the other hand, efficiency is of paramount importance in power circuits, which operate far from the condition of impedance matching.

Example 3.14

For the circuit of Fig. 3.41, find the values of R_L and X_L for maximum power absorption and the value of the maximum power.

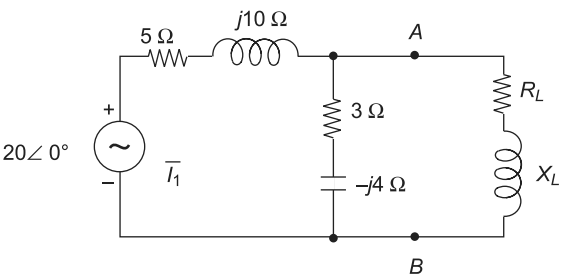


Fig. 3.41

Solution To begin with, we find the Thevenin equivalent of the circuit to the left of *AB,* which is redrawn in Fig. 3.42.

$$\bar{V}_{TH} = 20\angle 0° \times \frac{3 - j4}{(5 + j10) + (3 - j4)} = 10\angle -90° \text{ V}$$

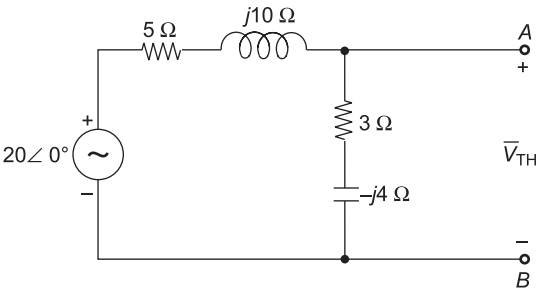


Fig. 3.42

Short-circuiting the voltage source as in Fig. 3.43,

$$\bar{Z}_{TH} = \frac{(5 + j10)(3 - j4)}{(8 + j6)} = \left(\frac{55 + j10}{8 + j6}\right) = 5 - j2.5\ \Omega$$

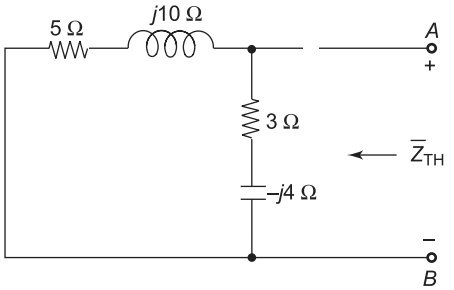


Fig. 3.43

By the maximum power transfer theorem,

$$\bar{Z}_L = 5 + j2.5\ \Omega$$

Example 3.15

For the series circuit of Fig. 3.44, with the current and voltage indicated, find the values of *R*, *r*, *L* and the frequency of the applied voltage and its magnitude.

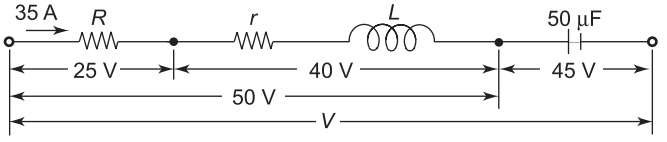


Fig. 3.44

Solution

$$45/X_c = 35 \text{ A or } X_c = 1.286 = 10^6/(\omega \times 50)$$

$$\therefore \quad f = 10^6/(1.286 \times 2\pi \times 50)$$

$$= 2.475 \text{ kHz}$$

The voltage phasor triangle is drawn in Fig. 3.45(a).

$$\cos\theta = [(25)^2 + (50)^2 - (40)^2]/(2 \times 25 \times 50)$$

$$= 0.61$$

or $\theta = 52.4°$

$$x = 50 \cos 52.4° - 25 = 5.5 \text{ V}$$

$$y = 50 \sin 52.4° = 39.61 \text{ V}$$

From the circuit diagram of Fig. 3.44, we have

$$35 \times r = 3.5$$

or $r = 0.157\ \Omega$.

and $35 \times (2\pi \times 2475\ L) = 39.61$

or $L = 0.073$ mH

The complete phasor diagram is drawn in Fig. 3.45(b), from which

$$V \text{ (applied)} = [(25 + 5.5)^2 + (5.39)^2]^{0.5} = 51 \text{ V}$$

$$R = 25/35 = 0.714\ \Omega$$

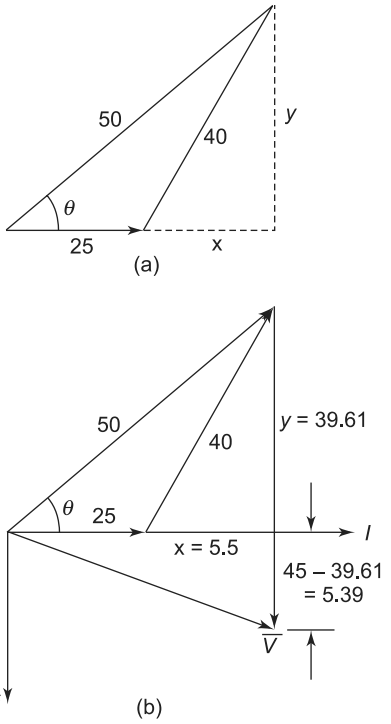


Fig. 3.45

Example 3.16

Convert the time-domain circuit of Fig. 3.46 to the frequency domain and solve for i_1 using mesh analysis.

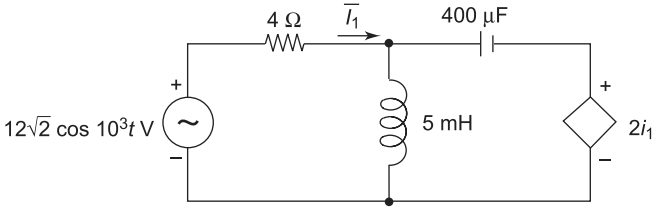


Fig. 3.46

Solution The frequency-domain circuit is drawn in Fig. 3.47 for $\omega = 10^3$ rad/s. The mesh equations are as follows:

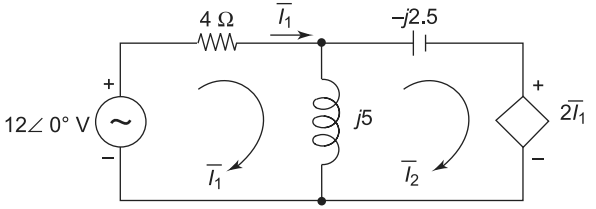


Fig. 3.47

Mesh 1: $(4 + j5)\,\bar{I}_1 - j5\bar{I}_2 = 12$ (i)

Mesh 2: $-j5\ \bar{I}_1 + j2.15\ \bar{I}_2\,72 = -2\,\bar{I}_1$ (ii)

or $(2 - j5)\,\bar{I}_1 - j2.5\bar{I}_2 = -2\bar{I}_1$ (iii)

Solving Eqs (i) and (ii), we get

$$\Delta = \begin{vmatrix}(4 + j5) & -j5\\ (2 - j5) & j2.5\end{vmatrix} = 12.5 + j20 = 23.58 \angle 58°$$

$$\Delta_1 = \begin{vmatrix}12 & -j5\\ 0 & j2.5\end{vmatrix} = j30 = 30 \angle 90°$$

$$\Delta_2 = \begin{vmatrix}(4 + j5) & 12\\ (2 - j5) & 0\end{vmatrix} = -24 + j60 = 64.42 \angle 111.8°$$

$$\bar{I}_1 = \Delta_1|\Delta_2 = 30 \angle 90°|64.42 \angle 111.8° = 0.46 \angle -21.8° \text{ A}$$

$$i_1 = 0.46\sqrt{2}\cos(10^3 t - 21.8°)\text{ A}$$

Example 3.17

For the circuit of Fig. 3.48, find the current $i(t)$ using the superposition theorem.

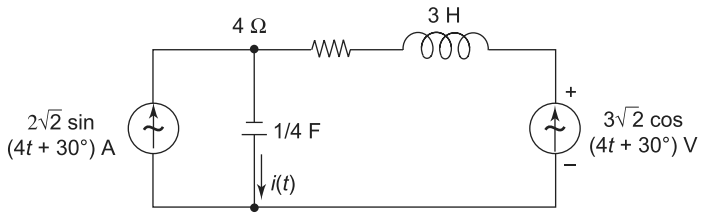


Fig. 3.48

Solution

$$\omega = 4 \text{ rad/s}$$

$$3H \rightarrow j4 \times 3 = j12\ \Omega$$

$$1/4\,F \rightarrow -j(1/(1/4) \times 4) = -j1\,\Omega$$

$$2\sqrt{2}\sin(4t + 10°) \rightarrow 2 \angle 10° \text{ A}$$

$$3\sqrt{2}\cos(4t + 30°) \rightarrow 3 \angle (90° + 30°) = 3 \angle 120° \text{ V}$$

The frequency-domain circuit is drawn in Fig. 3.49 (sine is taken as reference).

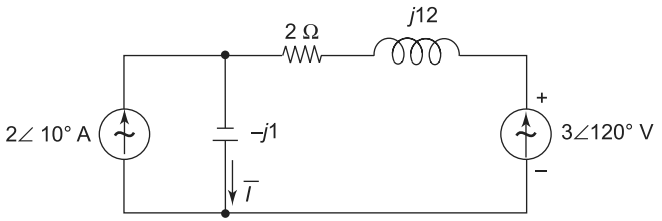


Fig. 3.49

Employing superposition, the circuit as an excited current/voltage source is redrawn in Fig. 3.50(a) and 3.50(b). Calculations of $\bar{I}_1$ and $\bar{I}_2$ are carried out as follows:

$$\bar{I}_1 = \left(\frac{2+j2}{2+j2-j1}\right) \times 2\angle 10° = 2.828\angle 45° \times 2\angle 10°/2.236\angle 26.6°$$

$$= 2.53\angle 28.4° = 2.23 + j1.20\,\text{A}$$

$$\bar{I}_2 = 3\angle 120°/(2+2j-j1) = 3\angle 120°/2.236°\angle 26.6°$$

$$= 1.342\angle 93.4° = -0.08 + j1.34\ \text{A}$$

$$\therefore \quad \bar{I} = \bar{I}_1 + \bar{I}_2 = 2.14 + j2.55 = 3.33\angle 50°\ \text{A}$$

$$i(t) = 3.3\sqrt{2}\sin(4t + 50°)\,\text{A}$$

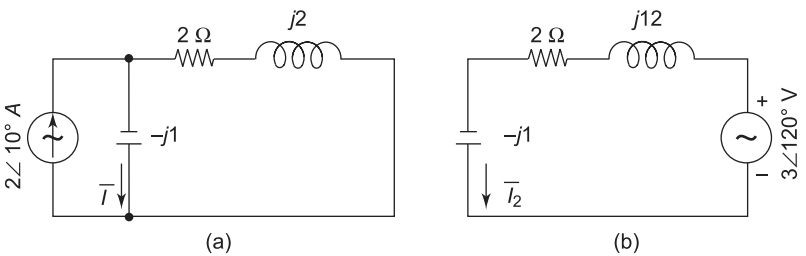


Fig. 3.50

Example 3.18

A coil of 8 Ω resistance and 0.1 H inductance is connected in series with a condenser of 160 μF capacitance across a 230 V, 50 Hz supply (Fig. 3.51). Calculate (a) the inductive reactance, (b) the capacitive reactance, (c) the circuit impedance, current and the pf, and (d) the coil and condenser voltages respectively.

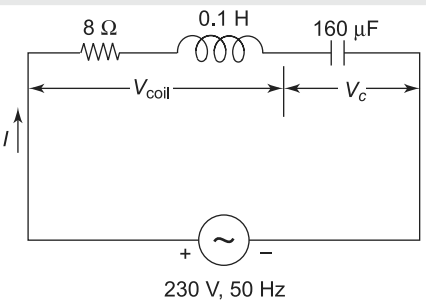


Fig. 3.51

Solution

(a) $X_L = 314 \times 0.1 = 31.4\ \Omega$

(b) $X_C = 10^6/314 \times 160 = 19.9\ \Omega$

(c) $$Z = \sqrt{[8^2 + (31.4 - 19.9)^2]} = 14\ \Omega$$

$$I = V/Z = 230/14 = 16.43\ \text{A}$$

$$\text{pf} = \cos \tan^{-1} (31.4 - 19.9)/8 = 0.572 \text{ lagging } (X_L > X_C)$$

(d) $$V_{\text{coil}} = 16.43\sqrt{8^2 + 31.4^2} = 532.4\ \text{V}$$

$$V_c = 16.43 \times 19.9 = 327\ \text{V}$$

Remark Observe that coil voltage and condenser voltage are more than the applied voltage. This phenomenon will be studied later in this chapter.

Example 3.19

The time-domain circuit of Fig. 3.52 is excited with a voltage source $v_s(t) = 4\sqrt{2}\cos 2t$.

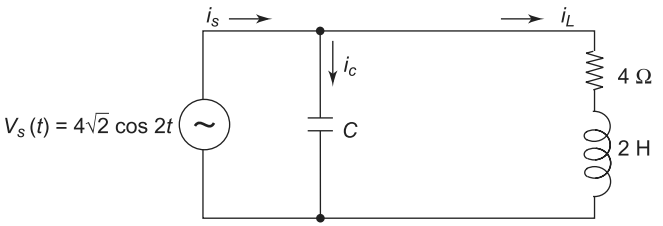


Fig. 3.52 *Time-domain circuit*

(a) Draw the frequency-domain circuit labelling current and voltages.

(b) Determine the value of the capacitor C such that $\bar{I}_s$ is in phase with $\bar{V}_s$.

(c) Draw the phasor diagram showing voltage and currents.

Solution

(a) The frequency-domain circuit is drawn in Fig. 3.53 wherein

$$\bar{V}_s = 4 \angle 0°, X_L = \omega L = 2 \times 2 = 4\ \Omega, X_C = \frac{1}{\omega C} \text{ to be determined}$$

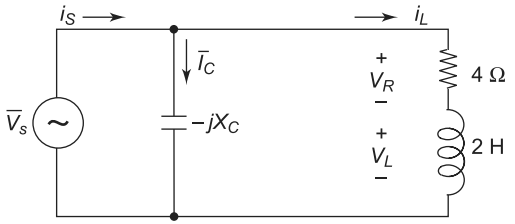


Fig. 3.53

(b) $$\bar{I}_S = \bar{I}_L + \bar{I}_C$$

For $\bar{I}_s$ to be in phase with $\bar{V}_s$,

$$\bar{I}_s = I_s \angle 0°$$

It means that its imaginary part is zero.

For this, the imaginary parts of $\bar{I}_L$ and $\bar{I}_C$ should cancel out.

$$I_L = \frac{4}{4+j4} = \frac{1}{1+j1} = \left(\frac{1}{2} - j\frac{1}{2}\right) = \frac{1}{\sqrt{2}} \angle -45^\circ \text{ A}$$

Its imaginary part is $\left(-j\frac{1}{2}\right)A$

$$\bar{I}_C = \frac{4}{jX_C} = j\frac{4}{X_C} \text{ is imaginary only}$$

Then

$$j\frac{4}{X_C} - j\frac{1}{2} = 0 \text{ or } X_C = 8\ \Omega,\ X_C = \frac{1}{\omega C} = \frac{1}{2C} = 8 \Rightarrow C = \frac{1}{16} = 0.0625 \text{ F}$$

$$\bar{I}_C = j\frac{1}{2} = j0.5$$

(c) Phase diagram is drawn in Fig. 3.54.

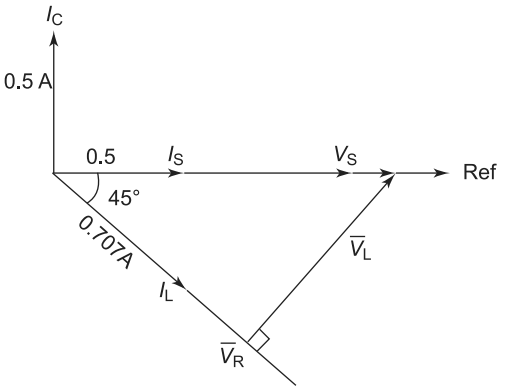


Fig. 3.54

$$\bar{V}_R = \frac{1}{\sqrt{2}} \times 4 = 2\sqrt{2} \text{ V}$$

$$\bar{V}_L = \frac{1}{2} \times 4 = 2\sqrt{2} \text{ V}$$

$\bar{V}_L$ loads and $\bar{V}_R$ by 90°

Example 3.20

In the circuit of Fig. 3.55, R = 2 Ω, L = 0.3 H and $i_R = 10\sqrt{2}\cos(10t + 45^\circ)$ A with v as reference. Draw the phasor diagram showing $\bar{V}_C$, $\bar{V}$ and $\bar{I}_L$.

Determine therefrom

(a) value of capacitor

(b) $\bar{I}_L$ and $i_L(t)$

(c) $\bar{V}$ and $v(t)$

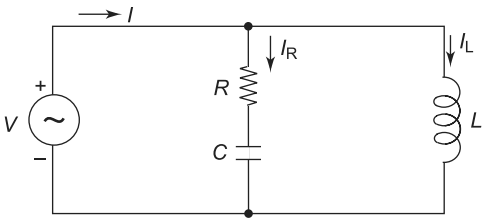


Fig. 3.55

Solution

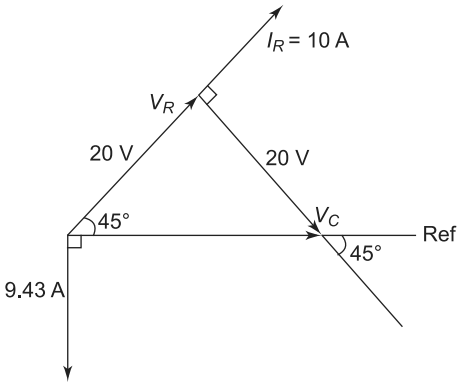


Fig. 3.55(a)

Note Parts not indicated

The phasor diagram is drawn in Fig. 3.55(a)

$$\bar{I}_R = 10 \angle 45°$$

$$\bar{V} = V \angle 0°$$

As $R = 2\ \Omega$,

$$R\bar{I}_R = 2 \times 10 \angle 45° = 20 \angle 45° \text{ V}$$

$\bar{V}_C$ being capacitor voltage lags $\bar{I}_R = \bar{I}_C$ by 90°

From the voltage triangle, we find

$$\bar{V}_C = 20 \angle 45° - 90° = 20 \angle -45° \text{ V}$$

Also, $$\bar{V} = 20\sqrt{2} \angle 0° \text{ V} = 28.28$$

Now $V_C = \omega C I_C$; $\omega = 10$ rad/s

$$C = \frac{20}{10 \times 10} = 0.2 \text{ F}$$

$$X_L = \omega L = 10 \times 0.3 = 3\ \Omega$$

$$\bar{I}_L = \frac{\bar{V}}{X_L} \angle -90° = \frac{20\sqrt{2}}{3} \angle -90°\ \text{V}$$

From $\bar{V}_C$,

$$v_C = 28.28 \cos (10t - 45°)$$

From $\bar{I}_L$,

$$i_L(t) = 9.43 \cos (10t - 90°) = 9.43 \sin 10t\ \text{A}$$

Example 3.21

In the circuit of Fig. 3.56(a), R = 2 kΩ , C = 5 μF. Determine its series circuit equivalent having the same terminal (driving point) admittance at ω = 1000 rad/s.

Solution

$$X_C = \frac{1}{\omega C} = \frac{1}{1000 \times 5 \times 10^{-6}}$$

Terminal admittance

$$\bar{Y} = \frac{1}{R} + \frac{1}{-jX_C} = (0.5 + j5) \times 10^{-3}\ \text{℧}$$

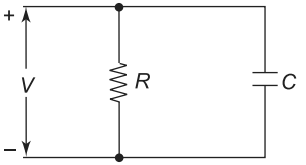


Fig. 3.56(a)

The series equivalent is drawn in Fig. 3.56. For the series circuit to have same admittance, it is convenient to match the impedances.

From Eq. (i),

$$\bar{Z}_i = \frac{1}{Y_i} = \frac{10^3}{0.5 + j5} = \frac{0.5 - j5}{0.25 + 25} \times 10^3 = 19.8 - j198\ \Omega$$

Therefore, $R_{\text{eq}} = 19.8\ \Omega$

$$X_{C\text{eq}} = 198\ \Omega = \frac{1}{1000 \times C}$$

or $$C = \frac{10^6}{1000 \times 198} = 50.5\ \mu\text{F}$$

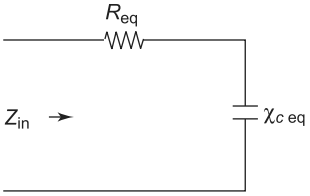


Fig. 3.56 (b)

Example 3.22

Find the Thevenin and Norton equivalents as seen from the terminals '*a*' and '*b*' of the circuit of Fig. 3.57. Draw the equivalent circuits.

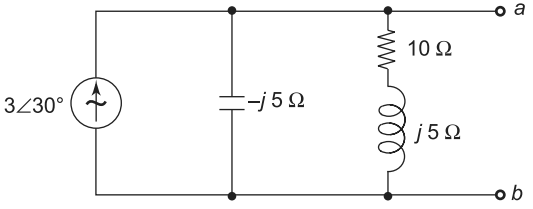


Fig. 3.57

Solution Impedance of each parallel branch

$$\bar{Z}_C = -j5$$

$$\bar{Z}_{RL} = (10 + j5)$$

By current division,

$$\bar{I}_C = \frac{10 + j5}{10 + j5 - j5} \times 3 \angle 30° = (1 + j0.5) \times 3 \angle 30°$$

$$= 1.12 \angle 26.6° \times 3 \angle 30°$$

$$= 3.36 \angle 56.6° \text{ V}$$

Open-circuit voltage

$$\bar{V}_{OC} = \bar{V}_{TH} = -j5 \times \bar{I}_C = -j5 \times 3.36 \angle 56.6°$$

$$= 16.8 \angle -33.4 \ V$$

Open-current source impedance seen from '*a*', '*b*'

$$\bar{Z}_{TH} = \frac{-j5 \times (10 + j5)}{10 + j5 - j5} = -j5(1 + j0.5)$$

$$= 2.5 - j5 \ \Omega$$

or $3.59 \angle -63.4° \ \Omega$

The Thevenin equivalent is drawn in Fig. 3.57(a).

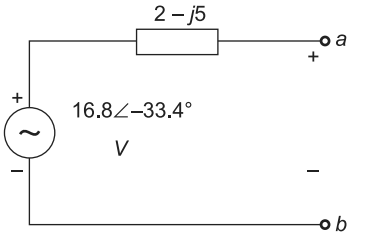


Fig. 3.57(a)

Norton's Equivalent We find short-circuit current to be

$$\bar{I}_{SC} = \frac{V_{TH}}{Z_{TH}} = \frac{16.8 \angle -33.4°}{5.59 \angle -63.4} = 3 \angle 30° \text{ A}$$

The Norton's equivalent is drawn in Fig. 3.57(b). Observe the direction of I_{SC}. It is such as to produce the same-polarity at '*ab*' as $\bar{V}_{OC}$. It is also observed that if '*ab*' are shorted in Norton, I_{SC} would flow in the same direction as in Thevenin on shorting '*ab*'.

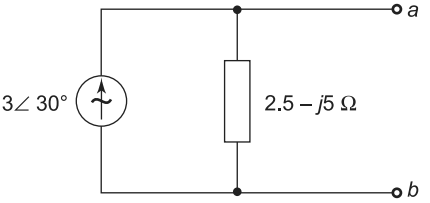


Fig. 3.57(b)

Example 3.23

A resistance of 6 Ω is connected in series with a choke having a resistance *r* and inductance *L* connected in series across a voltage source of voltage 240 V, 50 Hz. The voltage drop across the resistance is 120 V and across choke coil is 205 V. Calculate (a) resistance, inductance and impedance of the choke coil, and (b) its power loss and power factor.

Solution The circuit for this problem is drawn in Fig. 3.58

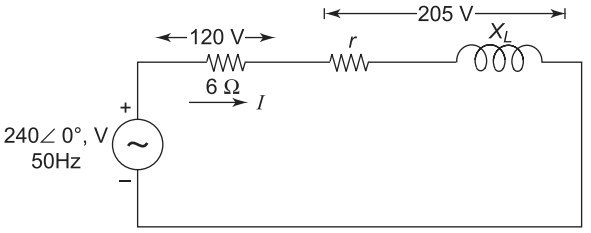


Fig. 3.58

(a) By Ohm's law,

$$I = \frac{120}{6} = 20 \text{ A}$$

$$20\sqrt{(6+r)^2 + X_L^2} = 240 \text{ V} \quad \text{(i)}$$

$$20\sqrt{r^2 + X_L^2} = 205 \text{ V} \quad \text{(ii)}$$

Equations (i) and (ii) yield

$$r = 1.5\ \Omega \qquad X_L = 10.14\ \Omega \qquad L = \frac{10.14}{2\pi \times 50} = 32.28 \text{ mH}$$

$$Z = \sqrt{(1.5)^2 + (10.14)^2} = 10.25\ \Omega$$

(b) Power loss in choke $= (20)^2 \times 1.5 = 600$ W

Power factor of choke $= \dfrac{600}{205 \times 20} = 0.146$ lagging

Example 3.24

Average power drawn by the load in Fig. 3.59 is 200 kW, pf = 0.707 lagging. The source voltage is $v(t) = 2000\sqrt{2}\cos 314\,t$. Find the value of the shunt capacitor C to as to raise the combined pf to 0.85 lagging.

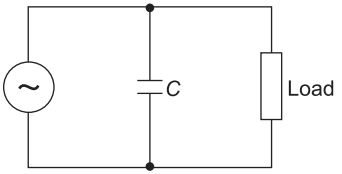


Fig. 3.59

Solution

$$\text{pf} = \cos\theta = 0.707 \Rightarrow \theta = 45° \text{ lag}$$

From P, Q, S phasor diagram,

$$\frac{Q}{P} = \tan\theta = \tan 45° = 1$$

$$Q = P = 200 \text{ KVA (positive)}$$

For $\text{pf} = \cos\theta' = 0.85$ log $\theta'' = 32°$, $\tan\theta' = 0.62$

$$\tan\theta' = \frac{Q(\text{load} + \text{cap})}{P} = 0.62$$

$$Q' = 200 \times 0.62 = 124 \text{ kVAR}$$

$$Q' = Q - Q_C$$

$$124 = 200 - Q_C = 76 \text{ kVAR}$$

$$X_C = \frac{1}{\omega C} = \frac{1}{314C}$$

$$I_C = \frac{2000}{X_C} = 2000 \times 314C$$

$$V = 2000 \text{ V}$$

$$Q_C = VI_C = (2000)^2 \times 314C = 76 \times 10^3$$

or $$C = \frac{76 \times 10^3}{(2000)^2 \times 314} = \frac{76 \times 10^{-6}}{4 \times 0.314} = 60\ \mu\text{F}$$

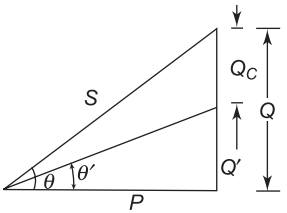


Fig. 3.59(a)

Example 3.25

In the circuit of Fig. 3.60, $L_1 = L_2 = 2$ mH, $C = 500$ μF and $R = 2\ \Omega$

(a) For $v = 10\sqrt{2}\cos(1000t + 90^\circ)V$, determine the input impedance.

(b) Calculate $\bar{I}$, $\bar{I}_R$ and $\bar{I}_{L2}$ show them on a phasor diagram along with $\bar{V}, \bar{V}_L$ and $\bar{V}, \bar{V}_C$.

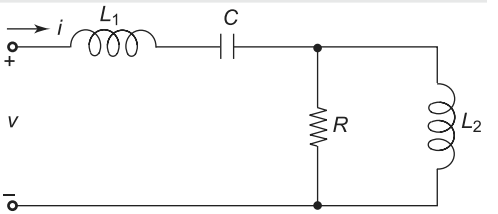


Fig. 3.60

Solution Transforming the circuit to frequency domain,

$$\bar{V} = 10 \angle 90^\circ \text{V}, \quad \omega = 1000 \text{ rad/s}$$

$$C \to \frac{1}{j\omega C} = -\frac{10^6}{1000 \times 500} = -j2\ \Omega$$

$$L_1 = L_2 \to j\omega L$$

$$= j \times 1000 \times 2 \times 10^{-3}$$

$$= j2\ \Omega$$

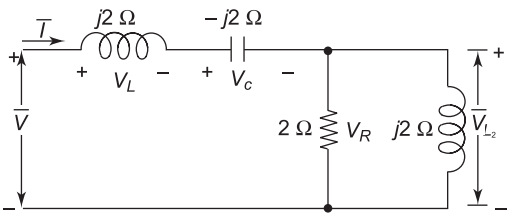


Fig. 3.60(a)

The circuit is redrawn in Fig. 3.60(a).

(a) Input impedance

R, L in parallel

$$\bar{Z}_2 = 2 \| (j2) = \frac{j4}{2 + j2} = \frac{j2}{1 + j1} = \frac{j2}{\sqrt{2} \angle 45^\circ} = \sqrt{2} \angle 45^\circ \Omega$$

L_1, C in series

$$\bar{Z}_1 = j2 - j2 = 0\ \Omega$$

Therefore,

$$\bar{Z} = \bar{Z}_2 + \bar{Z}_1 = \sqrt{2} \angle 45^\circ\ \Omega$$

(b)
$$\bar{I} = \frac{\bar{V}}{\sqrt{2} \angle 45^\circ} = \frac{10 \angle 90^\circ}{\sqrt{2} \angle 45^\circ} = 5\sqrt{2} \angle 45^\circ$$

$$\bar{V}_{12} + \bar{V}_R = \bar{V} = 10 \angle 90^\circ \text{V}; \ \bar{V}_C = -j2\bar{I} = -j2 \times 5\sqrt{2} \angle 45^\circ = 10\sqrt{2} \angle -45^\circ \text{A}$$

$$\bar{I}_R = \frac{10 \angle 90^\circ}{2} = 5 \angle 90^\circ$$

$$\bar{I}_{L2} = \frac{10 \angle 90^\circ}{2} = 5 \angle 0^\circ$$

Phasor diagram [Fig. 3.60(b)]

Reference phasor $\bar{I}_L = 5 \angle 0^\circ$

$$\bar{V}_L = 10 \angle 90^\circ$$

$$\bar{V}_L = \bar{V}_R = \bar{V}$$

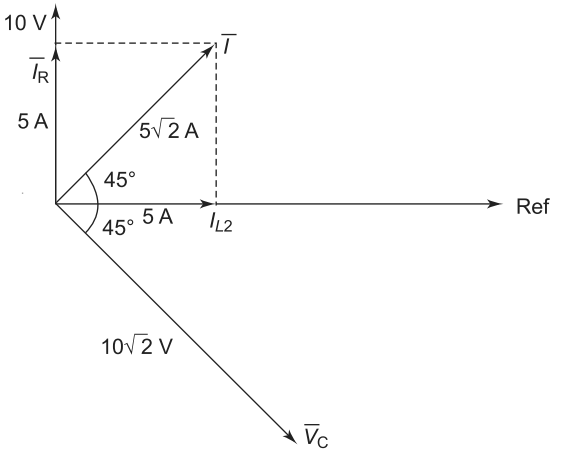


Fig. 3.60(b)

Example 3.26

In the circuit of Fig. 3.61, find the Thevenin equivalent at '*AB*' and from there find the complex power fed to the load. What should be the load impedance so that it receives maximum power?

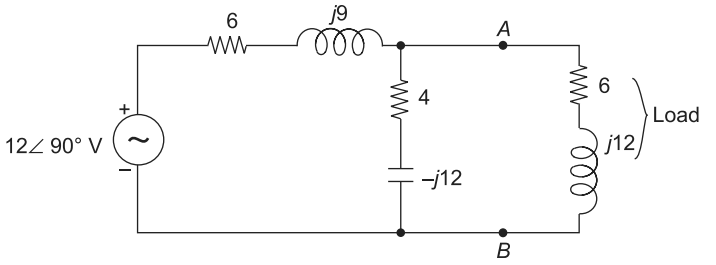


Fig. 3.61

Solution Thevenin equivalent voltage

$$V_{TH} = V_{OC} = \left[\frac{4 - j12}{(6+4) - j(12-9)}\right] \times 12 \angle 90°$$

$$= \frac{4 - j12 = 12.65 \angle -71.6°}{10 - j3 = 10.44 \angle -16.7°} \times 12 \angle 90°$$

$$= 14.54 \angle 35.1° \text{ V}$$

Short circuit the voltage source and

$$Z_{TH} = (6 + j\,9) \| (4 - j\,12)$$

$$= \frac{10.82 \angle 56.3° \times 12.65 \angle -71.6°}{10 - j3 = 10.44 \angle -16.7°} = 13.1 \angle -54.9° = 7.47 - j10.64\ \Omega$$

The circuit in the form of Thevenin equivalent is drawn in Fig. 3.61(a).

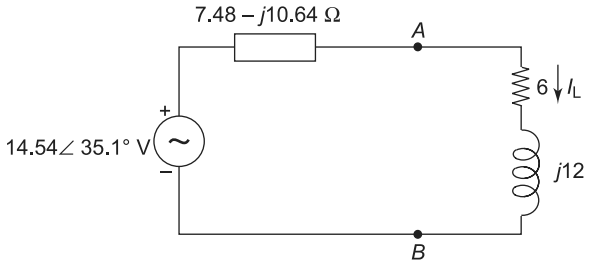


Fig. 3.61(a)

$$\bar{I}_L = \frac{14.54 \angle 35.1°}{(7.48 + 6) + j(12 - 10.64)}$$

$$= \frac{14.54 \angle 35.1}{13.48 + j1.36} = \frac{14.54 \angle 35.1°}{13.54 \angle 5.7°}$$

$$= 1.07 \angle 29.4° \text{ A}$$

Complex power fed to load

$$\bar{S} = \bar{V}\,\bar{I}^* = \bar{Z} \cdot \bar{I} \cdot \bar{I}^* = I^2 \bar{Z}$$

$$= (1.07)^2 \times (6 + j12)$$

$$= 6.86 \text{ W} + j\ 13.7 \text{ VAR (inductive)}$$

Load from maximum power output

$$\bar{Z}_L = \bar{Z}^*_{\text{TH}} = 7.48 + j10.64\,\Omega = 13.1 \angle 54\ 9° \ \Omega$$

$$\bar{I}_L = \frac{14.54 \angle 35.1°}{\bar{Z}_{\text{TH}} + \bar{Z}^*_{\text{TH}}} = \frac{14.54 \angle 35.1°}{2 \times 7.48} = 0.972 \angle 35.1° \text{ A}$$

Output

$$\bar{S} = (0.972)^2 \times 13.1 \angle 54.9°$$

$$= 12.37 \angle 54.9° \text{VA}$$

$$= 7.11\text{W} + j10.12 \text{ VAR (inductive)}$$

Maximum real power output = 7.11 W (more than 6.86 W)

Example 3.27

For the network of Fig. 3.62, what load impedance across terminal '*ab*' would absorb maximum average real power? What is the value of this real power?

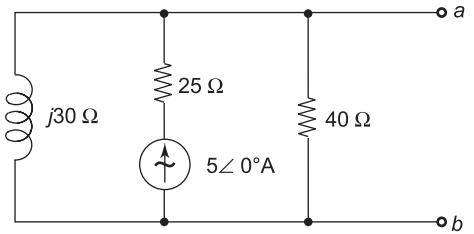


Fig. 3.62

Solution Thevenin impedance (current source open-circuited) as seen from terminals '*ab*'

$$\bar{Z}_{\text{TH}} = 40 \| (j30) = \frac{j40 \times 30}{40 + j30} = \frac{j120}{4 + j3}$$

$$= \frac{j120(4 - j3)}{25} = \frac{360 + j480}{25}$$

$$= \frac{600 + \angle 53.1°}{25} = 24 \angle 53.1° = 14.4 + j19.2\,\Omega$$

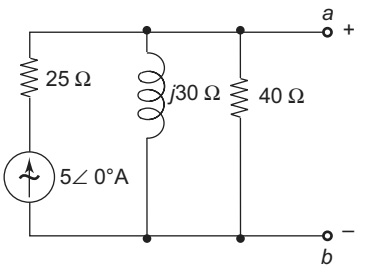


Fig. 3.63(a)

For maximum power absorption,

$$\bar{Z}_L = \bar{Z}^*_{\text{TH}} = 24 \angle -5.31°$$

Thevenin voltage from Fig. 3.63(a),

$$\bar{V}_{\text{TH}} = 24 \angle 53.1° \times 5 \angle 0°$$

$$= 120 \angle 53.1° \text{ V}$$

$$\bar{Z}_{\text{TH}} + \bar{Z}^*_{\text{TH}} = 2\,\text{Re}(\bar{Z}_{\text{TH}})$$

$$= 2 \times 14.4 = 28.8\,\Omega$$

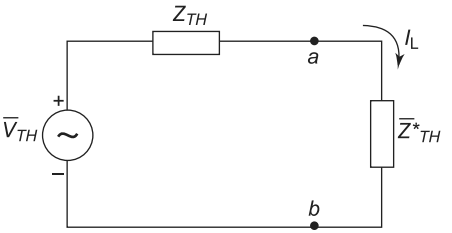


Fig. 3.63(b)

Therefore,

$$\bar{I}_L = \frac{\bar{V}_{\text{TH}}}{28.8} = \frac{120 \angle 53.1°}{28.8}$$

$$= 4.17 \angle 53.1° \text{ A}$$

$$I_L = 3.17 \text{ A}$$

Maximum real power absorbed

$$P \text{ (max)} = I_L^2 \times 14.4 \text{ ; where Re } (\bar{Z}^*_m) = 14.4\,\Omega$$

$$= (4.17)^2 \times 14.4 = 250 \text{ W}$$

Example 3.28

In the circuit of Fig. 3.64 $v_s(t) = 4\sqrt{2} \cos 2t$ V, (a) determine $\bar{I}_L$ (b) find the value of C such that $\bar{I}_S$ is in phase with $\bar{V}_S$ (c) draw the complete phasor diagram.

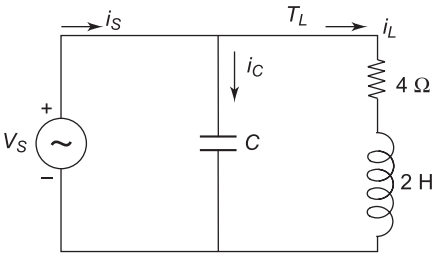


Fig. 3.64

Solution Transforming the circuit to frequency domain

$$v_s(t) = \bar{V}_s = 4\sqrt{2} \angle 0° \text{ V}, \omega = 2 \text{ rad/s}$$

$$2\text{H} \rightarrow j\,2 \times 2 = j4\ \Omega$$

$$C \rightarrow \frac{1}{j\,2C}$$

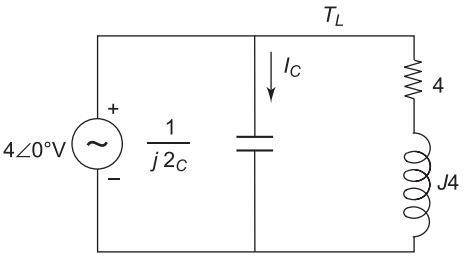


Fig. 3.64(a)

The frequency domain circuit is drawn in Fig. 4.64(a).

(a) $$\bar{I}_L = \frac{4\sqrt{2} \angle 0°}{4 + j4} = \frac{\sqrt{2} \angle 0°}{1 + j1}$$

$$= 1 \angle -45° \text{ A}$$

$$= \left(\frac{1}{\sqrt{2}} - j\frac{1}{\sqrt{2}}\right) \text{A}$$

(b) For $\bar{I}_S$ to be in phase with $\bar{V}_s$, $\bar{I}_C$ should cancel the imaginary part of $\bar{I}_2$. Therefore

$$I_C = j\frac{1}{\sqrt{2}} = \frac{4\sqrt{2} \angle 0°}{\frac{1}{j\,2C}} = j8\sqrt{2}C$$

Or $$C = \frac{1}{16} = 0.0625 \text{ F}$$

(c) The phasor

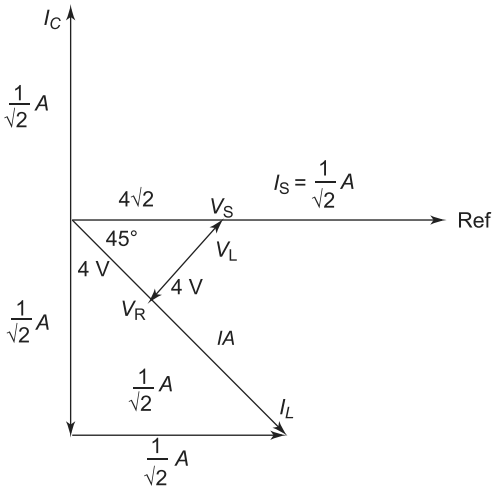


Fig. 3.64(b)

3.7 RESONANCE

Here, we shall consider circuits that pass a narrowband of frequencies and reject others. Such circuits are known as *resonant circuits*, and the phenomenon of resonance occurs in all types of physical systems, e.g. in a stringed instrument.

Consider the *RLC* series and parallel networks of Fig. 3.65(a) and (b).

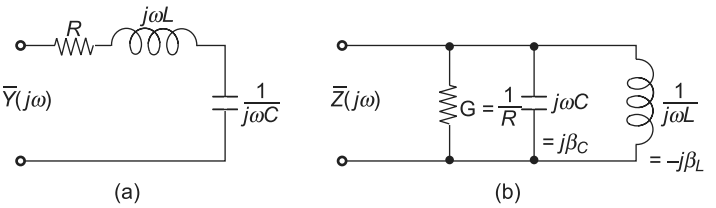


Fig. 3.65 *(a) RLC series network (b) RLC parallel network*

3.7.1 Series Circuit

$$\bar{Y}(j\omega) = \frac{1}{\bar{Z}(j\omega)} = \frac{1}{R + j\left(\omega L - \frac{1}{\omega C}\right)} \tag{3.54}$$

3.7.2 Parallel Circuit

$$\bar{Z}(j\omega) = \frac{1}{\bar{Z}(j\omega)} = \frac{1}{G + j\left(\omega C - \frac{1}{\omega L}\right)} \tag{3.55}$$

Observe that the admittance of the series circuit has the same form as the impedance of the parallel circuit (replace R by G and L by C). This is because the two circuits are *dual* of each other. Both circuits can therefore be treated together.

From Eqs (3.54) and (3.55), it immediately follows that admittance of the series circuit and the impedance of the parallel circuits are maximum when the following condition is satisfied

$$\omega L = \frac{1}{\omega L}$$

If frequency is variable (with fixed L and C), this condition (called condition of resonance) is satisfied at a frequency of

$$\omega_0 = \frac{1}{\sqrt{LC}} \text{ ; } \textit{resonant frequency} \tag{3.56}$$

At the resonant frequency,

Series circuit: $$\bar{Y}(j\omega_0) = \frac{1}{R} = \bar{Y}_0 \text{ (maximum admittance)} \tag{3.57}$$

Parallel circuit: $$\bar{Z}(j\omega_0) = \frac{1}{G} = \bar{Z}_0 \text{ (maximum impedance)} \tag{3.58}$$

The plots of $|\bar{Y}(j\omega)|$ for the series circuit and $|\bar{Z}(j\omega)|$ for the parallel circuit drawn in Figs 3.66(a) and (b) as ω is varied from 0 to ∞. These plots, are similar as Eqs (3.54) and (3.55) have the same form. The nature of the plot is induced by the reasoning below.

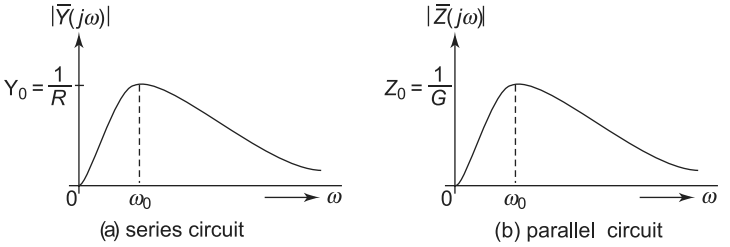


Fig. 3.66

At $\omega = 0$,

$$\frac{1}{\omega C} = \infty \Rightarrow |\bar{Y}(j\omega)| = 0 \tag{3.59}$$

$$\frac{1}{\omega L} = \infty \Rightarrow |\bar{Z}(j\omega)| = 0 \tag{3.60}$$

At $\omega \to \infty$,

$$\omega L = \infty \Rightarrow |\bar{Y}(j\omega)| = 0 \tag{3.59a}$$

$$\omega C = \infty \Rightarrow |\bar{Z}(j\omega)| = 0 \tag{3.60a}$$

These plots, therefore, start at zero at $\omega = 0$, pass through a maxima and tend to zero asymptotically as $\omega \to \infty$. The magnitudes of the maximum admittance and maximum impedance, and the frequency at which these occur are found below.

Consider a fixed amplitude, variable frequency, voltage-excited series circuit and current-excited parallel circuit as in Fig. 3.67(a) and (b). It then follows from Eqs (3.54) and (3.55) that

$$\bar{I} = \frac{V \angle 0^\circ}{R + j\left(\omega L - \frac{1}{\omega C}\right)} \text{ (series circuit)} \tag{3.61}$$

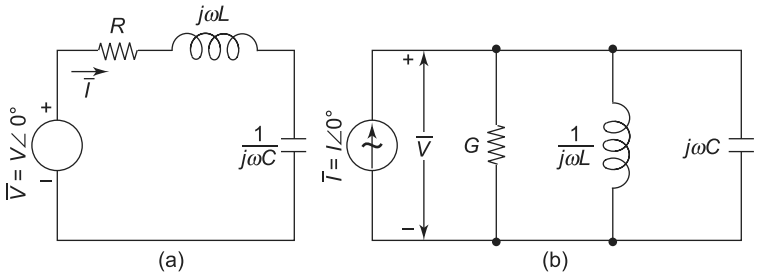


Fig. 3.67 *(a) Voltage excited RLC series circuit (b) Current excited RLC parallel network*

$$\bar{V} = \frac{\bar{I} \angle 0^\circ}{R + j\left(\omega L - \frac{1}{\omega C}\right)} \text{ (parallel circuit)} \tag{3.62}$$

As per Eqs (3.57) and (3.58),

$$\bar{I}(\max) = \frac{V}{R} \text{ (series circuit)} \tag{3.62a}$$

$$\bar{V}(\max) = \frac{1}{G} \text{ (parallel circuit)} \tag{3.62b}$$

It follows from Eqs (3.62a) and (3.62b) that at *resonance*, *both circuits have unity power factor*.

Under resonance condition, the circuit behaviour is described below:

1. For a series circuit, unity power factor, admittance (pure conductance) is maximum or impedance (pure resistance) is minimum.
2. For a parallel circuit, unity power factor, impedance (pure resistance) is maximum or admittance (pure conductance) is minimum. We can, therefore, make the general statement that "at resonance, the terminal voltage and input current to the circuit are in phase, i.e. pf is unity."

The phasor diagrams at resonance for the series and parallel circuits are drawn in Figs. 3.68(a) and (b) respectively.

It is seen from Eqs (3.59) and (3.60) and also Eqs (3.61) and (3.62) that the equations for admittance of series and impedance of parallel circuit have the same form. *So from now onwards we will deal with parallel resonant circuit only* as this has more practical applications.

From the phasor diagram of Fig. 3.68(b), it is seen that the inductance and capacitance currents cancel out and the current input equals the conductance current. We can write the expressions for inductance and capacitance currents at resonance in terms of the resonance frequency.

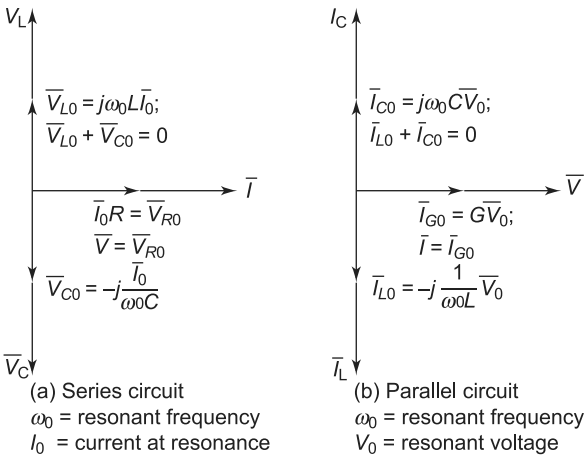


Fig. 3.68 *Phasor diagrams at resonance*

Capacitance current

$$\bar{I}_{C0} = j\omega_0 C\bar{V}_0$$

But $$\bar{V}_0 = \bar{I}/G = R\bar{I};\ \bar{I} = \bar{I}_{G0}$$

Then $$\bar{I}_{C0} = j\omega_0 CR\bar{I} \tag{3.63}$$

Inductance current

$$\bar{I}_{L0} = -j\frac{1}{\omega_0 L}\bar{V}_0$$

$$= -j\frac{1}{\omega_0 L}R\bar{I}$$

$$= -j\omega_0 CR\bar{I} \tag{3.64}$$

It then follows that

$$\bar{I}_{C0} + \bar{I}_{L0} = 0 \tag{3.65a}$$

and also

$$\left|\bar{I}_{C0}\right| = \left|\bar{I}_{L0}\right| = \omega_0 CR\, I\ ;\ I = \text{input current} \tag{3.65b}$$

It is seen that from the above equations and the phasor diagram that the net current drawn by the *LC* combination is zero, while all the input current flows through the conductance (*G*). The voltage across the circuit is then $\bar{V}_0 = \bar{I}/G = \bar{I}R;\ \bar{I} = \bar{I}_{G0}$, which indeed implies unity pf for the complete circuit.

The current that circulates through *L* and *C* has a magnitude $(\omega_0 CR)I$. In a resonant circuit by design $\omega_0 CR >> 1$ (it is the circuit's *quality factor* as we shall soon see)

$$I_{C0} = I_{L0} >> I \text{ (input current)}$$

It means that resonant *LC* circulating current is far larger than input current, a sort of current amplifying effect.

Similarly, for the series resonant circuit, we find from the phasor diagram of Fig. 3.68(a),

$$\left|\bar{V}_{L0}\right| = \left|\bar{V}_{C0}\right| = \omega_0 L I_0 \tag{3.65c}$$

and

$$\bar{V}_{L0} + \bar{V}_{C0} = 0 \tag{3.65d}$$

The applied voltage, therefore, drops across resistance only that is

$$V = RI_0 \text{ or } I_0 = \frac{V}{R} \tag{3.65e}$$

Equation (3.65c) is then written as

$$V_{L0} = V_{C0} = \left(\omega_0 \frac{L}{R}\right) V$$

In series resonance, $\left(\omega_0 \dfrac{L}{R}\right) >> 1$ as it is the *quality factor*.

Thus,

$$V_{L0} = V_{C0} >> V \text{ (input voltage)} \tag{3.65f}$$

In other words, the voltage drops across *L* and *C* are far larger than the applied voltage.

Frequency Response

Consider again the parallel circuit excited by fixed magnitude of input current, but variable frequency, and examine the variation of the magnitude of the circuit terminal voltage (it will of course have the same frequency as the input current). The frequency response of the circuit is sketched in Fig. 3.69.

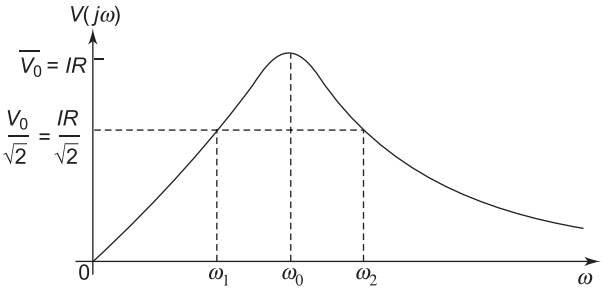


Fig. 3.69 *Frequency response of parallel circuit; ω_0 = resonant frequency, R = 1/G*

The voltage magnitude peaks at ω_0 which corresponds to maximum impedance (resistive) as per Eq. (3.62b).

At frequencies ω_1, ω_2 the voltage magnitude reduces to

$$\frac{V_0}{\sqrt{2}} = \frac{IR}{\sqrt{2}} \text{; magnitude of circuit impedance reduces to } R/\sqrt{2} \tag{3.66}$$

Power dissipated in the circuit at these frequencies is

$$\frac{(V_0/\sqrt{2})^2}{R} = \frac{1}{2}\left(\frac{V_0^2}{R}\right) = \text{half of power dissipated at resonance} \tag{3.67}$$

Therefore, these frequencies are known as *half-power frequencies*.

It is observed from Fig. 3.69 that for $\omega < \omega_1$ and $\omega > \omega_2$, the circuit voltage drops sharply. Also at $\omega = 0$, $V = 0$ as inductance acts as a short-circuit.

The range of frequencies between ω_1 to ω_2 is the *pass-band* with *bandwidth*,

$$\omega_b = \omega_1 - \omega_2 \tag{3.68}$$

Before deriving the expression for the circuit bandwidth, it is necessary to define the quality factor which has a direct bearing on the bandwidth.

For the parallel *RLC* circuit of Fig. 3.67(b), how the individual susceptances B_c and B_L, admittance Y and impedance Z vary with frequency are shown in Fig. 3.70(a). Figure 3.70(b) is the plot of Z vs ω indicating $Z_{max} = 1/G$, half power frequencies (at $Z = 1/(\sqrt{2}G) = 0.707/G$) and the pass-band (bandwidth).

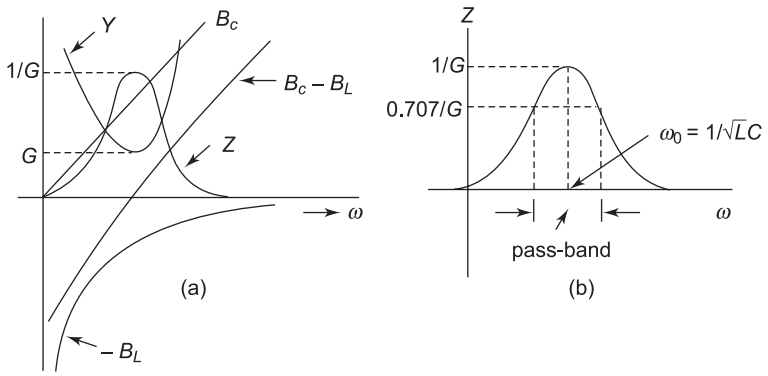


Fig. 3.70 *Frequency response in parallel RLC circuit*

3.7.3 Quality Factor

It is convenient to work in terms of admittance of the parallel circuit (at resonance admittance is minimum). From Eq. (3.55),

$$\bar{Y}(j\omega) = G + j\left(\omega C - \frac{1}{\omega L}\right);\ R = 1/G \tag{3.69}$$

In terms of resonance frequency ω_0, Eq. (3.69) can be written as follows:

We define

$$Q_0 = \frac{\omega_0 C}{G} = \omega_0 RC = 2\pi fRC = \text{quality factor at resonance} \tag{3.70}$$

Then

$$\bar{Y}(j\omega) = \frac{1}{R}\left[1 + jQ_0\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right] \tag{3.71}$$

The quality factor is a dimensionless quantity and it is a determining factor in bandwidth of the circuit as we shall soon see.

It can be proved that

$$Q_0 = 2\pi \left(\frac{\text{maximum energy stored per period}}{\text{total energy lost per period}} \right) \tag{3.72}$$

This is proved later.

For the series *RLC* circuit replacing *C* by *L* and *G* by *R* in Eq. (3.70), the quality factor is given by

$$Q_0 = \omega_0 \frac{L}{R} \tag{3.73}$$

Let us now derive the expression of bandwidth and see how is it affected by the *Q* factor. Reconsider the expression for admittance as in Eq. (3.71), reproduced below.

$$\bar{Y}(j\omega) = G\left[1 + jQ_0\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right] \tag{3.74}$$

At half-power points, the admittance increases to $\sqrt{2}G$ (or impedance reduces to $\frac{R}{\sqrt{2}}$. It is seen from Eq. (3.71) that this can happen only when the imaginary part is ±1. This occurs at two frequencies given by

$$Q_0\left(\frac{\omega_2}{\omega_0} - \frac{\omega_0}{\omega_2}\right) = -1 \text{ and } Q_0\left(\frac{\omega_0}{\omega_0} - \frac{\omega_0}{\omega_1}\right) = 1$$

from which we get the expressions for the two half-power frequencies as

$$\omega_1 = \omega_0 \left[\sqrt{1 + \left(\frac{1}{2Q_0}\right)^2} - \frac{1}{2Q_0} \right] \tag{3.75a}$$

$$\omega_2 = \omega_0 \left[\sqrt{1 + \left(\frac{1}{2Q_0}\right)^2} + \frac{1}{2Q_0} \right] \tag{3.75b}$$

The bandwidth is then found as

$$\omega_b = \omega_2 - \omega_1 = \frac{\omega_0}{Q_0} \tag{3.76}$$

Multiplying Eq. (3.74a) and (3.74b), it can be shown that

$$\omega_0 = \sqrt{\omega_1 \omega_2} \tag{3.77}$$

which means that the resonance frequency is the geometric mean of the two half-power frequencies.

It is easily observed from the expression for is bandwidth [Eq. (3.76)] that higher quality factor means lower bandwidth or greater *frequency selectivity* of the circuit.

For a high-*Q* circuit, Eqs (3.75) (a) and (b) get simplified to

$$\omega_1, \omega_2 = \omega_0 \left(1 \mp \frac{1}{2Q_0}\right); 1 + \left(\frac{1}{2Q_0}\right)^2 = 1$$

$$= \omega_0 \mp \frac{\omega_0}{2Q_0} = \omega_0 \mp \frac{1}{2}\omega_b \tag{3.78}$$

It means that in a high-*Q* circuit, bandwidth is symmetrical about the resonant frequency. In other words, half-power points are located half bandwidth away from ω_0 on either side.

Proof of Eq. (3.72) for Quality Factor

With reference to Fig. 3.67(b) under resonant condition, the currents in inductance and capacitance cancel themselves out and the circuit current $\overline{I}$ flows in the conductance.

Let

$$i(t) = I_m \cos \omega_0 t$$

The corresponding voltage response (at resonance) is

$$v(t) = \frac{i(t)}{G} = \frac{I_m}{G} \cos \omega_0 t$$

The instantaneous energy stored in the capacitance is

$$w_C(t) = \frac{1}{2} C v^2 = \frac{I_m^2 C}{2G^2} \cos^2 \omega_0 t$$

The instantaneous energy stored in the inductor is

$$w_L(t) = \frac{2}{2} L i_L^2 = \frac{1}{2} L \left(\frac{1}{L} \int_0^t v dt \right)^2$$

$$= \frac{I_m^2 C}{2G^2} \sin^2 \omega_0 t$$

The total instantaneous energy stored (in capacitance and in inductance) is

$$w(t) = w_L(t) + w_C(t) = \frac{I_m^2 C}{2G^2}$$

which being constant is also the maximum energy stored.

Average power dissipated by the conductance

$$P_G = \frac{I_m^2}{2G}$$

Energy dissipated in one cycle

$$P_G T = \frac{1}{f_0} \frac{I_m^2}{2G}$$

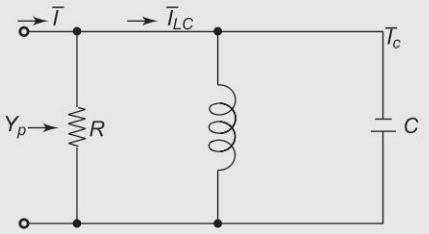
$$= \frac{2\pi}{\omega_0} \frac{I_m^2}{2G}$$

Substituting in Eq. (3.72),

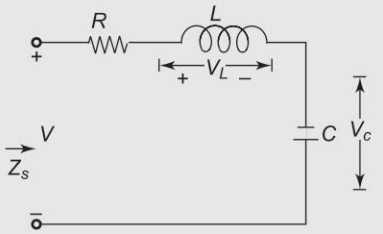
$$Q = 2\pi \left(\frac{I_m^2 C}{2G^2} \right) \Bigg/ \left(\frac{2\pi}{\omega_0} \frac{I_m^2}{2G} \right)$$

$$= \frac{\omega_0 C}{G} = \omega_0 RC$$

Table 3.2 *Summary of resonance:* $\omega_0 = \dfrac{1}{\sqrt{LC}}$



$$Q_0 = \omega_0 RC, \quad \alpha = \frac{1}{2RC}$$



$$Q_0 = \omega_0 \frac{L}{R}, \quad \alpha = \frac{R}{2L}$$

At ω_0, magnitude-wise $I_{L0} = I_{C0} = Q_0 I$	At ω_0, magnitude-wise $V_{L0} = V_{C0} = Q_0 V$
At any frequency $\bar{Y}_p(j\omega) = \frac{1}{R}\left[1 + jQ_0\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right]$	At any frequency $\bar{Z}_s(j\omega) = R\left[1 + jQ_0\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right]$

Half-power frequencies

$$\omega_1, \omega_2 = \omega_0\left[\sqrt{1 + \left(\frac{1}{2Q_0}\right)^2} \mp \frac{1}{2Q_0}\right]$$

$$\omega_0 = \sqrt{\omega_1 \omega_2}$$

Bandwidth $\omega_b = \omega_2 - \omega_1 \dfrac{\omega_0}{Q_0} = 2\alpha$

Approximation valid for high Q_0

$$\omega_1, \omega_2 = \omega_0 \pm \frac{1}{2}\omega_b$$

Example 3.29

A parallel *RLC* circuit has $Q_0 = 200$. Two component values are given. Find the third component value for the following combinations:

(a) $R = 1W$, $C = 2\ \mu F$

(b) $L = 2 \times 10^{-15}$ H, C = 1.2 nF

(c) $R = 118.5\ k\Omega$, $L = 120$ pF

Solution

(a) $Q_0 = \omega_0 RC;\ \omega_0 = \dfrac{1}{\sqrt{LC}}$

$$Q_0 = \frac{1}{\sqrt{LC}}.RC = R\sqrt{\frac{C}{L}}$$

$$200 = 1 \times \sqrt{\frac{2\times10^{-6}}{L}} \Rightarrow L = \frac{2\times10^{-6}}{(200)^2} = 50\times10^{-12} = 50 \text{ pH}$$

(b) $$200 = R \times \sqrt{\frac{1.2\times10^{-9}}{2\times10^{-15}}} \Rightarrow R = 200 \times \sqrt{0.6\times10^{6}} = 155 \text{ k}\Omega$$

(c) $$200 = 118.5\times10^{3}\sqrt{\frac{C}{120\times10^{-12}}}$$

$$\sqrt{C} = \frac{200\sqrt{120\times10^{-12}}}{118.5\times10^{3}} = 18.49\times10^{-9}$$

$$C = 341.9\times10^{-18} = 0.342\times10^{-15} = 342 \text{ pF}$$

Example 3.30

A parallel *RLC* circuit has R = 1 kΩ, C = 40 μF and L = 13 mH. Determine ω_0 and Q_0.

Solution

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{13\times10^{3}\times49\times10^{-6}}}$$

or $$\omega_0 = 1.253\times10^{-3}$$

$$= 1.253 \text{ kHz}$$

$$Q_0 = \omega_0 RC$$

$$= 1.253\times10^{3}\times1\times10^{3}\times49\times10^{-6}$$

$$= 61.4$$

Example 3.31

An RLC series circuit has R = 5 Ω, L = 5 mH and C = 0.08 μF. Calculate (a) ω_0, f_0, (b) ω_b; ω_1, ω_2 and (c) $\overline{Z}_{in}$ at resonant frequency.

Solution

(a) $$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{5\times10^{-3}\times0.08\times10^{-6}} = 50\,k \text{ rad/s}$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{50}{2\pi} = 7.96 \text{ kHz}$$

(b) $$Q_0 = \omega_0 \frac{L}{R} = 50\times10^{3}\times\frac{5\times10^{-3}}{5} = 50$$

$$\text{Bandwidth} = \frac{\omega_0}{Q_0} = \frac{50 \times 1000}{50} = 1000 \text{ rad/s}$$

It is easily seen that we can express

$$\omega_b = \frac{\omega_0}{Q_0} = \frac{\omega_0 R}{\omega_0 L} = \frac{R}{L} = \frac{5}{5 \times 10^{-3}} = 1000 \text{ rad/s}$$

Half-power frequencies

$$\omega_1, \omega_2 = \omega_0 \left[\sqrt{1 + \left(\frac{1}{2Q_0} \right)^2} \pm \frac{1}{2Q_0} \right]$$

$$\frac{1}{2Q_0} = 0.01 \left(\frac{1}{2Q_0} \right)^2 = 0.1 \times 10^{-3} << 1$$

So, we can use the approximate result

$$\omega_1, \omega_2 = \omega_0 \mp \frac{1}{2} \omega_b = 50{,}000 \mp 500$$

$$= 49{,}500 \text{ or } 50{,}500 \text{ rad/s}$$

(c) $\bar{Z}_{\text{in}} = R = 5\ \Omega$

Example 3.32

A series circuit has an inductor of L = 40 μH and R = 3.02 Ω. What should be the value of C of the capacitor for the circuit to be resonant at 800 kHz. What is the bandwidth of the circuit and $\bar{Z}_m$?

Solution

$$\omega_0 = 2\pi \times 800 \times 10^3 \text{ rad/s}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \Rightarrow C = \frac{1}{\omega_0^2 L}$$

Substituting values,

$$C = \frac{1}{(2\pi \times 800 \times 10^3)^2 \times 40 \times 10^{-6}}$$

$$= \frac{10^{-5}}{(2\pi \times 8)^2 \times 4} = 0.99 \text{ nF}$$

Quality factor $Q_0 = \omega_0 \frac{L}{R}$

$$Q_0 = (2\pi \times 800 \times 10^3) \times \frac{40 \times 10^{-6}}{4.02} = 50$$

Bandwidth, $f_b = \frac{f_0}{Q_0} = \frac{800 \times 10^3}{50} = 16 \text{ kHz}$

Example 3.33

In the circuit of Fig. 3.71, G = 5 μ℧, L = 2 mH. It draws a minimum current of 2 mA at a frequency of 5k rad/s.

(a) At what value of C the is voltage V maximum and what is its value?

(b) With the value of C as found in part (a), what should be the value of I for the inductor current to be 1 A?

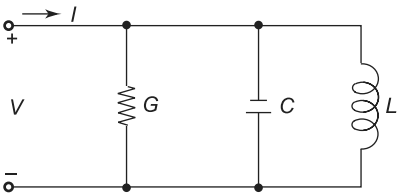


Fig. 3.71

Solution

(a) For V to be maximum, the circuit should be resonant for which

$$\omega_0^2 = \frac{1}{LC} \quad \text{or} \quad C = \frac{1}{\omega_0^2 L}$$

$$C = \frac{1}{(5\times10^3)^2 \times 2 \times 10^{-3}} = 20\ \mu\text{F}$$

Under resonance I flows through G only. So

$$V = \frac{I}{G} = \frac{I}{5\times10^{-6}} = 0.2\times10^6\, I$$

$$V_{(\max)} = \frac{I}{G} = \frac{2\times10^{-3}}{5\times10^{-6}} = 400\ \text{V}$$

$$\omega L = 5\times10^3 \times 2 \times 10^{-3} = 10\ \Omega$$

(b) $$I_L = \frac{V}{\omega L} = \frac{0.2\times10^6\, I}{10} = 1000\ \text{mA};\ (1\ \text{A})$$

$$\therefore \quad I = \frac{10^4}{0.2\times10^6} = 0.05\ \text{mA}$$

Example 3.34

An RLC series circuit has a resonance frequency of 1000 Hz. Its power factor reduces to 0.707 at a frequency of 1050 Hz. Calculate its quality factor.

Solution At half-power frequency, the real and imaginary part of $\bar{Z}_{in}$ of the series circuit are equal. So its power factor is

$$\cos 45^\circ = \frac{1}{\sqrt{2}} = 0.707$$

Thus, ω_2 = 1050 Hz, higher half-power frequency.
Then bandwidth

$$\omega_b = \frac{\omega_0}{Q_0} \qquad \text{or} \qquad Q_0 = \frac{\omega_0}{\omega_b} = \frac{1000}{100} = 10$$

As $\left(\frac{1}{2Q_0}\right)^2 = \left(\frac{1}{20}\right)^2 = 2.5\times10^{-3} << 1$, so it is high-$Q$ circuit and so our assumption is valid.

Example 3.35

An *RLC* series circuit of Fig. 3.72 has a resonant frequency of 200*k* rad/s and a bandwith of 5*k* rad/s. The inductor coil has L = 2.5 mH and a Q of 65. Calculate the value of coil resistance r.

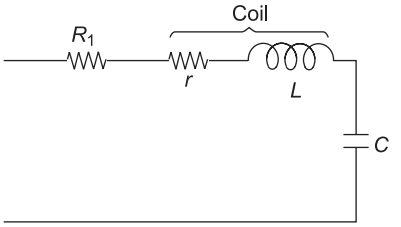


Fig. 3.72

Solution

$$\omega_b = \frac{\omega_0}{Q_0}$$

$$Q_0 = \frac{\omega_0}{\omega_b} = \frac{200}{5} = 40$$

$$Q_0 = \omega_0 \frac{L}{r}$$

$$65 = 200 \times \frac{2.5 \times 10^{-3}}{r}$$

$$r = 7.69 \times 10^{-3}\ \Omega$$

Example 3.36

A capacitor of 12 nF is connected in series with an inductor of 4 mH and 5 Ω resistance as shown in Fig. 3.73.

(a) Calculate the resonant frequency, ω_0.

(b) At ω_0, the voltage across the capacitor is required to be 1.5 V. What voltage should be applied across the circuit input?

(c) Draw a phasor diagram. Show as to how the capacitor voltage can be larger than the input voltage.

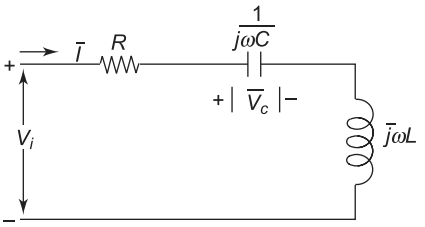


Fig. 3.73

Solution

(a) Resonant frequency

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{4 \times 10^{-3} \times 12 \times 10^{-9}}}$$

or $\omega_0 = 0.144 \times 10^6 = 144$ k rad/s

(b) At ω_0, $V_C = 1.5$ V

$$I = \omega_0 C V_C = 144 \times 10^3 \times 12 \times 10^{-9} \times 1.5$$

$$= 2.592 \text{ mA}$$

At the resonance circuit impedance, $Z_i = R = 5\ \Omega$, (resistive)

$\therefore$ $V_i = RI = 5 \times 2.592 = 12.96$ mV

(c) At ω_0,

$\bar{I}$ is in phase with $\bar{V}_i$

$\bar{V}_C$ lags $\bar{I}$ by 90°

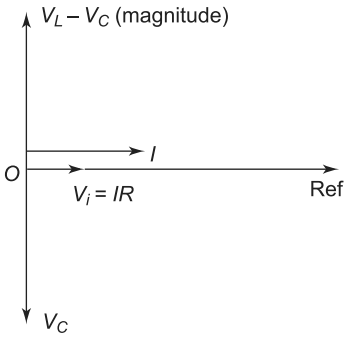


Fig. 3.73(a) *Phasor diagram*

$\bar{V}_L = -\bar{V}_C$ so lead $\bar{I}$ by 90°

Capacitive reactance

$$B_C = \frac{1}{\omega_0 C} = \frac{1}{144 \times 10^3 \times 12 \times 10^{-9}}$$

or $B_C = 579\ \Omega >> 5\ \Omega$

so $V_C >> V_i$

Example 3.37

A parallel resonant circuit is required to have ω_0 = 2.5 MHz, Z_{in} (at ω_0) = 60 kΩ, Q_0 = 80. Determine the value of *R*, *L* and *C*.

Solution

$$\omega_0 = \frac{1}{\sqrt{LC}} = 2.5 \text{ MHz or } 1.57 \text{ M rad/s} \quad \text{(i)}$$

In a parallel *RLC* circuit $Z_i(\omega_0) = R$

$\therefore$ $R = 60\ \text{k}\Omega$ (ii)

$Q_0 = \omega_0 RC$ (iii)

$80 = 13.7 \times 10^6\ 60 \times 10^3\ \text{C}$ (iv)

or $C = 83.9\ \mu\text{F}$ (v)

From Eq. (i),

$$\frac{1}{LC} = (15.7 \times 10^6)^2$$

$$L = \frac{1}{(15.7 \times 106)^2 \times 84.9 \times 10^{-6}} = 478 \text{ nH}$$

$R = 60\ \text{k}\Omega$, C = 83.9 μF, $L = 0.478\ \mu\text{H}$

Example 3.38

A series resonant circuit has a capacitor of 2.5 μF and a resistor of 8 Ω. Its bandwidth is 400 rad/s. Determine (a) *L*, (b) ω_0, (c) Q_0, and (d) ω_1, ω_2.

Solution

(a) Bandwidth, $\omega_b = \frac{\omega_0}{Q_0}$, $Q_0 = \omega_0 \frac{L}{R}$

Then

$$\omega_b = \frac{L}{R} = 400$$

or $L = \frac{8}{400} \times 10^3 = 20 \text{ mH}$

(b) $$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{20 \times 10^{-3} \times 2.5 \times 10^{-6}}}$$

or $\omega_0 = 4.47k$ rad/s

(c) $$Q_0 = \omega_0 \frac{L}{R} = 4.47 \times 10^3 \times \frac{20 \times 10^{-3}}{8}$$

or $Q_0 = 11.2$

(d) It is a high-Q circuit. So $\omega_1, \omega_2 = \omega_0 \mp \frac{1}{2}\omega_b = 4.270$, 4.670 k rad/s

Example 3.39

An *RLC* series circuit hits a resonant frequency of 10^6 rad/s and a bandwidth of 1*k* rad/s. At resonance, an applied voltage of 0.05 V causes a current of 5 = mA to flow. Find

(a) the values of *R*, *L* and *C*,

(b) the voltage across *L* and across *C*; also find the net voltage across *L* and *C*, and

(c) frequencies at which current will reduce by a factor of $\frac{1}{\sqrt{2}}$.

Solution

(a) At resonant frequency, the circuit presents only the resistance *R* as

$$\left(j\omega_0 L - j\frac{1}{\omega_0 C}\right) = 0$$

Thus,

$$R = \frac{0.05}{5 \times 10^{-3}} = 10\ \Omega$$

Bandwidth $\omega_b = \frac{\omega_0}{Q_0}$ or $Q_0 = \frac{\omega_0}{\omega_b} = \frac{10^6}{10^3} = 1000$

Also,

$$Q_0 = \omega_0 \left(\frac{L}{R}\right)$$

or $$L = R\left(\frac{Q_0}{\omega_0}\right) = 10 \times \frac{1000}{10^6} \times 10^3$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

or $$C = \frac{1}{\omega_0^2 L} = \frac{10^{12}}{10^{12} \times 10 \times 10^{-3}}$$

(b) At ω_0, $V_L = V_C = \omega_0 LI = 10^6 \times 10 \times 10^{-3} \times 5 \times 10^{-3} = 50$ V

(c) Current reduction by $\frac{1}{\sqrt{2}}$ occurs at half-power frequencies

$$\omega_1, \omega_2 = 10^6 \mp \frac{1}{2} \times 10^3 = 500 \times 10^3, 1500 \times 10^3 \text{ rad/s}$$

Example 3.40

An *RLC* parallel circuit has R = 1 MΩ, L = 1 H, and C = 1 μF. It is excited by a current $\bar{I} = 10 < 0°$ μA. Find the ω_0 and Q_0. If the frequency of current $\bar{I}$ is ω_0, find the voltage across the circuit. At what frequencies would the voltage reduces by a factor of $\frac{1}{\sqrt{2}}$?

Solution

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{1 \times 1 \times 10^{-6}}} = 1000 \text{ rad/s}$$

At resonance, current $\bar{I}$ flows only through R. Therefore, circuit voltage is

$$\bar{V} = 1 \times 10^6 \times 10 \times 10^{-6} \angle 0° = 10 \angle 0 \text{ V}$$

The voltage will reduce by a factor of $\frac{1}{\sqrt{2}}$ at half-power frequencies, so we must find the bandwidth.

$$Q_0 = \omega_0 RC$$

$$\omega_b = \frac{\omega_0}{Q_0} = \frac{1}{RC} = 1 \text{ rad/s}$$

Then

$$\omega_1, \omega_2 = \omega_0 \mp \frac{1}{2}\omega_b$$

$$= 1000 \mp 0.5 = 999.5, 1000.5 \text{ rad/s}$$

Example 3.41

A constant voltage of 1 MHz frequency is connected across an inductor (r in series with L) in series with a variable capacitor. The circuit draws maximum current when the capacitance is 500 pF. The current reduces by a factor $\frac{1}{\sqrt{2}}$ when the capacitor is adjusted to 450 pF. Determine r, L and Q_0. Given L = 10 mH and C = 1 nF.

Solution The circuit is drawn in Fig. 3.74.

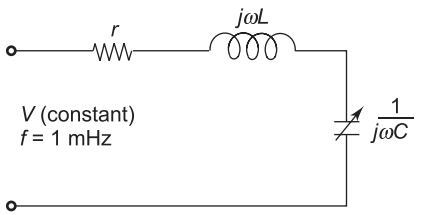


Fig. 3.74

Case 1 C = 500 pF

The current drawn is maximum at 1 MHz. Therefore, resonant frequency is 1 MHz.

$$\omega_0^2 = \frac{1}{LC}$$

$$L = \frac{1}{\omega_0^2 C} = \frac{10^3}{(2\pi \times 10^6)^2 \times 500 \times 10^{-12}}$$

$$= 0.0633 \text{ mH}$$

Case 2 C = 450 pF

Resonant frequency of the circuit is now

$$(2\pi f_0')^2 = \frac{1}{LC} = \frac{1}{0.0633 \times 10^{-3} \times 450 \times 10^{-12}}$$

$$\omega_0' = 2\pi f_0' = 3.925 \times 10^6 \text{ rad/s}$$

$$f_0' = 0.943 \text{ MHz}$$

Summary

- Between two sinusoidal waveforms of the same frequency, it is possible to determine the phase angle difference and which one is leading or lagging. All we need to do is to find the angle between consecutive corresponding points, say positive peaks.
- The forced response of a circuit to sinusoidal voltage or current is a single sinusoid of the same frequency as the forcing function.
- A sinusoidal function can be transformed to a phasor.
- A phasor can only have magnitude and angle, the frequency is to be recorded separately.
- Time-domain description of a circuit can be transformed to frequency-domain form wherein voltage/current source become phasors, capacitors and inductors take the form of impedance (or admittance), which are complex numbers.
- Resistance transforms to resistance.
  Capacitance transforms to capacitive reactance $1/j\omega C$.
  Inductance transforms to capacitive reactance $j\omega L$.
  Combination of resistances and reactance contribute impedance (or its inverse admittance).
- All the analysis techniques and theorems of resistive circuits apply to frequency-domain circuits.
- Phasor analysis can be used only for circuits wherein all sources have the same frequencies.
- Condition for maximum power transfer is $\bar{Z}_L = \bar{Z}_{TH}^*$.
- Complex power is $\bar{S} = P + jQ$; Q is positive for lagging pf and negative for leading pf. The unit of P is watt (W), Q is volt-ampere reactive (VAR) and S is volt-ampere (VA).
- Power Factor = $\dfrac{\text{Real power}}{\text{Apparent power}}$ of a load lagging/leading

  = cos θ, θ = angle between voltage across load and current drawn by load
- Capacitors in shunt across load are employed to improve the combined pf, thereby reducing reactive power demand and power supply.
- Resonance is a condition in which a circuit, when excited by fixed amplitude sinusoidal voltage/current, produces maximum amplitude current/voltage response.
- An electrical network (circuit) is in resonance when voltage and current at its input are in phase, that is, the power factor is unity.
- The quality factor (Q) of a network is proportional to the maximum energy stored divided by the energy lost per cycle.
- At half-power frequency, the circuit response amplitude reduces to $\dfrac{1}{\sqrt{2}}$ of its maximum value.
- The bandwidth of a resonant circuit is the difference between upper and lower half-power frequencies.

- ➢ In a high-*Q* resonant circuit, the resonant frequency is the mid-frequency of the bandwidth.
- ➢ At resonant frequency, the admittance of a series circuit is maximum and the impedance of a parallel circuit is maximum.

Exercises

Review Questions

1. Explain the meaning of steady-state sinusoidal response of a circuit.
2. Distinguish between time and frequency-domain relationship. Take the example of an *RL* series circuit excited by sinusoidal current.
3. What is a phasor? How does the phasor concept help in addition and subtraction of sinusoidal quantities? Use a two-term expression as an example.
4. How does the sinusoidal response of a circuit differ from the excitation (voltage or current)?
5. Explain what is impedance. What role does it play in phasor diagrams?
6. Distinguish between a phasor and a complex quantity.
7. Can you carry out the following addition using the phasor method?
   $20 \cos (200t + 30°) + 10 \sin (100t - 60°)$
8. Draw the phasor diagram to find
   $\bar{V} = 10 \angle 0° + 10 \angle 60° - 10\sqrt{3} \angle 30°$
9. From the given circuit (Fig. 3.75), determine the expression for forced response.
10. Convert $\bar{I} = 20 \angle 60°, f = 400$ Hz to time-domain form.
11. Voltage $\bar{V} = 100 \angle 30° \text{ V}$ is applied across two terminals of a circuit, which draws current $\bar{I} = 10 \angle -30° \text{ A}$. Is the impedance seen from the terminals inductive or capacitive?
12. Explain the meaning and significance of the power factor of a circuit.

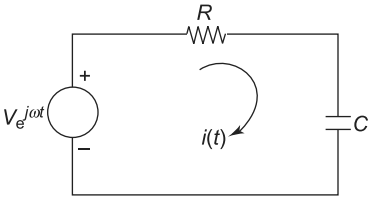


Fig. 3.75

13. A sinusoidally excited circuit is applied a voltage *V*(rms). The circuit draws current *I* leading the voltage by an angle θ. What are the reactive volt-amperes (VAR) drawn by the circuit and its sign?
14. A capacitor *C* is connected across *R* in series with inductor *L*. The admittance of this parallel circuit is $\bar{Y} = G + jB$. Write the expression for *G*.
15. For the adjoining circuit (Fig. 3.76), write the expression for complex power in terms of the current $\bar{I}$.
16. What is the sign convention for reactive power?
17. How does a capacitor in-shunt across a lagging pf load, improve its power factor? Can the combined pf be made unity?
18. Write the expression for power factor for complex power $\bar{S} = P + jQ$. When it will be lagging/leading?
19. A load draws real power *P* at pf = cos θ. Write the expression for reactive power *Q* of the load.

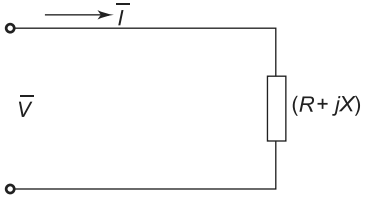


Fig. 3.76

20. What are the two kinds of simple resonant circuits?
21. Sketch the variation of impedance/admittance with frequency in *RLC* series and parallel resonant circuits.
22. Explain what is meant by resonance in electrical circuits (simple circuits).

23. What is the power factor of an *RLC* parallel circuit at resonant frequency? Explain the reason.
24. Repeat Question 4 for *RLC* series circuit.
25. In an *RLC* parallel circuit, the input current is $i(t) = I_m \cos \omega_0 t$; ω_0 = resonant frequency. Write the expression for the circuit voltage.
26. In an *RLC* series circuit, the applied voltage is $v(t) = V_m \cos \omega_0 t$; ω_0 = resonant frequency. Write the expression for the circuit current.
27. Explain what is quality factor and what is its significance. How does it affect the circuit bandwidth?
28. Under what condition is the resonant frequency mid-way between the bandwidth?
29. What is the circulating current in an *RLC* parallel resonant circuit?
30. In an *RLC* series circuit, the net voltage across *L* and *C* at resonant frequency is zero. Explain.
31. Write the expression for quality factor Q_0 at resonant frequency for series and parallel resonant circuits.
32. What is meant by half-power frequency of a resonant circuit? Is there one or two such frequencies?
33. Cite a practical application of a parallel resonant circuit.

Problems

1. An iron-cored choking coil has the circuit equivalent of a series resistance of 5 Ω (which represents the iron loss of the coil) and an unknown inductance *L*. It draws a current of 10 A on applied voltage of 240 V, 50 Hz. Find (a) coil inductance, (b) iron loss, and (c) pf of the coil.
2. A coil of resistance 8 Ω and inductance 0.1 H is connected in series with a condenser of capacitance 160 μF across 230 V, 50 Hz supply. Calculate (a) the inductive reactance (b) the capacitive reactance (c) the circuit impedance, current and pf, and (d) the coil and condenser voltages respectively.
3. A resistance of 6 Ω is connected in series with an iron-cored choke coil (*r* in series with *L*). The circuit draws a current of 5 A at 240 V, 50 Hz. The voltage across resistance is 120 V and across the coil is 200 V. Calculate (a) resistance, reactance and impedance of the coil, (b) the power absorbed by the coil, and (c) the overall pf.
4. The series circuit of Fig. 3.77 carries a current of 35 A. Find the values of *R*, *r* and *L* and the frequency of the applied voltage and its magnitude.

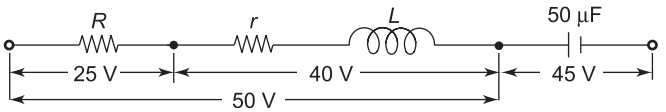


Fig. 3.77

5. The average power drawn by the load in Fig. 3.78 is 250 kW at 0.707 lagging pf. The generator voltage is $v(t) = 2300\sqrt{2} \sin 314\, t$. Find the value of *C* such that the resultant power factor (load and cap) is 0.866 lagging.

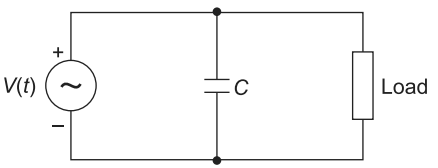


Fig. 3.78

6. For the circuit of Fig. 3.79, find the value of R and the pf of the circuit.

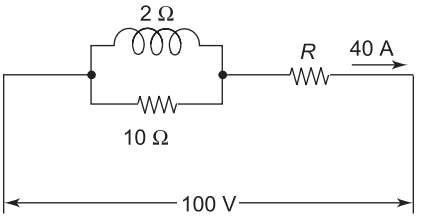


Fig. 3.79

7. For the circuit of Fig. 3.80, find the value of V and the circuit pf.

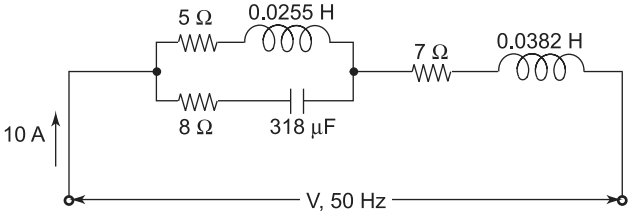


Fig. 3.80

8. For the circuit of Fig. 3.81,

$$v_s = 4 \cos 2t$$

(a) Determine $\overline{I}_L$.

(b) Determine the value of C such that $\overline{I}_S$ and $\overline{V}_S$ are in phase.

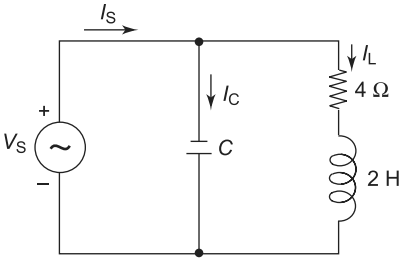


Fig. 3.81

9. For the circuit of Fig. 3.82,

$$v_t(t) = \sqrt{2} \sin \omega t$$

(a) Determine $\overline{V}_1 / \overline{V}_2 (j\omega)$.

(b) Given $\omega = 2$, determine $v_2(t)$.

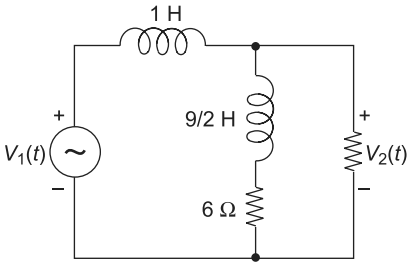


Fig. 3.82

10. For the circuit of Fig. 3.83,

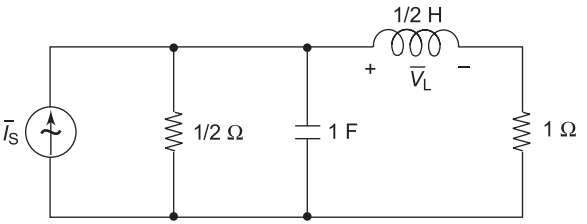


Fig. 3.83

$$v_L = \sqrt{2}\cos 2t \quad \text{or} \quad \bar{V}_L = 1\angle 0°$$

(a) Obtain the current and voltage phasors in all the elements and $\bar{I}_S$.
(b) Write an expression for $i_s(t)$.
(c) Obtain the complex power of the source $\bar{I}_S$.
(d) Obtain the power absorbed by the resistors.

11. For the circuit of Fig. 3.84,

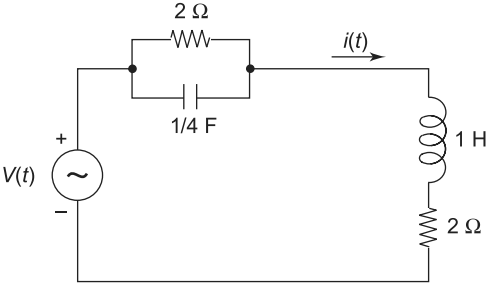


Fig. 3.84

$$i(t) = \sqrt{2}\cos 2t$$

Find $v(t)$ using phasor diagram.

12. For the circuit of Fig. 3.85, find $v(t)$. Hence, determine the average power drawn from the source.

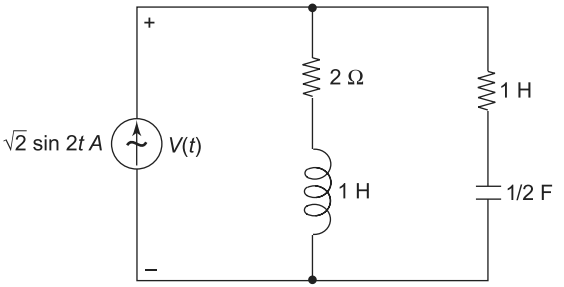


Fig. 3.85

13. For the circuit of Fig. 3.86, find voltages $\overline{V}_1$ and $\overline{V}_2$.

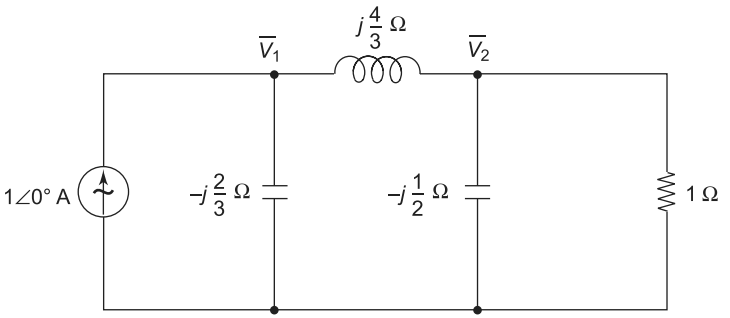


Fig. 3.86

14. For the circuit shown in Fig. 3.87,

$$i_L(t) = \sqrt{2}\cos 2t$$

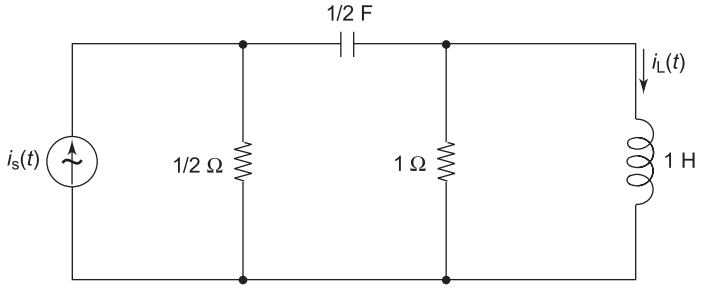


Fig. 3.87

(a) Construct a phasor diagram showing currents and voltages in all the elements and $\overline{I}_s$.
(b) Determine the complex power supplied by the source.
(c) Determine the complex power for each passive element. Also, show that the average real power drawn from the source equals the sum of the average power absorbed by the resistive elements.

15. For the circuit of Fig. 3.88, find voltage V_{AB} using the mesh method of analysis.

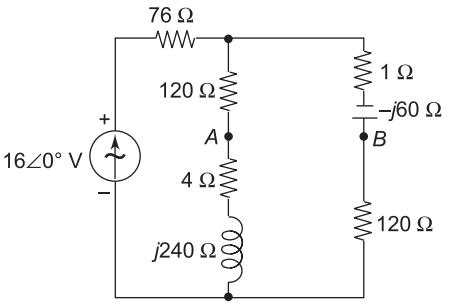


Fig. 3.88

16. For the circuit of Fig. 3.89, calculate the complex power absorbed by the load $(4 + j6)\ 0\ \Omega$ by finding first the Thevenin equivalent of the circuit to the left of *AB*.

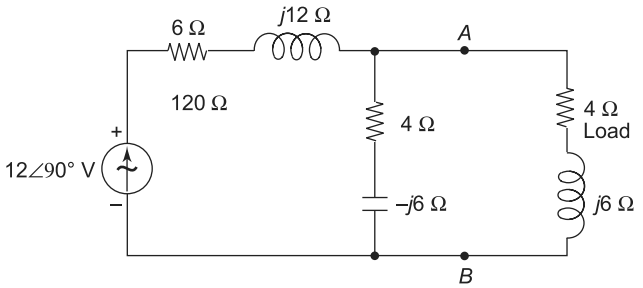


Fig. 3.89

17. For the lag and lead networks shown in Fig. 3.90(a) and (b) respectively, find

$$\bar{H}(j\omega) = \frac{\bar{V}_2(j\omega)}{\bar{V}_1(j\omega)}$$

This is called the *transfer function*.

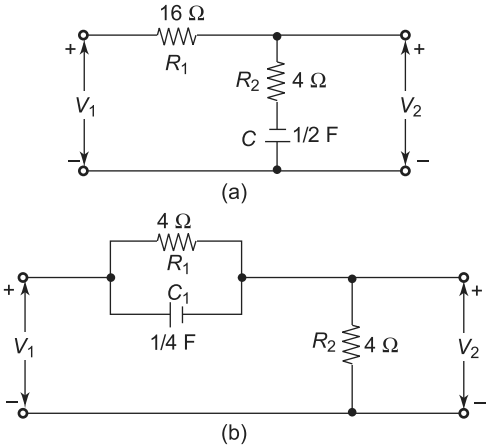


Fig. 3.90 *(a) Lag network and (b) lead network*

18. For the network of Fig. 3.91, find $\bar{H}(j\omega) = \bar{V}_2(j\omega/\bar{V}_1(j\omega)$.

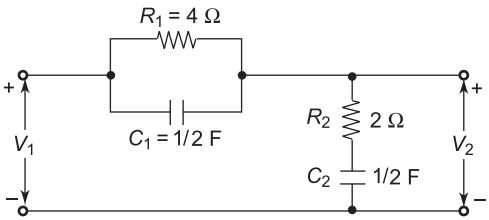


Fig. 3.91

19. A constant voltage of 1 MHz frequency is applied to an inductor (r in series with L) in series with a variable capacitor. The current drawn is maximum when the capacitor is set to 400 pF; while the current is reduced to $1/\sqrt{2}$ of that when the capacitance is 450 pF. Find the values of r, L and Q.
20. A resistor and a capacitor are in series with a variable inductor. When the circuit is connected to 230 V, 50 Hz mains, the maximum current obtained by varying the inductor is 0.35 A, the voltage across capacitor being 300 V. Calculate the circuit constants.
21. A coil of inductance 7.5 H and resistance 40 Ω in series with a condenser is fed from a constant voltage variable frequency source. The maximum current is 1.2 A at 100 Hz. Find the frequency when the current is 0.848 A.
22. For the parallel circuit shown in Fig. 3.92, determine i_R, i_L and i_c. Draw the phasor diagram indicating all currents and voltages.

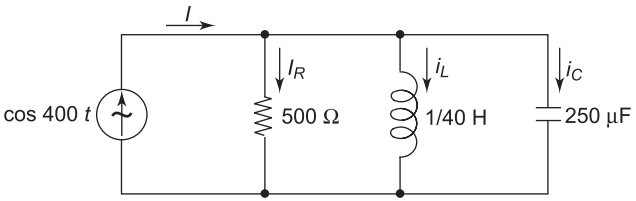


Fig. 3.92

23. For the circuit of Fig. 3.93, show that the circulating current is $V\sqrt{C/L}$, provided R is small where V is the applied voltage. Given L = 10 mH, R = 1 Ω and C = 104 pF, find the current input to the parallel circuit at (a) resonant frequency, and (b) at 90% of resonant frequency.

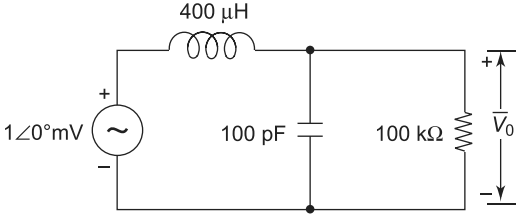


Fig. 3.93

24. For the circuit shown in Fig. 3.93, find ω_0 and Q_0 at ω_0.

25. A parallel resonant circuit has $R = 60$ kΩ, $L = 5$ mH and $C = 50$ pF. Determine f_0, Q_0 and the bandwidth in Hz.
26. A coil of 15 Ω resistance and inductance 0.75 H is connected in series with a condenser.
    The combination draws maximum current when a fixed amplitude sinusoidal voltage of 50 Hz is applied. A second condenser is now connected in parallel with this circuit. What should be its capacitance for the combined circuit to act as a non-inductive resistance at 100 Hz? Calculate the current drawn by the combined circuit if the applied voltage is 200 V.

Multiple-Choice Questions

1. The current i through the inductance of Fig. 3.94 is given by

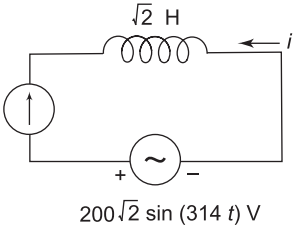


Fig. 3.94

(a) (200/313) cos (314t) (b) –(200/314), cos (314t)
(c) 200×314 sin (314t) (d) -200×314 sin (314t)

2. The phasor current through an impedance is 1 $\angle 0°$V and the voltage across it is 2 $\angle 60°$V. The reactive power in VARs consumed in the impedance is

(a) $j\sqrt{3/2}$ (b) $-j\sqrt{3/2}$
(c) $j\sqrt{3}$ (d) $-j\sqrt{3}$

3. A Capacitor of $1/2\pi f$ is connected in series with a 1 r resistance to a voltage source 1 V, 2 P HZ, the voltage drop across the capacitance would be

(a) 2 V, leading applied voltage by 45° (b) $1/\sqrt{2}$ V, lagging applied voltage by 45°
(c) $1/\sqrt{2}$ V, leading applied voltage by 45° (d) $\sqrt{2}$ V, lagging applied voltage by 90°

4. For the circuit shown in Fig. 3.95, $i_s = 5 \cos 2t$, the phasor current I_L through the inductance is given by

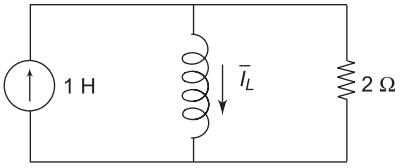


Fig. 3.95

(a) $(5\sqrt{2}) \angle -45°$ (b) $(5\sqrt{2}) \angle -45°$
(c) $(5\sqrt{2}) \angle 45°$ (d) $(5\sqrt{2}) \angle -45°$

5. In Fig 3.96, $V_S = 5\sqrt{2}$ cost. The complex power drawn by the circuit is (3/2 + *j*2). The values of R and L respectively are

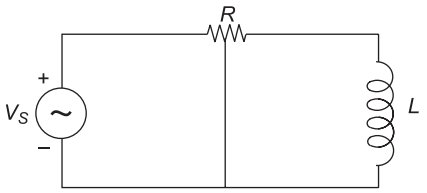


Fig. 3.96

(a) 6, 8 (b) $6/\sqrt{2}, 8/\sqrt{2}$

(c) 3, 4 (d) 3/5, 4/5

6. A resistance of 1*r* is connected in series with an inductance 1 H, if a 1 A (rms) sinusoidal current ($1/2\pi$ Hz) is passed through the circuit, the rms voltage across the circuit would be

(a) $\sqrt{2}$ (b) 2 (c) 1 (d) 2π

7. A resistance of 1 *r* is connected is parallel to an inductance of 1 H and the circuit excited from 1 V, $1/2\ \pi$ Hz source, the current drawn by the circuit is

(a) 1A, lagging the voltage by 90° (b) 1A lagging the voltage by 45°

(c) $\sqrt{2}$ A , lagging the voltage by 90° (d) $\sqrt{2}$ A , lagging the voltage by 45°

Answers

Multiple-Choice Questions

1. a 2. d 3. b 4. d 5. a 6. a 7. d

Three-Phase Circuits

chapter 4

Goals & Objectives

- Polyphase systems
- Three-phase circuits

4.1 INTRODUCTION

Most generation, transmission and large-power utilisation is accomplished by means of polyphase systems which have several sources equal in magnitude but with a progressive difference of $2\pi/q$, where q is the number of phases (for $q = 2$, phase difference is $\pi/2$). Such systems have distinct economic and operational advantages over a single-phase system. To avoid undue complexity, a three-phase system is almost universally adopted.

4.2 THREE-PHASE VOLTAGES AND CURRENTS

A set of three sinusoidal voltages (or currents) that are equal in magnitude but have a progressive phase difference of $2\pi/3$ (120°) constitute a balanced three-phase voltage (or current) system. The three-phase quantities (voltages/currents) are otherwise said to be unbalanced. Three voltage sources forming a *balanced three-phase system* are shown in Fig. 4.1(a). In instantaneous form, these voltages (known as phase voltages) are expressed as

$$v_{aa'} = \sqrt{2}\, V_p \sin \omega t \tag{4.1a}$$

$$v_{bb'} = \sqrt{2}\, V_p \sin (\omega t - 120°) \tag{4.1b}$$

$$v_{cc'} = \sqrt{2}\, V_p \sin (\omega t - 240°) \tag{4.1c}$$

where V_p = rms amplitudes of phase voltage.

The waveform of the three-phase voltages is drawn in Fig. 4.1(b).

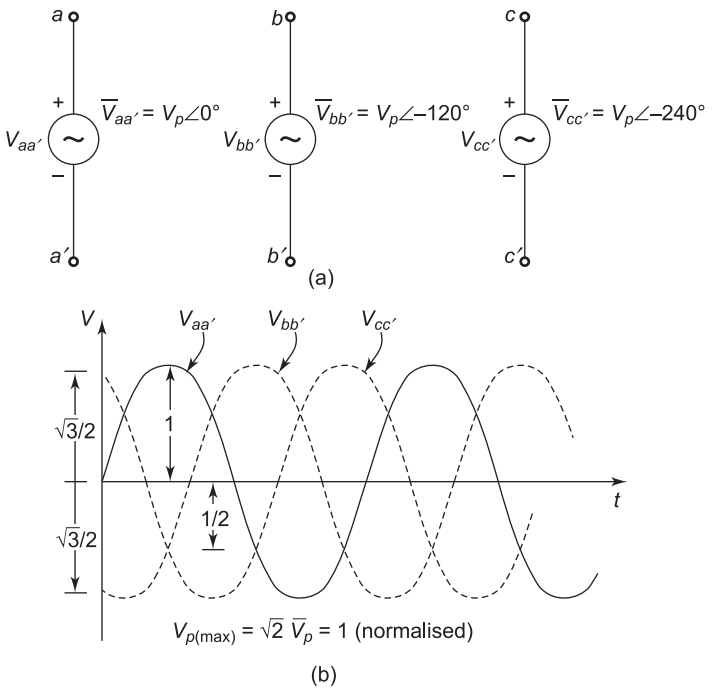


Fig. 4.1 *Balanced three-phase system: (a) Three-phase voltage sources (b) Voltage waveform of three-phase sources*

In phasor form, Eq. (4.1) can be written as

$$\bar{V}_{aa'} = V_p \angle 0° \tag{4.2a}$$

$$\bar{V}_{bb'} = V_p \angle -120° \tag{4.2b}$$

$$\bar{V}_{cc'} = V_p \angle -240° \tag{4.2c}$$

The phasor diagram of the three voltages is drawn in Fig. 4.2(a) where for convenience we may write $\bar{V}_{aa'}$, as $\bar{V}_a$-phase *a*, $\bar{V}_{bb'}$ as $\bar{V}_b$-phase *b* and $\bar{V}_{cc'}$, as $\bar{V}_c$-phase *c*.

Consider now the instantaneous voltage sum

$$v_{aa'} + v_{bb'} + v_{cc'} = \sqrt{2}V[\sin\omega t + \sin(\omega t - 120°) + \sin(\omega t - 240°)] = 0 \tag{4.3}$$

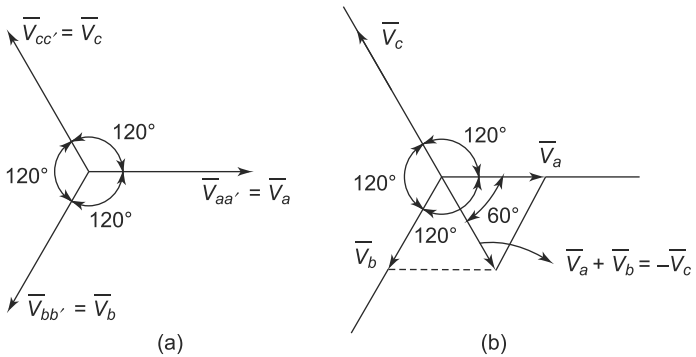


Fig. 4.2 *Phasor diagram of balanced three-phase voltages*

It is immediately seen that the sum of balanced three-phase voltages (or currents) is zero at all times. In phasor form,

$$\bar{V}_{aa'} + \bar{V}_{bb'} + \bar{V}_{cc'} = 0 \tag{4.4}$$

This is verified from the phasor diagram of Fig. 4.2(b).

Phase Sequence

In the balanced three-phase voltages presented above in phasor form [Eqs. (4.2)] and in phasor diagram of Fig. 4.2, phase '*a*' leads phase '*b*', which then leads phase '*c*' by 120°. This is known as *positive phase sequence abc*. The negative phase sequence is *cba* wherein

$$\begin{aligned} \bar{V}_a &= V_p \angle 0° \\ \bar{V}_b &= V_p \angle 120° \\ \bar{V}_c &= V_p \angle 240° \end{aligned} \tag{4.5}$$

The phasor diagrams for both the phase sequences are drawn in Fig. 4.3 (a) and (b) for comparison.

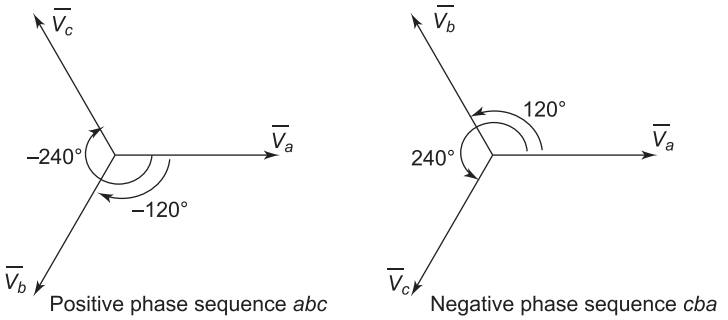


Fig. 4.3

In actual physical system, the phase sequence depends on arbitrary[1] labelling of the terminals as *a*, *b* and *c*. We shall assume in our study the positive phase sequence.

4.3 STAR (Y) CONNECTION

Both three-phase source and load can be star connected. This source-load connection is labelled as Y-Y connection.

4.3.1 Star (Y) Connected Source

In this connection, the similar polarity ends (say a', b', c') of the three-phase voltage sources of Fig. 4.1(a) are joined together to form the *neutral point* and three leads are taken out from the other ends and one lead from the neutral as shown in Fig. 4.4.

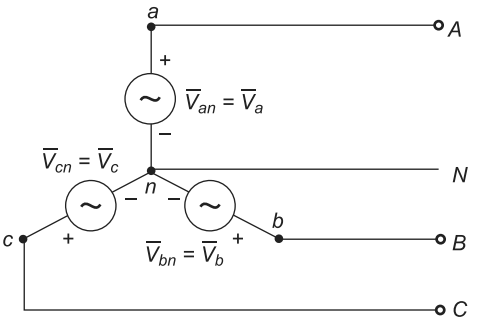


Fig. 4.4 *Star connection*

4.3.2 Line-to-Line Voltages

These are commonly referred to as line voltages. The phasor diagram showing phase and line voltages is drawn in Fig. 4.5 from the star connection of Fig. 4.4.

The voltage between lines *a* and *b* (or *A* and *B*) is

$$\overline{V}_{ab} = \overline{V}_{an} - \overline{V}_{bn} \tag{4.6}$$

[1] But this should be consistent through and the power system.

It immediately follows from the phasor diagram of Fig. 4.5 that

$$\overline{V}_{ab} = \sqrt{3}\,\overline{V}_{an}\ \angle 30^\circ \text{ ; reference phase '}a\text{'}$$

$$= \sqrt{3}\,\overline{V}_P\ \angle 30^\circ \tag{4.6a}$$

Similarly,

$$\overline{V}_{bc} = \overline{V}_{bn} - \overline{V}_{cn}$$

$$= \sqrt{3}\,\overline{V}_{bn}\ \angle 30^\circ$$

$$= \sqrt{3}\,V_p\ \angle -90^\circ] \text{ ; reference phase '}a\text{'} \tag{4.7}$$

and

$$\overline{V}_{ca} = \overline{V}_{cn} - \overline{V}_{an}$$

$$= \sqrt{3}\,\overline{V}_{cn}\ \angle 30^\circ$$

$$= \sqrt{3}\,V_p\ \angle -210^\circ \text{ ; reference phase '}a\text{'} \tag{4.8}$$

It is seen from the phasor diagram of Fig. 4.5 that for balanced phase voltages,

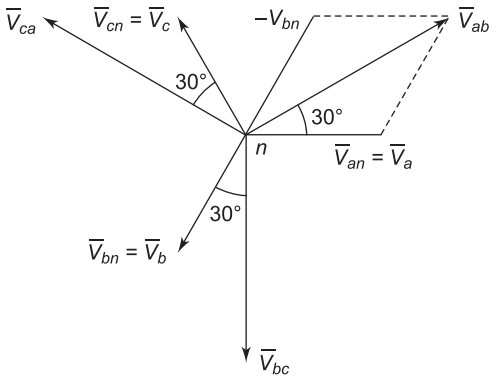


Fig. 4.5 *Phase and line voltages in star connection*

line voltages also form a balanced set advanced in phase by 30° from the phase voltages. In terms of magnitude,

$$V(\text{line-to-line}) = \sqrt{3}\,V(\text{phase})$$

or

$$V_L = \sqrt{3}\,V_p \tag{4.9}$$

Sum of the voltage phasors

$$\overline{V}_{ab} + \overline{V}_{bc} + \overline{V}_{ca} = 0$$

4.3.3 Star-connected Source Feeding Star-connected Load

Consider now a balanced 3-phase load connected in star fed from a balanced 3-phase star-connected source through 3 lines and a neutral connection as shown in Fig. 4.6. It is to be noted that a balanced load means that each of the three *phase impedances* $(\overline{Z}_p)$ are equal.

It is to be recorded here.

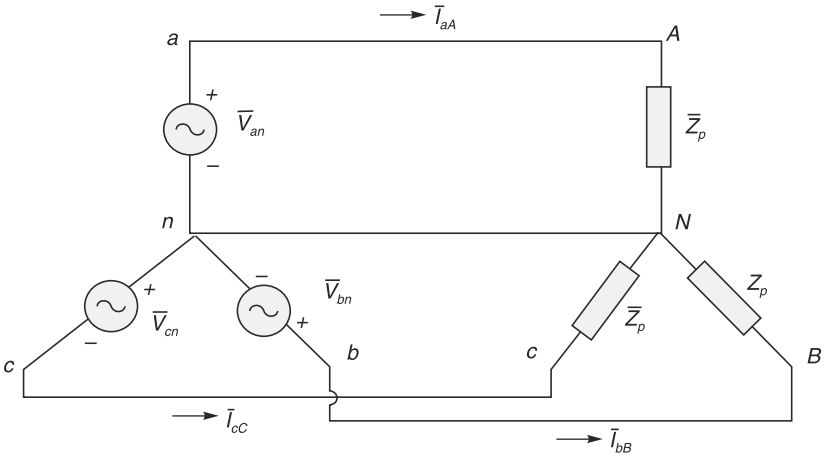


Fig. 4.6 *Balanced star-connected source feeding balanced star-connected load*

that the connecting lines have zero impedance

From the loop *na AN*, the line current

$$\bar{I}_{aA} = \frac{\bar{V}_{an}}{\bar{Z}_p} = \frac{V_{an}}{Z_p} \angle 0° \tag{4.10}$$

Similarly, $$\bar{I}_{bB} = \frac{\bar{V}_{bn}}{\bar{Z}_p} = \left(\frac{V_{an}}{Z_p}\right) \angle -120°$$

and $$\bar{I}_{cC} = \frac{\bar{V}_{cn}}{\bar{Z}_p} = \left(\frac{V_{an}}{Z_p}\right) \angle -240°$$

We thus find that the line currents form a balanced set. Therefore,

$$\bar{I}_{aA} + \bar{I}_{bB} + \bar{I}_{cC} = 0 \tag{4.11}$$

As the sum of the three line currents is zero, no current flows in the neutral connection. The source and load neutrals need not be connected; neutral nodes *n* and *N* have the same potential.

It is seen from the stat-star connection that the phase and line currents are identical, i.e.

$$I(\text{line}) = I(\text{phase})$$

or $$I_L = I_P \tag{4.12}$$

The phasor diagram showing phase voltages and line current is drawn in Fig. 4.7. Each line current differs in phase from corresponding phase voltage of the impedance angle $\theta = \angle \bar{Z}_p$.

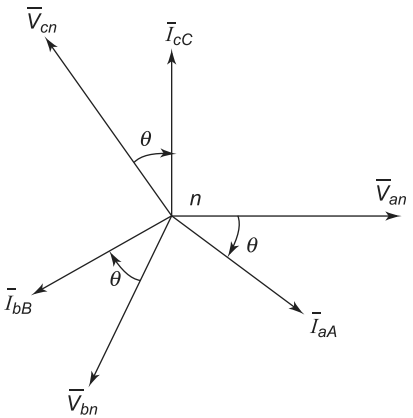


Fig. 4.7 *Phasor diagram of balanced star-star connection*

Power Factor

In a balanced source-load system, the power factor cos θ is the same for each phase. It is commonly referred to as the system power factor.

Example 4.1

For the balanced star-star connection of Fig. 4.6, the source phase voltage is 200 V and load impedance is 100 < 60° Ω. Calculate all the phase voltages, line voltages and time currents in phasor form.

Solution Phase voltages

$$\bar{V}_{an} = 200\angle 0°\,\text{V}\,,\ \bar{V}_{bn} = 200\angle -120°\,,\ \bar{V}_{cn} = 200\angle -240°$$

Line currents

$$I_L = I_P = \frac{200}{100} = 2\text{A}$$

Phase angle = θ = –60°

$$\bar{I}_{aA} = 2\angle -60°\,A, \bar{I}_{bB} = 2\angle -120° - 60° = 2\angle -180°\,\text{A}$$

The reader is advised to draw a complete phasor diagram.

4.4 DELTA (Δ) CONNECTION

A balanced star-connected source, feeding a balanced delta-connected load is sketched in Fig. 4.8.

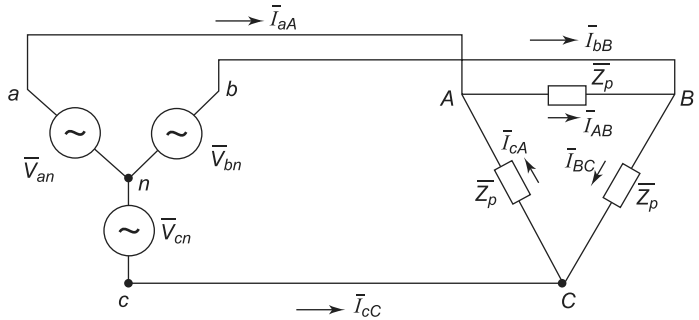


Fig. 4.8 *Star-connected source feeding delta-connected load*

It is immediately observed that no neutral connection is possible.
Voltage applied across each delta phase is the line voltage, i.e.

$$V(\text{line}) = V(\text{phase }\Delta)$$

or
$$V_L = V_p \tag{4.12}$$

The delta phase currents are expressed as

$$I_{AB} = \frac{\bar{V}_{ab}}{Z_p},\ \bar{I}_{BC} = \frac{\bar{V}_{bc}}{\bar{Z}_p},\ \bar{I}_{CA} = \frac{\bar{V}_{ca}}{\bar{Z}_p} \tag{4.13}$$

As the delta voltages are a balanced three-phase set, the delta phase currents also form a balanced set except that these differ by the phase angle $\theta = \angle \overline{Z}_p$.

The line currents are flowing to delta terminals (A, B, C) and are found by applying *KCL* at each node. Thus,

$$\begin{aligned} \overline{I}_{aA} &= \overline{I}_{AB} - \overline{I}_{CA} \\ \overline{I}_{bB} &= \overline{I}_{BC} - \overline{I}_{AB} \\ \overline{I}_{cC} &= \overline{I}_{CA} - \overline{I}_{BC} \end{aligned} \tag{4.14}$$

As we know from the phase and line relationship of balanced voltages, the phase and line delta currents are related as

$$I_L = \sqrt{3} I_p \tag{4.15}$$

The phase relationship is that the line currents lag in phase by 30° from the phase currents.

The above delta relationships are clarified by the phasor diagram of Fig. 4.9.

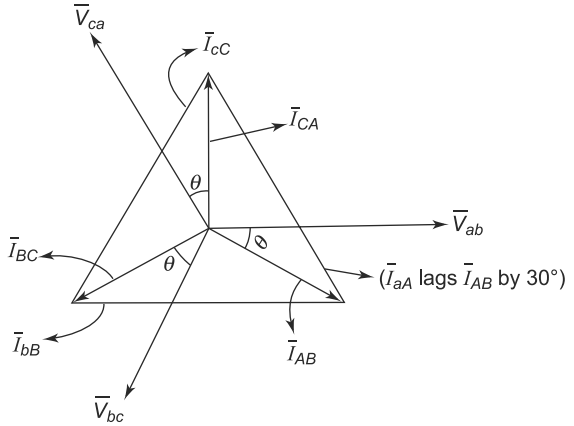


Fig. 4.9 *Phasor diagram of delta load voltages and currents*

Power Factor

It is cos θ, where θ is the angle between line voltage and corresponding phase current. Also as said, already $\theta = \angle \overline{Z}_p$.

Example 4.2

A three-phase power system with a line voltage of 400 V is supplying a delta-connected load of 1500 W at 0.8 pf lagging. Determine the phase and line currents and also the phase impedance.

Solution The circuit diagram of the power system is drawn in Fig. 4.10.

It is a balanced three-phase system. So each load phase draws one-third power. Thus,

$$P(\text{phase}) = \frac{1500}{3} = 500\,\text{W}$$

But $$P = V_p I_p \cos\theta$$

For delta connection,

$$V_p = V_L = 400 \text{ V}$$

or pf, $\cos\theta = 0.8$ lag

Substituting values

$$500 = 400 I_p \times 0.8$$

or $$I_p = 1.56 \text{ A}$$

In delta connection,

$$I_L = \sqrt{3}\, I_p = 1.56\sqrt{3}$$

$$= 2.70 \text{ A}$$

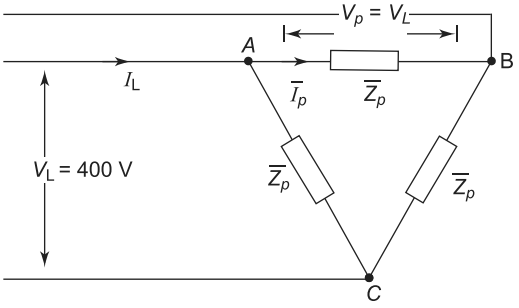


Fig. 4.10

Now,

pf angle $\theta = \cos^{-1} 0.8 = 36.9°$ lag

Therefore,

$$\bar{I}_p = 2.70 \angle -36.9°$$

Then

$$\bar{Z}_p = \frac{\bar{V}_p}{\bar{I}_p} = \frac{400 \angle 0°}{2.70 \angle -36.9°}$$

or $$\bar{Z}_p = 256 \angle 36.9° \ \Omega$$

The circuit diagram is drawn here for tutorial purpose, otherwise it is not necessary.

Example 4.3

A three-phase system supplies 1200 W to a star-connected load at 0.8 pf lagging. Determine the amplitude of line and phase current and $\bar{Z}_p$, the phase impedance.

Solution The circuit diagram is drawn in Fig. 4.11.

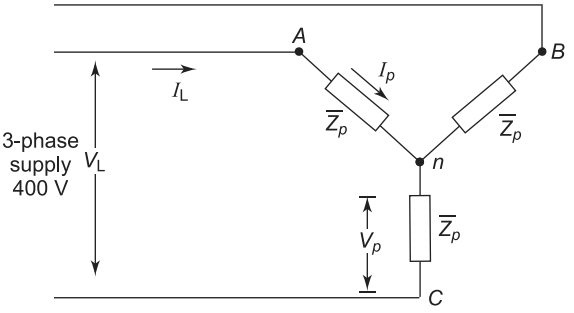


Fig. 4.11

Power drawn by each phase

$$P(\text{phase}) = \frac{1200}{3} = 400 \text{ W}$$

In star-connection

$$V_p = \frac{V_L}{\sqrt{3}} = \frac{400}{\sqrt{3}} = 231\text{V}$$

$$I_L = I_p$$

$$P(\text{phase}) = V_p I_p \cos\theta$$

$$400 = 231 \times I_p\, 0.8$$

or $I_p = 2.16$ A, $\theta = 36.9°$ lag

so $I_L = 2.16$ A

Phasor impedance

$$\bar{Z}_p = \frac{\bar{V}_p}{I_p} = \frac{231}{2.16 \angle -36.9°}$$

or $\bar{Z}_p = 106.9 \angle 36.9° \ \Omega$

It is not necessary to draw the circuit diagram. It is drawn here for tutorial purpose.

Δ-connected Source

In practice, the source is *not delta connected* as even a slight unbalance of source voltages causes of the sum of delta voltages to be nonzero. Even a small delta loop voltage causes a large circulating current as the impedances of the three phases is very small. This causes undesirable power loss in the loop and reduces the capacity of delta source to supply load current.

4.5 THREE-PHASE POWER

Phase voltages and currents in a balanced three-phase circuit (star or delta) can be written in the instantaneous form as

$$v_a = \sqrt{2}\, V_p \sin\omega t \tag{4.16a}$$

$$v_b = \sqrt{2}\, V_p \sin(\omega t - 120°) \tag{4.16b}$$

$$v_c = \sqrt{2}\, V_p \sin(\omega t - 240°) \tag{4.16c}$$

and

$$i_a = \sqrt{2}\, I_p \sin(\omega t - \theta) \tag{4.17a}$$

$$i_b = \sqrt{2}\, I_p \sin(\omega t - \theta - 120°) \tag{4.17b}$$

$$i_c = \sqrt{2}\, I_p \sin(\omega t - \theta - 240°) \tag{4.17c}$$

where θ = phase angle between phase voltage and current pair.

The instantaneous power in each phase is

$$p_a = v_a i_a = V_p I_p [\cos\theta - \cos(2\omega t - \theta)] \tag{4.18a}$$

$$p_b = v_b i_b = V_p I_p [\cos\theta - \cos(2\omega t - \theta - 240°)] \tag{4.18b}$$

$$p_c = v_c i_c = V_p I_p [\cos\theta - \cos(2\omega t - \theta - 480°)] \tag{4.18c}$$

The total instantaneous three-phase power is

$$\mathcal{P} = p_a + p_b = p_c = 3V_P I_P \cos\theta \tag{4.19}$$

Notice that the sum of the three second-harmonic oscillating terms which have a progressive phase difference of 120° is zero. As a result, the instantaneous three-phase power in a balanced system is constant and equal to three times the average power per phase. This is in contrast to power in a single-phase system [Eq. (3.45)], which has a second-harmonic oscillating component. Constancy of power in a balanced three-phase system affords the important advantage of uniform torque in three-phase electric machines. *Inter alia*, this is an important reason in universal adoption of three-phase system except in low power applications.

Thus, in a balanced three-phase system,

$$P = 3\, V_p I_p \cos\theta;\ \cos\theta = pf \tag{4.20}$$

Converting phase values to line values,

$$P = \sqrt{3}\, V_L I_L \cos\theta = 3I_p^2 R_p;\ \cos\theta = pf \tag{4.21}$$

where R_p = equivalent per phase series resistance of load.

Similarly, $$Q = \sqrt{3}\, V_L I_L \sin\theta = 3I_p^2 X_p \tag{4.22}$$

where X_p = equivalent per phase series reactance of load. Of course, in a balanced three-phase system, each phase has the same power factor.

4.6 THREE-PHASE CIRCUIT ANALYSIS

Figure 4.12 shows a typical three-phase, star-connected voltage source, transmission line and star-connected load. Both source and load are balanced three phases. The two neutrals are isolated but these were connected as shown by the dotted line. No current would flow in the neutral connection as $\bar{I}_a + \bar{I}_b + \bar{I}_c = 0$; the currents would form a balanced set in a balanced system. Thus, no voltage drop would occur in the neutral connection. For the reference phase, a loop is shown.

$$\bar{V}_a = (\bar{Z}_{TL} + \bar{Z}_L)\bar{I}_a \tag{4.23}$$

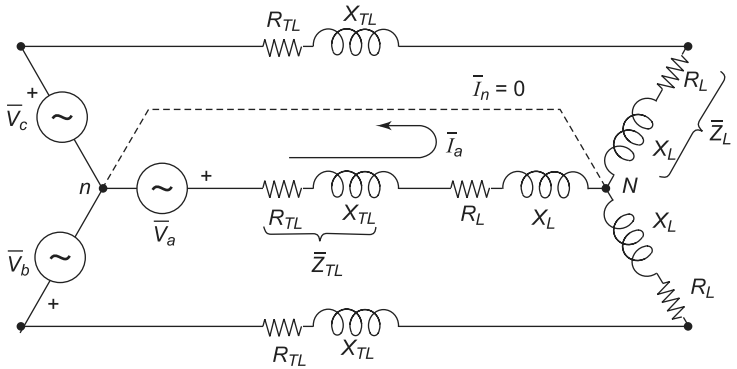


Fig. 4.12 *Balanced three-phase system*

We need to only solve the loop equation (4.23) corresponding to the phase *a*. The currents and voltages in other two loops would have the same magnitude but a progressive phase difference of 120°. Equation (4.23) corresponds to the single-phase equivalent circuit of Fig. 4.13 whose solution completely determines the solution of the three-phase circuit of Fig. 4.12.

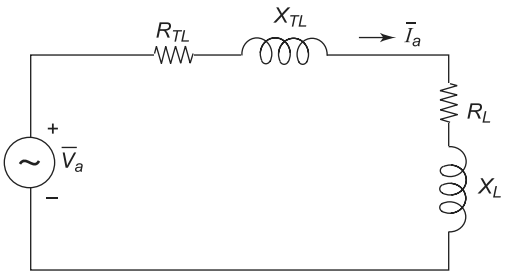


Fig. 4.13 *Per phase equivalent of the three-phase circuit of Fig. 4.12*

4.7 STAR-DELTA CONVERSION

Figure 4.14 shows three delta-connected impedances whose equivalent star (shown dotted) is to be found. Generalisation of Eq. (2.11), in complex impedance form, yields

$$\bar{Z}_a = \frac{\bar{Z}_{ab}\bar{Z}_{ac}}{\bar{Z}_{ab} + \bar{Z}_{bc} + \bar{Z}_{ca}} \tag{4.24a}$$

$$\bar{Z}_b = \frac{\bar{Z}_{bc}\bar{Z}_{ba}}{\bar{Z}_{ab} + \bar{Z}_{bc} + \bar{Z}_{ca}} \tag{4.24b}$$

$$\bar{Z}_c = \frac{\bar{Z}_{ca}\bar{Z}_{cb}}{\bar{Z}_{ab} + \bar{Z}_{bc} + \bar{Z}_{ca}} \tag{4.24c}$$

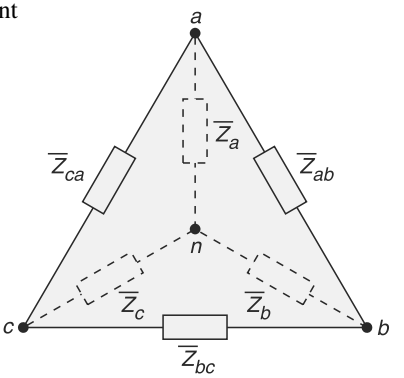


Fig. 4.14 *Star-delta conversion*

Similarly, in converting star to delta, it follows from Eq. (4.10),

$$\bar{Z}_{ab} = \frac{\bar{Z}_a\bar{Z}_b + \bar{Z}_b\bar{Z}_c + \bar{Z}_c\bar{Z}_a}{\bar{Z}_c} \tag{4.25a}$$

$$\bar{Z}_{bc} = \frac{\bar{Z}_a\bar{Z}_b + \bar{Z}_b\bar{Z}_c + \bar{Z}_c\bar{Z}_a}{\bar{Z}_a} \tag{4.25b}$$

$$\bar{Z}_{ca} = \frac{\bar{Z}_a\bar{Z}_b + \bar{Z}_b\bar{Z}_c + \bar{Z}_c\bar{Z}_a}{\bar{Z}_b} \tag{4.25c}$$

If the impedances are balanced, it follows from the above results that

$$\bar{Z}_\Delta = 3\bar{Z}_Y \tag{4.26}$$

Example 4.4

A balanced star-connected load is supplied from a symmetrical three-phase, 400 V (line-to-line) supply. The current in each phase is 50 A and lags 30° behind the phase voltage. Find (a) phase voltage, (b) phase impedance, and (c) active and reactive power drawn by the load. Also, draw line phasor diagram showing phase and line voltages and line currents.

Solution The system circuit diagram is drawn in Fig. 4.15.

(a) $V_L = 400$ V

$$V_P = \frac{400}{\sqrt{3}} = 231 \text{ V; reference phasor}$$

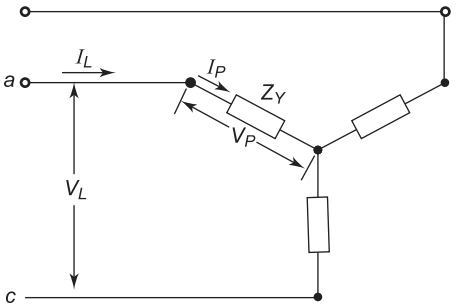


Fig. 4.15

(b) $\bar{I}_L = \bar{I}_P = 50 \angle -30°$

$$\bar{Z}_Y = \frac{231 \angle 0°}{50 \angle -30°} = 4.62 \angle +30°$$

$$= 4 + j2.31$$

(c) $P = \sqrt{3} V_L I_L \cos\theta$

$= \sqrt{3} \times 400 \times 50 \cos 30° = 30$ kW

$Q = \sqrt{3} V_L I_L \sin\theta$

$= 3 \times 400 \times 50 \times \sin 30° = 17.32$ kVAR

The phasor diagram is drawn in Fig. 4.16.

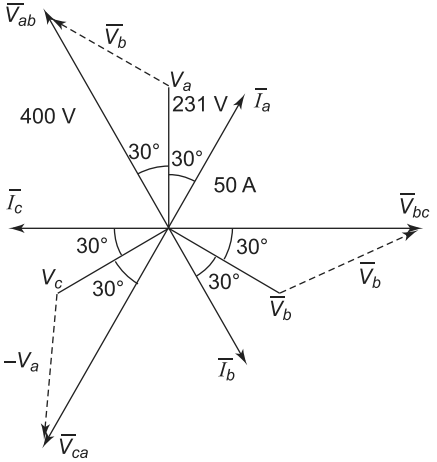


Fig. 4.16

Example 4.5

A balanced delta-connected load of impedance 16 + *j* 12 Ω/phase is connected to a three-phase 400 V supply. Find the phase current, line current, power factor, power, reactive VA and total VA. Also draw a phasor diagram.

Solution Refer to Fig. 4.17.

$$V_P = V_L = 400 \text{ V}$$

$$I_P = \frac{400 \angle 0°}{16 + j12} = 20 \angle -36.9° \text{ A}$$

$pf = \cos 36.9° = 0.8$ lagging

$$I_L = \sqrt{3} \times 20 = 34.64 \text{ A}$$

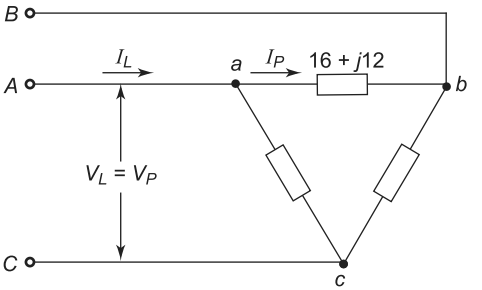


Fig. 4.17

$$P = \sqrt{3} \times 400 \times 34.64 \times 0.8 = 19.2 \text{ kW}$$

$$Q = \sqrt{3} \times 400 \times 34.64 \times 3639° = 14.4 \text{ kVAR}$$

The phasor diagram is drawn in Fig. 4.18 where 36.9° ≈ 37°

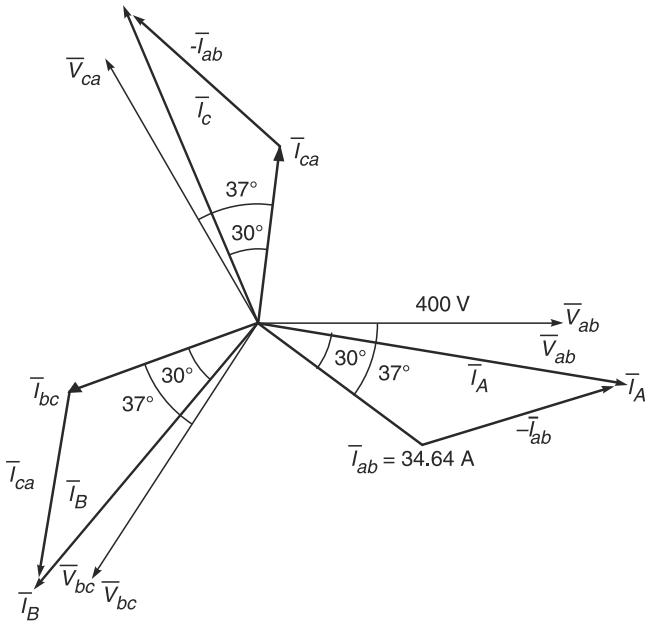


Fig. 4.18

4.8 THREE-PHASE POWER MEASUREMENT

Two-Wattmeter Method

A wattmeter has two coils—a current coil and a voltage coil. A single-phase wattmeter is connected in the circuit as in Fig. 4.19 to measure the power $P = VI \cos \phi$ wherein the load current passes through the current coil and the voltage is applied across the voltage coil.

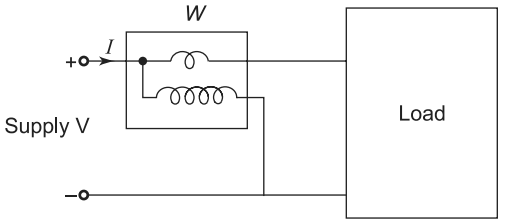


Fig. 4.19

Instead of using three wattmeters to measure three-phase power, it is possible and economical to use two wattmeters to measure three-phase power. The connection diagram to measure power to a three-phase balanced load is drawn in Fig. 4.20. The current coils of the two wattmeters are connected in series with any two lines and the negative ends of the two voltage coils are connected to the third line.

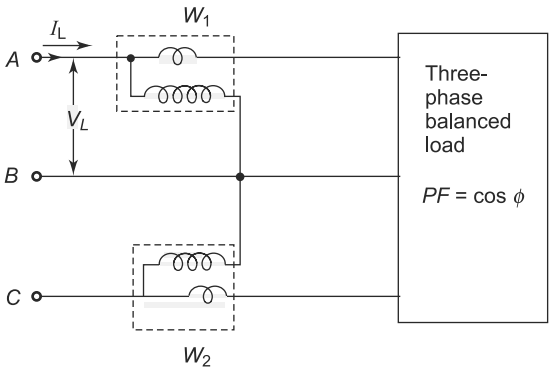


Fig. 4.20 *Connection diagram*

The load may be star or delta connected. We shall assume star but delta load can be converted to equivalent star. The phasor diagram showing relevant voltages and currents is drawn in Fig. 4.21 with lagging phase angle ϕ.

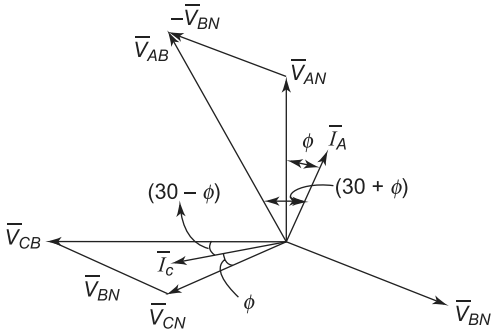


Fig. 4.21 *Phasor diagram*

From the phasor diagram, power reading of the wattmeter W_1 is

$$W_1 = V_L I_L \cos \angle \text{ between } \overline{V}_{AB} \text{ and } \overline{I}_A$$

$$= V_L I_L \cos (30° + \phi) \tag{4.27}$$

The reading of the wattmeter W_2 is

$$W_2 = V_L I_L \cos \angle \text{ between } \overline{V}_{Cb} \text{ and } \overline{I}_C$$

$$= V_L I_L \cos (30° - \phi) \tag{4.28}$$

The sum of the wattmeter readings

$$W_1 + W_2 = V_L I_L [\cos (30° + \phi) + \cos (30° - \phi)]$$

$$= 2V_L I_L \cos 30° \cos \phi$$

$$= \sqrt{3}\, V_L I_L \cos \phi = P \text{ (three-phase power)} \tag{4.29}$$

Also,

$$W_1 - W_2 = V_L I_L \sin \phi \tag{4.30}$$

The ratio $$\frac{W_1 - W_2}{W_1 + W_2} = \frac{1}{\sqrt{3}} \tan\phi$$

The power factor is then given by

$$\text{pf} = \cos\phi = \cos\tan^{-1}\left[\left(\frac{W_1 - W_2}{W_1 + W_2}\right)\sqrt{3}\right] \tag{4.31}$$

Conclusion

The three-phase power is the algebraic sum of the readings of the two wattmeters. If $(W_1 - W_2)$ is positive, the phase angle and so the pf are lagging; follows from Eq. (4.31). On the other hand, the phase angle and so the pf is leading if $(W_1 - W_2)$ is negative.

Without proof, it can be stated that the two-wattmeter method reads the total power $(W_1 + W_2)$ even if the load were unbalanced.

Example 4.6

In Fig. 4.21, find the phase angle between $\overline{V}_{AC}$ and $\overline{I}_A$ if the load pf is cos ϕ lagging.

Solution With $\overline{V}_{AN}$ as reference

$$\angle \overline{I}_A = -\phi$$

$$\angle \overline{V}_{AC} = -30°$$

$\angle$ between $\overline{V}_{AC}$ and $\overline{I}_A = -30° - (-\phi) = -30° + \phi$

Example 4.7

A balanced three-phase 400 V supply is connected to a balanced 3-phase delta-connected load as shown in Fig. 4.22. It is found by measurement that $\overline{I}_{ab} = 20\angle -30°$ A.

(a) Determine line current $\overline{I}_{Aa}$.

(b) Compute the total value of power received by the load.

(c) Calculate the resistive component of load impedance.

(d) Draw the phasor diagram showing line voltages, phase currents and line currents.

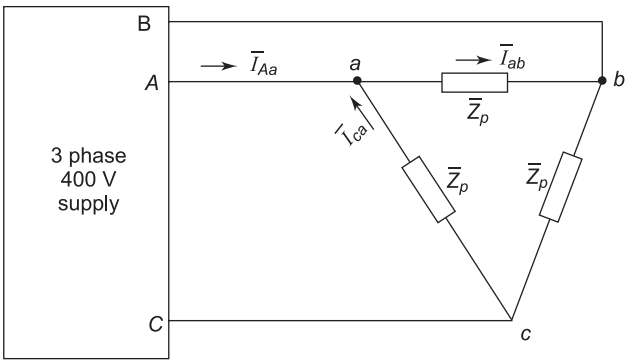


Fig. 4.22

Solution

(a) $\bar{I}_{ab} = 20 \angle -30° A$ Reference $V_{ab} \angle 0°$

For balanced load,

$$\bar{I}_{bc} = 20 \angle -30° - 120°$$

$$= 20 \angle -150° \text{ A}$$

$$\bar{I}_{ca} = 20 \angle -30° - 240°$$

$$= 20 \angle -270°$$

$$= 20 \angle -270° - 360°$$

$$= 20 \angle 90° \text{A}$$

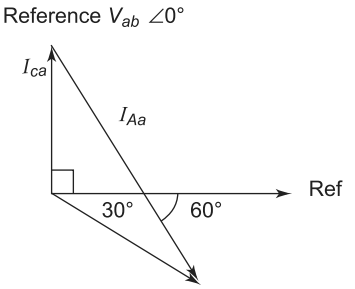


Fig. 4.23

The line current from phasor diagram of Fig. 4.23.

$$\bar{I}_{Aa} = \bar{I}_{ab} - \bar{I}_{ca}$$

$$= 20\sqrt{3} \angle -60° \text{ A}$$

(b) Power drawn by phase *ab* of load

$$P(\text{total}) = 3 \times 6.928 = 20.78 \text{ kW}$$

(c) $$\bar{Z}_p = \frac{400 \angle 0°}{20 \angle -30°} = 10 \angle 30° \ \Omega$$

$$= 8.66 + j5$$

Then, $R_p = 8.66\ \Omega$

(d)

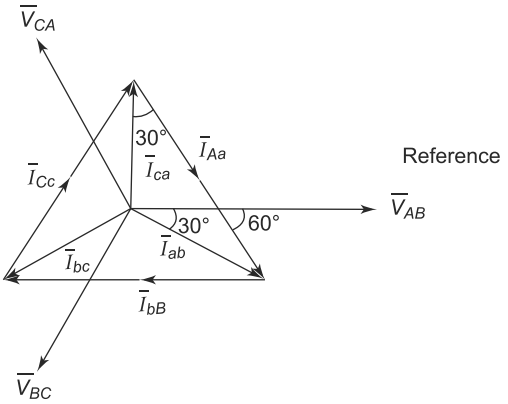


Fig. 4.24

Example 4.8

A balanced star-connected load has an impedance of 5 ∠ 60° Ω. The voltage of '*a*' to neutral is $\bar{V}_{an}$ = 25 ∠ 30° V. Calculate the phasor currents in phases '*b*' and '*c*'. Write the expression for the phasor voltage '*a*' to '*c*', i.e. $\bar{V}_{ac}$.

Solution

$$\bar{I}_{an} = \frac{\bar{V}_{an}}{\bar{Z}_P} = \frac{25\angle 30°}{5\angle 60°} = 5\angle -30° \text{ A}$$

Being balanced

$$\bar{I}_{bn} = 5\angle -30° - 120° = 5\angle -150° \text{ A}$$

and $$\bar{I}_{cn} = 5\angle -30° + 120° = 5\angle -90° \text{ A}$$

Given $$\bar{V}_{an} = 25\angle 30° \text{ V}$$

Then $$\bar{V}_{cn} = 25\angle 30° + 120° = 25\angle 150° \text{ V}$$

$$\bar{V}_{ac} = \bar{V}_{an} = 25\sqrt{3}\angle 0° \text{ V}$$

or $$V_{ac} = 43.30° \text{ V}$$

The phasor diagram is drawn in Fig. 4.25.

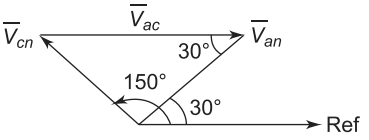


Fig. 4.25

Example 4.9

A three-phase, 50 Hz, 400 V system feeds a load of 25 kW at pf = 0.7 lagging as shown in Fig. 4.26 Three capacitors are connected between lines across the load to improve the pf to 0.85. Determine the resultant current drawn from the supply and value of the capacitors.

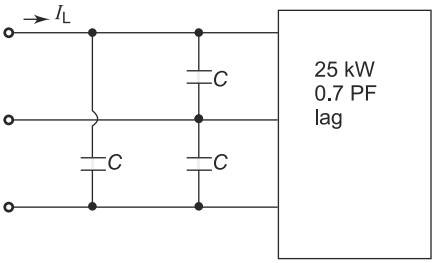


Fig. 4.26

Solution As the capacitors are delta-connected, we shall take load also as delta-connected. The line current fed to load is

$$25 \times 10^3 = 3\sqrt{3} \times 400 \times I_D \times 0.7$$

The phase current is

$$\bar{I}_P = 29.76 \angle -45.6° \text{A}$$

The system's per phase diagram is drawn in Fig. 4.27. As the capacitor does not draw any real power, the resultant phase current is given by

$$I'_P = \left(\frac{2500}{3}\right) \times \frac{1}{400} \times \frac{1}{0.85} = 24.5 \text{ A}, \ \phi' = \cos^{-1}0.85 = 31.8° \text{ lag}$$

Resultant line current

$$I'_L = 24.5\sqrt{3} = 42.4 \text{ A}$$

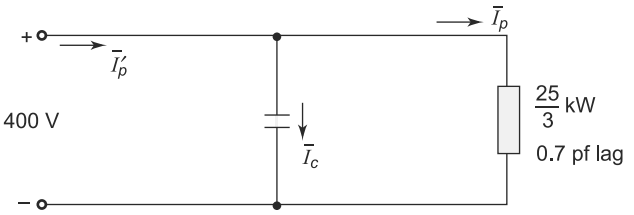


Fig. 4.27

As per KCL at the node in Fig. 4.27

$$I'_P = \bar{I}_P + \bar{I}_C$$

$$24.5 \angle -31.8° = 29.76 \angle -45.6° + \bar{I}_C$$

Converting to rectangular form,

$$20.8 - j12.9 = 20.8 - j21.26 + j\, I_C;\ I_C \text{ leads by } 90°$$

Or $I_C = 10.74$ A

But $I_C = V\omega C$

So we get

$$C = \frac{10.74}{400 \times 2\pi \times 50} = 85.5\ \mu\text{F}$$

Example 4.10

A three-phase, three-wire balanced system with delta-connected load is sketched in Fig. 4.28. Given $\bar{V}_{an} = 231 \angle 60°$, complex power absorbed by each phase of load = 2.5 − *j*1.2 KVA. Phase sequence *abc*. Determine $\bar{V}_{bc}, \bar{Z}_P, \bar{I}_{an}$.

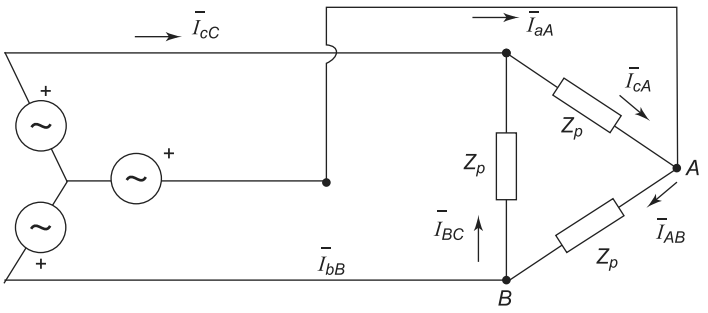


Fig. 4.28

Solution

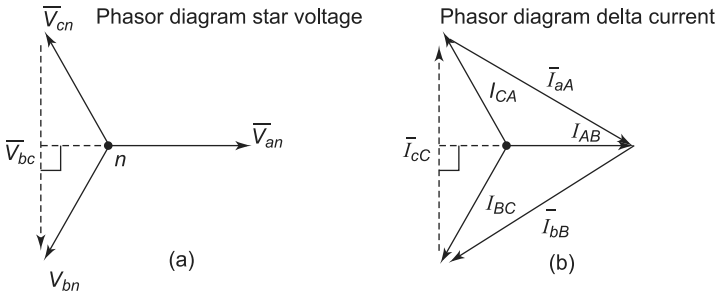


Fig. 4.29

$\overline{V}_{bc} = \sqrt{3}\,\overline{V}_{an} \angle 60° - 90°$; from phasor diagram of Fig. 4.29(a).

$$= \sqrt{3} \times 231 \angle -30°$$

$$= 400 \angle -30° \text{ V} = 0.4 \angle -30° \text{ kV}$$

$$\overline{S}_P = \overline{V}_{BC}\,\overline{I}^{*}_{BC}$$

$$(2.5 - j1.2) = 0.4 \angle -30°,\ I^{*}_{BC} = 2.77 - 25.6°$$

$$\overline{I}^{*}_{BC} = \frac{2.5 - j1.2}{0.4 \angle -30°} = \frac{2.77 \angle -25.6°}{0.4 \angle -30°} = 6.925 \angle 4.4° \text{ A}$$

$$\overline{I}_{BC} = 6.925 \angle -4.4° \text{ A}$$

From the delta phasor diagram [Fig. 4.29(b)],

$$\overline{I}_a = \overline{I}_{aA} = \sqrt{3}\,\overline{I}_{BC} \angle 90° = 12 \angle 85.6° \text{ A}$$

Summary

- All practical power systems are three-phase; generation, transmissions and distribution. Domestic wiring is single-phase inside the building.
- Three-phase connections are star and delta.
- Three-phase operation is arranged to be nearly balanced.
- Balanced three-phase voltages (and currents) have a progressive phase difference of 120°.
- Phase sequence; positive *abc*, phase '*a*' leads '*b*' by 120° and '*b*' leads '*c*' by 120°, negative sequence *cba*, phase '*c*' leads '*b*' by 120° and '*b*' leads '*a*' by 120°.
- V_L = line to line voltage (or line voltage), V_p = phase voltage, I_L = line current, I_p = phase current
- Star connection $V_L = \sqrt{3}\,V_P$, $I_L = I_P$

  Delta connection $V_L = V_P$; $I_L = \sqrt{3}\,I_P$

➢ Three-phase power (active)

$P = \sqrt{3}\, V_L I_L \cos\theta$; $W\theta$ = phase angle between phase voltage and phase current,

It is same for each phase.

Power factor = cos θ lagging or leading; same for each phase. Commonly called three-phase (balanced) power factor.

Three-phase reactive power

$Q = \sqrt{3}\, V_L I_L \sin\theta$; VAR ; positive for lagging pf and negative for leading pf.

Three-phase volt-amperes (VA)

$$S = \sqrt{P^2 + Q^2}$$

➢ Balanced three-phase star/delta load impedance conversion

$$Z_Y = \frac{1}{3} Z_\Delta \text{ per phase}$$

➢ In a balanced three-phase system, calculations are carried out on per *phase basis*. The system is represented by a one-line diagram.

Exercises

Review Questions

1. A balanced three-phase star-connected voltage source supplies power to a balanced three-phase star-connected load. Show by a phasor diagram that if the load neutral is connected to the source neutral, no current will flow in the connecting wire.
2. Write the mathematical expressions for three balanced voltage sources. When one of the voltages has the peak value at an instant, what are the corresponding values of the other two voltages?
3. Show by a phasor diagram that when three-phase balanced voltage sources are connected in delta formation, no current will flow round the loop so formed. Explain why a delta-connected source is not used in practice.
4. Draw the phasor diagram of a star-connected balanced voltage source, if the relative phase angle between $\overline{V}_{BC}$, and $\overline{V}_{An}$ is 90°.
5. Solve Question 4 with the relative phase angle between $\overline{V}_{BC}$ and $\overline{V}_{Bn}$ as 30°.
6. In a three-phase balanced delta-connected load supplied from a balanced three-phase voltage source, what is the angle between line and phase currents as two three-phase sets? A three-phase load has a power factor of say 0.8 lagging. What is the meaning of this?
7. Is it same for all the three phases or their average value?
8. What is the meaning of 'phase sequence' in a three-phase voltage source?
9. A balanced three-phase delta-connected load has phase impedance of $(R + jX)$ and draws line current I. Write the expression for three-phase active and reactive powers.

Problems

1. A balanced star load of 8 $+j6\ \Omega$ per phase is connected to three-phase, 230 V supply. Find the line current, power factor, power, reactive VA and total VA.
2. A balanced three-phase, delta-connected load of 160 kW takes a leading current of 100 A with a line voltage of 1100 V, 50 Hz. Find the circuit constants of the load per phase.
3. A balanced delta-connected load of 16 $+j12\ \Omega$ phase is connected to a three-phase, 230 V supply. Find the line current, power factor, power, reactive VA and total VA.

4. A symmetrical three-phase, 400 V system supplies a balanced delta-connected load. The current in each delta branch is 30 A and its phase angle is 37° lagging (w.r.t. voltage across each branch). Find the line current and total power. Draw the phasor diagram showing all currents and voltages.
5. Three star-connected impedances $\bar{Z}_1 = 16 + j20\,\Omega$, per phase are in parallel with three delta-connected impedances of $\bar{Z}_2 = 27 + j18\,\Omega$ per phase across a three-phase, 400 V supply. Find the line current, power factor and reactive VA of the combination.
6. A 220 V, three-phase voltage is applied to a balanced delta-connected load.
   $\bar{I}_{ab} = 10 \angle -37°$ A w.r.t. $\bar{V}_{ab}$
   (a) Find the line current and its phase angle w.r.t. line to neutral voltage.
   (b) Compute total power received by the load.
   (c) Find the value of the resistive part of the phase impedance.
7. Input power to a three-phase motor is measured by the two-wattmeter method. The two wattmeter readings are 4.8 kW and –1.6 kW with a line voltage of 400 V. Calculate (a) the total power (active), (b) the power factor, and (c) the line current.
8. A star-connected source feeds a delta-connected load through lines of 5 Ω resistance each. The sending-end complex power is 3.45 + *j*1.8 KVA and receiving end complex power is 3 + *j*1.8 KVA. Find (a) line current, (b) load phase current, it (c) source phase voltage.

Multiple-Choice Questions

1. The sum of instantaneous power in a balanced three-phase system is
   (a) constant
   (b) constant plus a second-harmonic oscillating component
   (c) constant plus a fundamental oscillating component
   (d) constant plus a third-harmonic oscillating component
2. For a balanced delta-connected load, the phase angle b/W current is delta lag and its voltage is θ. The angle plus a line current and its equivalent star-phase voltage will therefore be
   (a) θ (b) $\theta + 30°$
   (c) $\theta + 60°$ (d) $\theta + 90°$
3. In the two-wattmeter method of power measurement, pf for balanced load is given by
   (a) cos tan $(W_1 + W_2)/(W_1 - W_2)$
   (b) cos tan $(W_1 - W_2)/(W_1 + W_2)$
   (c) cos tan^{-1} $\sqrt{3}\,(W_1 - W_2)/(W_1 + W_2)$
   (d) cos tan^{-1} $\sqrt{3}\,(W_1 + W_2)\,/\,(W_1 - W_2)$
4. In the two-wattmeter method of necessary power in a balanced three-phase circuit, the readings of the two wattmeters are in the ratio of 1:2. The circuit power factor is
   (a) 1/2 (b) $1\sqrt{2}$ (c) $\sqrt{3}/2$ (d) 1
5. In equivalent star of three balanced line voltages, the voltage of a phase of the star w.r.t. line voltage V_{bc} (phase sequence abc) has an angle of
   (a) +90° (b) –90° (c) +30° (d) –30°
6. Three impedances of z Ω each are connected in delta. Their equivalent star impedance phase will be
   (a) $z/3$ (b) $\sqrt{3}/2$ (c) $z/3$ (d) $3z$
7. In a balanced three-phase star-connected sources the angle are
   $\angle(\bar{V}_a, \bar{V}_{ab}), \angle(\bar{V}_b, \bar{V}_{bc}), \angle(\bar{V}_c, \bar{V}_{ca})$
   (a) all equal to –30° (b) all equal to +30°
   (c) all equal to +90° (d) all equal to –90°

8. Two wattmeters are used to find power in a balanced three-phase circuit. If the two wattmeters are found to have equal readings, the circuit power factor will be
   (a) $\sqrt{3}/2$ (b) 1 (c) 1/2 (d) $1\sqrt{2}$

9. If $\overline{V}_a = 1.\angle 0°; \overline{V}_b = 1.\angle 120°; \overline{V}_c = 1.\angle 240°$ constitutes a balanced set of three phase voltages, the magnitude and angle of voltage $\overline{V}_{bc}$ are
   (a) $1/\sqrt{3}, -90°$ (b) $\sqrt{3}, +90°$
   (c) $\sqrt{3}, -30°$ (d) $1/\sqrt{3}, +30°$

10. Given below are two sets of instantaneous phase voltages at two different time instants of a three-phase voltage system. Mark the correct answer.
   (a) $(-1, -1/2, 1/2),\ (-3\sqrt{2}, 0, -\sqrt{3}/2)$
   (b) $(-1, -1/2, 1/2),\ (\sqrt{3}/2\ 0, -\sqrt{3}/2)$
   (c) $(-1, -1/2, 1/2),\ (\sqrt{3}/2\ 0, -\sqrt{3}/2)$
   (d) $(-1, -1/2, -1/2),\ (\sqrt{3}/2\ 0, -\sqrt{3}/2)$

Answers

Multiple-Choice Questions

1. (a) 2. (a) 3. (c) 4. (c) 5. (b)
6. (d) 7. (a) 8. (b) 9. (b) 10. (d)

Magnetic Circuits

chapter 5

Goals & Objectives

- Fundamental laws of electromagnetism and induction; also certain rules
- Definitions of magnetic quantities
- Magnetic circuits, dc analog
- Energy stored in magnetic field
- Inductance—self- and mutual

5.1 INTRODUCTION

The electromagnetic system is an essential element of all rotating electric machinery and electromechanical devices as well as static devices like the transformer. The role of the electromagnetic system is to establish and control electromagnetic fields for carrying out conversion of energy, its processing and transfer. Practically, all electric motors and generators, ranging in size from fractional kW units found in domestic appliances, to the gigantic several thousand kW motors employed in heavy industry and several hundred megawatt generators installed in modern generating stations, depend upon the magnetic field as the coupling medium allowing interchange of energy in either direction between electrical and mechanical systems. It is seen that all electric machines including transformers use the medium of magnetic field for energy conversion and transfer.[1] The study of these devices essentially involves electric and magnetic circuit analysis and their interaction. Also, several other essential devices like relays, circuit breakers, etc. need the presence of a confined magnetic field for their operation.

The purpose of this chapter is to review the physical laws governing magnetic fields, induction of emf and production of mechanical force, and to develop methods of magnetic-circuit analysis.[2] Simple magnetic circuits and magnetic materials will be briefly discussed. In the chapters to follow, how the concepts of this chapter are applied in the analysis of transformers and machines will be dealt with.

5.2 AMPERE'S LAW—MAGNETIC QUANTITIES

Consider a long straight conductor carrying current i_1 as shown in Fig. 5.1. As discovered by Ampere, the current creates a field of force in the surrounding medium, which is known as the *magnetic field*. To investigate the field, we place an elemental conductor of length l parallel to the long conductor carrying

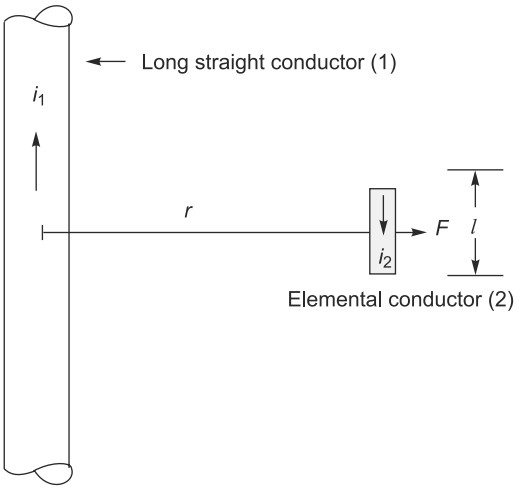


Fig 5.1 *Illustration of Ampere's law*

[1] Transformers are used in such varied applications as radio and television receivers and electrical power transmission and distribution circuits.

[2] The concept of quasi-static magnetic field and the underlying assumptions and their validity, which make the magnetic circuit analysis a simpler exercise and do not require involved magnetic field analysis, will be brought out clearly though briefly.

current i_2 in opposite direction. Of course, the elemental conductor ($i_2\ l$) is part of a circuit (not shown in the figure) which causes the current i_2 to flow. A force of repulsion acts on the elemental conductor at right angles to the long conductor and the element as shown in Fig. 5.1. The magnitude of this force (of magnetic origin) in MKS units is given by

$$F = \left(\frac{\mu i_1}{2\pi r}\right)(i_2 l)\text{N} \tag{5.1}$$

where μ is a constant of the medium called *permeability*.

As we rotate the elemental conductor (2) about the long conductor (1) in a plane circular path of radius r, the force F on the conductor (2) remains constant and outward-oriented. This *closed* circuit path is a line of magnetic flux; just called a *flux line*. In the region surrounding the conductors, there are flux lines all along the conductor extending from the conductor surface outwards. The symbol for flux is ϕ and its unit is weber (Wb).

5.2.1 Flux Density (*B*)

In any elemental area across flux, it is convenient to work in terms of flux density B as Wb/m^2.

We can write Eq. (5.1) as

$$F = B.(i_2 l) \tag{5.2a}$$

where the flux density B is defined as

$$B = \mu\left(\frac{i_1}{2\pi r}\right),\ \frac{\text{N}}{\text{Am}} \tag{5.2b}$$

In terms of flux, units of B are Wb/m^2, generally called *tesla* (T).

5.2.2 Magnetic Field Intensity (*H*) or Magnetising Force

It is convenient to work in terms of a quantity that is independent of the medium. We define from Eq. (5.2b) the magnetic field intensity as

$$H = \frac{i_1}{2\pi r} = \frac{B}{\mu}\ \text{A/m} \tag{5.3}$$

It is indeed the magnifising force i_1 spread over the length of the flux path.

The current i_1 in one conductor may comprise of

$$i_1 = Ni \tag{5.4}$$

where there are N conductors each carrying current i.

As current always flows in a closed path, N conductors indeed are N turns. So we write

$$N\,i = \textit{ampere-turns}\ (\text{AT}) \tag{5.5}$$

The ampere-turns in magnetic circuits are referred to as *magnetomotive force*.

$$f = mmf = Ni\ \text{AT} \tag{5.6}$$

5.2.3 Direction of Magnetic Flux, *B* and *H*

At this stage, we need to examine the direction of the magnetic quantities. The cross-sectional view of a long conductor carrying current is drawn in Fig. 5.2.

The symbol $\oplus$ on the conductor indicates the direction of current is into the plane of the paper. By virtue of symmetry, the *flux lines* are circular *closed paths*. The magnetic field intensity H is tangential to the flux line at every point and flux density B has the same direction as H. Thus, both H and B are *vectors* and have the same direction.

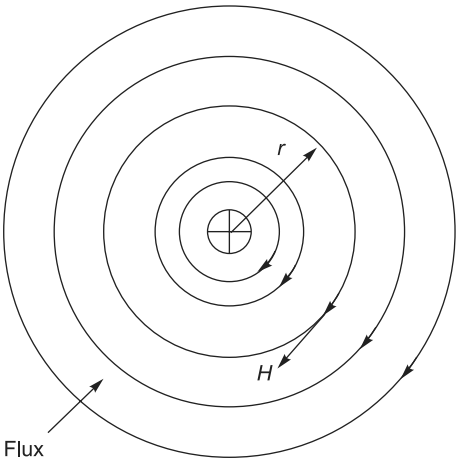


Fig. 5.2 *Magnetic field intensity and flux*

Right-Hand Rule

If you grasp the conductor by the right hand such that the thumb points in the direction of current, the flux is established in the direction in which the fingers curl.

It is observed from Fig. 5.2 that the flux lines are more dense near the conductor than far away, which means that the flux density decreases outwards. This results from the fact that

$$H = \frac{i}{2\pi r} \text{ and } B = \mu H$$

Permeability

It is the property of the medium which determines the flux density for a given magnetising force; it is indeed a constant of proportionality.

Thus,

$$B = \mu H; \mu = \text{permeability} \tag{5.7}$$

In *free space*,

$$B = \mu_0 H$$

where $\mu_0 = 4\pi \times 10^{-7}$ Wb/Am, permeability of free space (5.8)

We can express

$$\mu = \mu_0 \mu_r$$

where

$$\mu_r = \frac{\mu}{\mu_0}, \text{ the } \textit{relative permeability} \text{ of the medium} \tag{5.9}$$

Magnetic materials, iron, steel and certain alloys, by virtue of their inherent property induce much larger flux density. These magnetic materials have

$$\mu_r = 4000 - 10000$$

Of course, nonmagnetic materials have

$$\mu_r = 1$$

Magnetic Flux

For uniform flux density, normal to area A of Fig. 5.3(a), the flux passing through the area is

$$\phi = BA \tag{5.10}$$

If the flux makes an angle θ with respect to the surface normal as in Fig. 5.3(b) then

$$\phi = B\,A\cos\theta \tag{5.11}$$

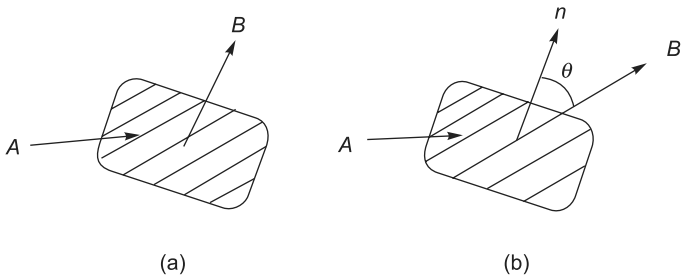


Fig. 5.3 *Magnetic flux*

In general, the total flux piercing a surface must be obtained by surface integral of the dot product.

Both H and B are *vectors* (these are directed quantities) and are related by the constant (μ, μ_0), while ϕ is a *scalar* quantity.

As we shall be dealing with magnetic fields of simple geometry, all we need is the magnitudes of H and B.

Ampere's Circuital Law

For the current-carrying long conductor (1) of Fig. 5.1, both the H and B vectors have circular paths as shown in Fig. 5.2.

Ampere's circuital law can be stated as

$$mmf,\ \mathcal{F} = H\,l,\ l = \text{length of flux line}$$

This law would be employed in analysis and design of electromagnetic circuits and devices.

5.3 MAGNETIC CIRCUITS

Consider a toroidal ring of *ferromagnetic* material of mean radius R and circular cross section of diameter d as shown in Fig. 5.4. The ring termed *core* is excited by a coil wound round it with N turns carrying a current i. By virtue of symmetry, flux established in the magnetic core is circular in shape.

5.3.1 Leakage Flux

The flux established along paths that lie mostly in air is very small compared to the core flux as the core has a permeability μ_r times that of air. This flux is called *leakage flux*, i.e. it leaks through the core. There are no magnetic insulators to prevent such leakage. Being small in magnitude, leakage flux will be neglected here[3].

[3] Effect of leakage flux in transformers and electric machines cannot be ignored. It must, therefore, be computed in machine design or in a built-up machine and its effect must be determined experimentally.

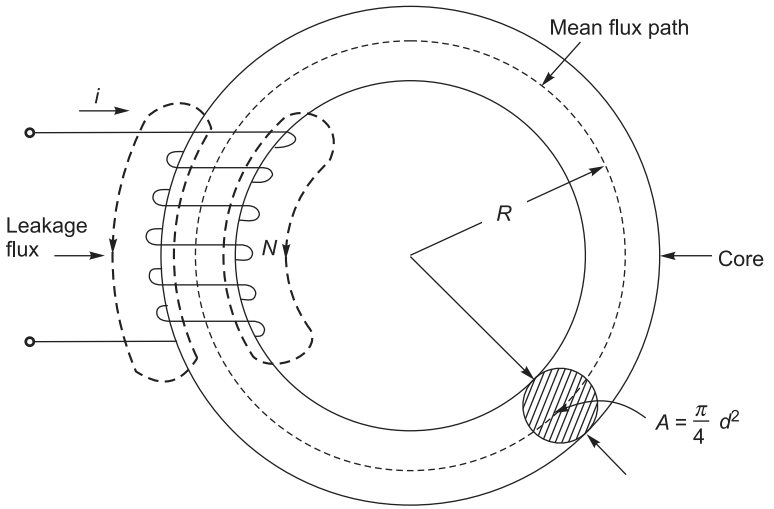


Fig. 5.4 *Toroidal ring of ferromagnetic material with exciting coil*

All the flux lines in the core enclose a current of

$$\mathcal{F} = Ni\ A \tag{5.12}$$

which is known as *magnetomotive force* (mmf) and in engineering practice has the units of ampere-turns (AT). It is a kind of magnetic potential difference. Thus,

$$\mathcal{F} = Ni\ AT \tag{5.13}$$

The mmf is expended in establishing flux round the core.

By symmetry, H in the core is constant along each flux line and for the mean flux line of radius R shown dotted in Fig. 5.7, the magnetising force is

$$H = \frac{\mathcal{F}}{2\pi R} = \frac{\mathcal{F}}{l} \text{ AT/m} \tag{5.14}$$

where l is the length of the mean flux path. The length of the flux lines in a toroidal core increases and H reduces as we proceed outwards. For slender core ($d << R$), it is sufficiently accurate to neglect this variation and base the calculations on the *mean flux path* and regard H as constant, across the core cross section.

The mean flux density

$$B = \mu H = \frac{\mu \mathcal{F}}{l} = T \tag{5.15}$$

As the flux in this core geometry is normal to the cross-sectional area, the total flux established round the core is given by

$$\phi = \mu H = AB = \frac{\mathcal{F}}{l/\mu A} = \frac{\mathcal{F}}{R} = PF \tag{5.16}$$

where $$\mathcal{R} = \frac{l}{\mu A} \text{ AT/Wb} \tag{5.17}$$

= reluctance of the magnetic circuit

$$= \mathcal{P} \times \frac{1}{\mathcal{R}}$$

and $\mathcal{P} = 1/\mathcal{R}$ = *permeance* of the magnetic circuit (5.18)

While units of reluctance (also permeance) have been defined above, these need not be specified every time.

The concept of reluctance, lumps the magnetic system into a circuit analogically expressed as a dc electric circuit, as shown in Fig. 5.5. In fact, Eq. (5.16) is no different from the circuital Ohm's law. In this analog,

$\mathcal{F}$ ~ dc voltage (potential)

$\mathcal{R}$ ~ resistance

ϕ ~ current

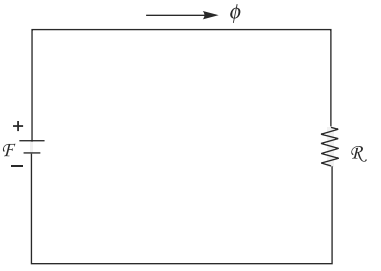


Fig. 5.5 *The dc circuit analog of magnetic system of Fig. 5.6*

The resistance of an electric wire is given by $\mathcal{R} = \dfrac{l}{\rho A}$ an equation analogous to Eq. (5.17) for magnetic reluctance.

Kirchhoff's two laws of the electric circuit equally apply to the magnetic circuits. It means that the mmf of loop equals the mmf expended in various parts of the loop (KVL) and the incoming and outgoing fluxes are equal at a junction of magnetic elements (KCL). In applying these laws, the circuit is divided into a number of elements so chosen that the flux density is approximately the same all over the element. The length of each element corresponds to its mean path.

The dc analog of a magnetic circuit applies only for computation of F, ϕ and R. There is no power loss in R but power loss $I^2 R$ occurs in dc circuit resistance.

Example 5.1

Figure 5.6(a) shows a rectangular magnetic core with an air gap. Find the exciting current needed to establish a flux density of B = 1.2 T in the air gap. Given N = 400 turns and μ_r (iron) = 4000.

Solution It is a simple series magnetic circuit with its analog shown in Fig. 5.6(b).

Core length $l_c = 2\,[(20 - 4) + (16 - 4)] - 0.2 = 55.8$ cm

Cross-sectional area of core $A_c = 16\ \text{cm}^2$

Core reluctance

$$\mathcal{R}_c = \frac{55.8 \times 10^{-2}}{4000 \times 4\pi \times 10^{-7} \times 10 \times 10^{-4}}$$

$$= 0.694 \times 10^5\ \text{AT/Wb}$$

Air-gap length $l_g = 0.2$ cm

Area of air gap $A_g = 16\ \text{cm}^2$

$$\text{Air-gap reluctance } \mathcal{R}_g = \frac{0.2 \times 10^{-2}}{4\pi \times 10^{-7} \times 16 \times 10^{-4}}$$

$$= 9.95 \times 10^5\ \text{AT/Wb}$$

$$\mathcal{R}(\text{total}) = \mathcal{R}_c + \mathcal{R}_g$$

$$= 0.694 \times 10^5 + 9.95 \times 10^5 = 10.64 \times 10^5\ \text{AT/Wb}$$

Flux in the magnetic circuit, $\phi = B\,A = 1.2 \times 16 \times 10^{-4} = 1.92$ mWb

Now $\text{Ni} = \mathcal{F} = \phi\mathcal{R}$

$$= 1.92 \times 10^{-3} \times 10.64 \times 10^5$$

$$= 2043\ \text{AT}$$

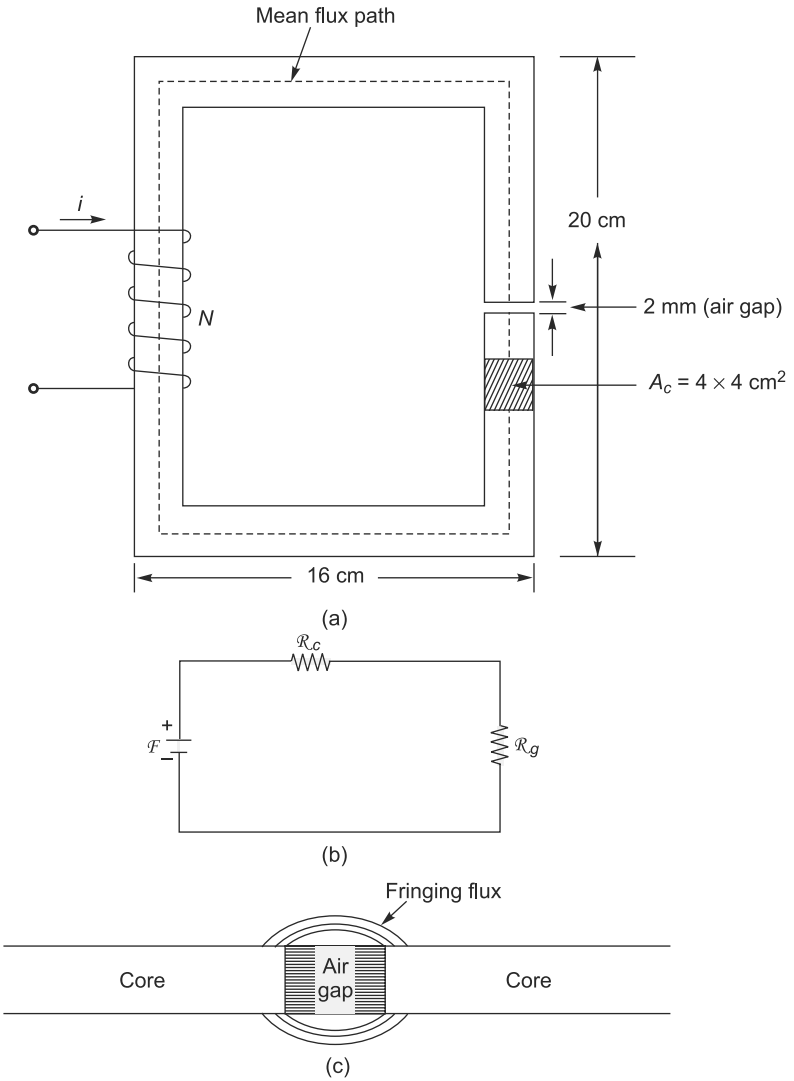


Fig 5.6 *(a) Magnetic core with air gap, (b) electric circuit analog of the case of Fig. 8.5 (a), and (c) flux fringing*

$\therefore$ Exciting current $i = \dfrac{2043}{400} = 5.11$ A

It is seen above that

$$\mathcal{R}_g/\mathcal{R}_e = 15.34$$

Therefore, for simplicity of computation, $\mathcal{R}_e$ (magnetic core reluctance) may be altogether neglected. Then

$$i = 1.2 \times 16 \times 10^{-4} \times 9.95 \times 10^5/400 = 5.77 \text{ A}$$

This simplification has caused an error of 6.6% which can be easily tolerated in magnetic-circuit calculations.

Fringing

The flux passing from the core to the air gap cannot remain confined to the air gap but would somewhat spread out, an effect called *fringing* as illustrated in Fig. 5.6(c). This is because the flux paths near the air gap have length comparable to the proper air gap length. As a result, the average flux density in the air gap is slightly less than the flux density in the core, i.e. $(B_g)\,(av) < B_c$. Fringing can be accounted for *empirically* by increasing the linear dimensions of the gap by one-gap length.

Let us consider the effect of fringing on the result (exciting current) for the example given below.

Air-gap area $A_g = 4 \times 4$ cm^2

Gap length = 0.2 cm

Air-gap area modified to account for fringing

$$A_g \text{ (modified)} = (4 + 0.2) \times (4 + 0.2)$$

$$= 15.64 \text{ cm}^2$$

Now $$\mathcal{R}_g = \frac{0.2 \times 10^{-2}}{4r \times 10^{-7} \times 17.64 \times 10^{-4}} = 9.002 \times 10^5 \text{ AT/Wb}$$

Then $$\mathcal{R}(\text{total}) = 0.694 \times 10^5 + 9.022 \times 10^5 = 9.72 \times 10^5 \text{ AT/Wb}$$

For the same core flux (1.92 mWb),

$$B_g(\text{av}) = \frac{1.92 \times 10^{-3}}{17.64 \times 10^{-4}} = 1.09 \text{ T} (< B_c = 1.2 \text{ T})$$

Now, $$i = \frac{\phi \mathcal{R}}{N} = \frac{1.92 \times 10^{-3} \times 9.72 \times 10^5}{400} = 5.66 \text{ A}$$

It is observed that for the same core flux, the exciting current needed is slightly less than that calculated earlier (5.11 A) as fringing somewhat reduces air-gap reluctance (9.022×10^5 in place of 9.95×10^5).

Example 5.2

The magnetic circuit of Fig. 5.7 has a cast steel core with dimensions as shown. It is required to establish a flux of 0.8 m Wb in the air gap of the central limb. Determine the mmf of the exciting coil, if for the core material $\mu_r = \infty$. Neglect fringing.

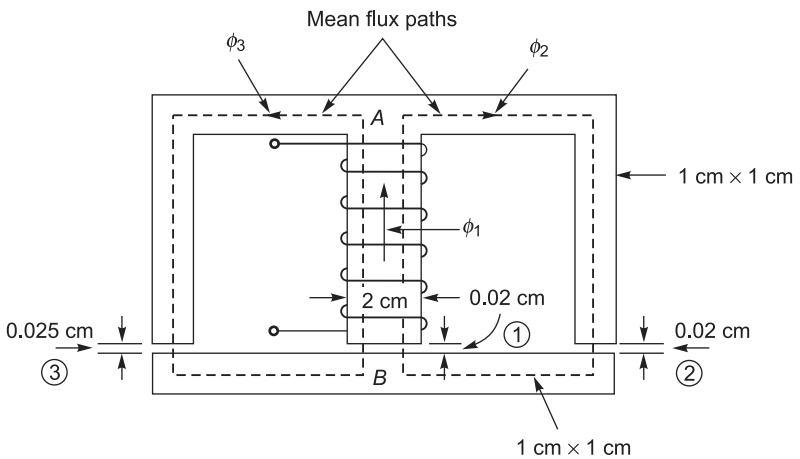


Fig. 5.7

Solution Since $\mu_r = \infty$. No mmf drops in any member of the core. The analogous electrical circuit is drawn in Fig. 5.8(a). It can be reduced to the circuit of Fig. 5.8(b) by parallel combination for R_{g2} and R_{g3}. Various gap reluctances are

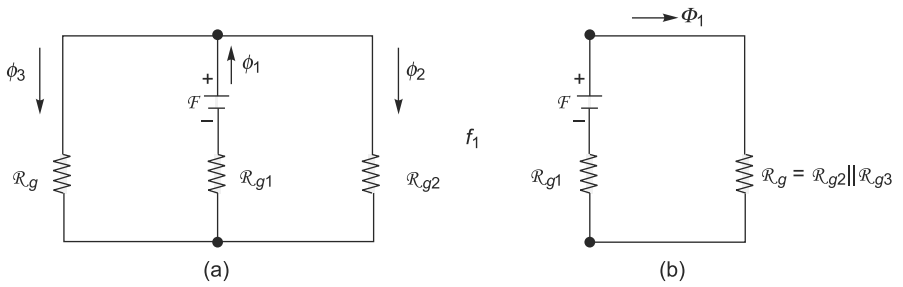


Fig. 5.8

$$\mathcal{R}_{g1} = \frac{0.02 \times 10^{-2}}{4\pi \times 10^{-7} \times 2 \times 1 \times 10^{-4}} = 0.796 \times 10^6 \text{ AT/Wb}$$

$$\mathcal{R}_{g2} = \frac{0.02 \times 10^{-2}}{4\pi \times 10^{-7} \times 1 \times 1 \times 10^{-4}} = 1.592 \times 10^6 \text{ AT/Wb}$$

$$\mathcal{R}_{g3} = \frac{0.025 \times 10^{-2}}{4\pi \times 10^{-7} \times 1 \times 1 \times 10^{-4}} = 1.989 \times 10^6 \text{ AT/Wb}$$

$$\mathcal{R}_{g2} \| \mathcal{R}_{g3} = \frac{1.592 \times 1.989}{1.592 + 1.989} \times 10^6 = 0.884 \times 10^6 \text{ AT/Wb}$$

Exciting coil current $\mathcal{F} = \phi_1(\mathcal{R}_{g1} + \mathcal{R}_{g2} \| \mathcal{R}_{g3})$

$= 0.8 \times 10^{-3} (0.796 + 0.884) \times 10^6$

$= 1344$ AT

5.4 MAGNETIC MATERIALS AND *B-H* RELATIONSHIP (MAGNETISATION CHARACTERISTIC)

Magnetic materials are characterised by high permeability and nonlinear *B-H* relationship (magnetisation characteristic) which exhibits *saturation* and *hysteresis*. This type of behaviour is explained by the domain theory of magnetisation for which a suitable book on material science may be consulted.

Magnetic materials are classified as *ferromagnetic* and *ferrimagnetic*. Iron and its various alloys are ferromagnetic. Hard ferromagnetic materials include permanent magnetic materials such as alnicos, chrome steels, certain copper-nickel alloys and several other alloys. Ferrimagnetic materials consist of mixed oxides of iron and other metals. The oxide mixture is *sintered*, i.e. heated to a steady temperature of 1300°C which is maintained for several hours. The resulting material known as *ferrite* is chemically homogeneous and extremely hard. It has typically maximum flux density of 0.3–0.5 T, as compared to 2.18 T for pure iron.

5.4.1 Magnetisation Characteristic

The *B-H* relationship for cyclic *H* is the *hysteresis loop* exhibited in Fig. 5.9 where the tip of the loop corresponds to the maximum *H* of the cyclic variation. Three hysteresis loops are indicated in this figure. The portions of the loops for decreasing *H* lie above the portions for increasing *H*, which is the hysteresis lag typical of ferro and ferrimagnetic materials. The dotted curve passing through tips of the hysteresis loops is the *normal magnetisation curve* or *B-H curve* of the material. A typical magnetisation curve is provided in Fig. 5.10. It is initially nonlinear with a nearly linear portion in the middle and exhibits saturation for high values of *H*. For extremely high values of *H*, it possesses a slope corresponding to that of free space ($\mu_r = 1$). It is this *B-H* curve which is used in magnetic-circuit calculations and hysteresis effects, where necessary, are accounted for empirically. In fact, the *B-H* curve is appreciably affected by heat treatment and mechanical handling. High degree of precision therefore need not be attempted in these calculations.

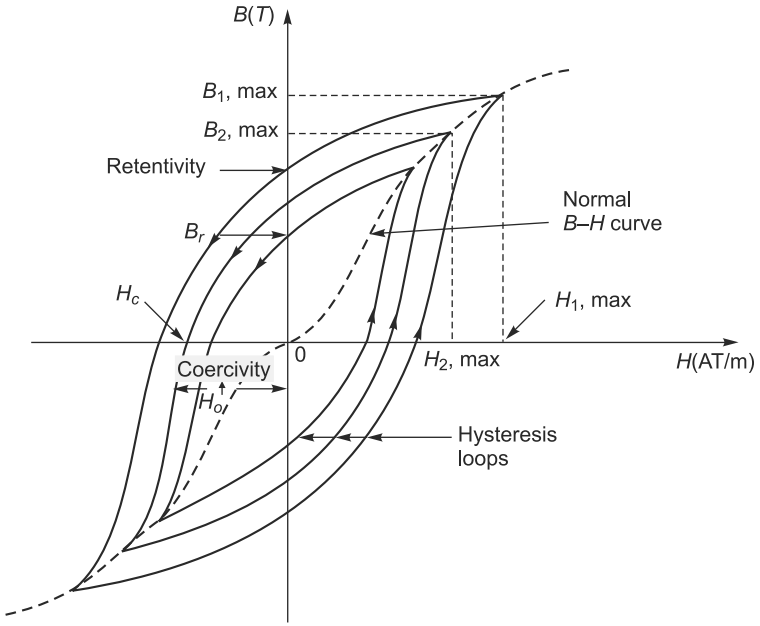


Fig. 5.9 *Hysteresis loop and magnetisation (B–H) curve*

In a *B-H* curve the value of the flux density at $H = 0$ is known as the *residual flux density* B_r. The value of *H* to reduce B_r to zero is called the *coercive force* H_c. The maximum possible value of B_r corresponding to deep saturation is know is as *retentivity* and the maximum value of H_0 is the *coercivity*. All these values are indicated in Fig. 5.9.

A ferrite material known as magnetic ceramic has a square hysteresis loop, which is substantially magnetically bistable as shown in Fig. 5.11. Square-loop materials are used in switching circuits, as storage elements in computers, and in special type of transformers in electronic circuits.

A small change magnetic force *H* caused full reversal of the flux density from $+B_r$ to $-B_r$ and vice versa. This can be recognised as I/O switching in computing circuit.

Typical magnetisation curves for important ferromagnetic materials are shown in Fig. 5.12. For economic reasons, magnetic circuits are designed with magnetic materials in a slightly saturated state.

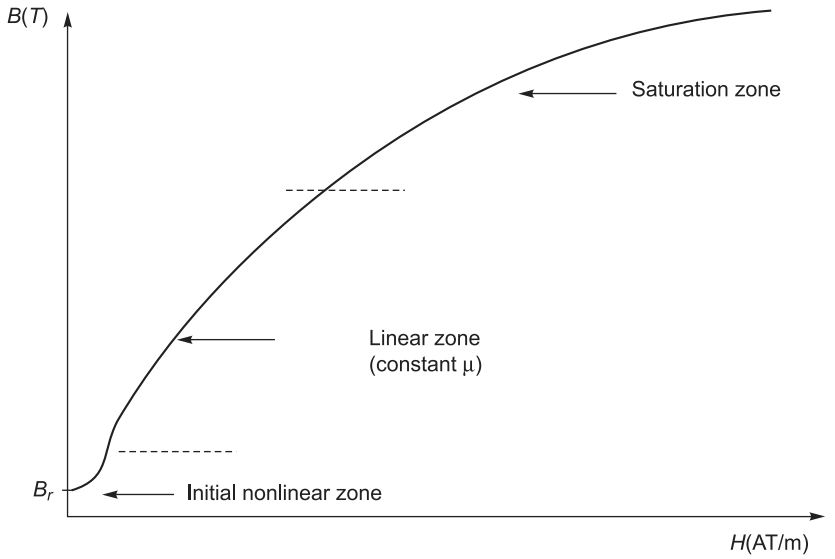


Fig. 5.10 *Typical normal magnetisation curve of ferromagnetic material*

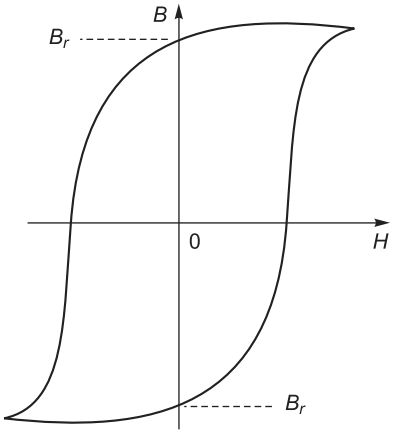


Fig. 5.11 *Square-loop magnetic material*

5.4.2 Sheet Steels

Transformers and such elements of electric machines that carry alternating flux are constructed from *silicon steel* in the form of thin sheets. Cores constructed from these sheets are called *laminated* cores with laminations of silicon steel. Addition of silicon in steel increases its electric resistivity thereby reducing eddy-current losses (Sec. 5.9). Laminating further greatly reduces eddy-current losses.

Steel has higher permeability in the direction of the edge of the cubic crystal. Steel sheets are therefore cold rolled so that all crystal edges align along the direction of rolling. These sheets are termed *Cold-Rolled Grain Oriented* (CRGO) steel. Laminations must be cut from sheet steel such that the direction of flux these are to carry is oriented along the sheet length.

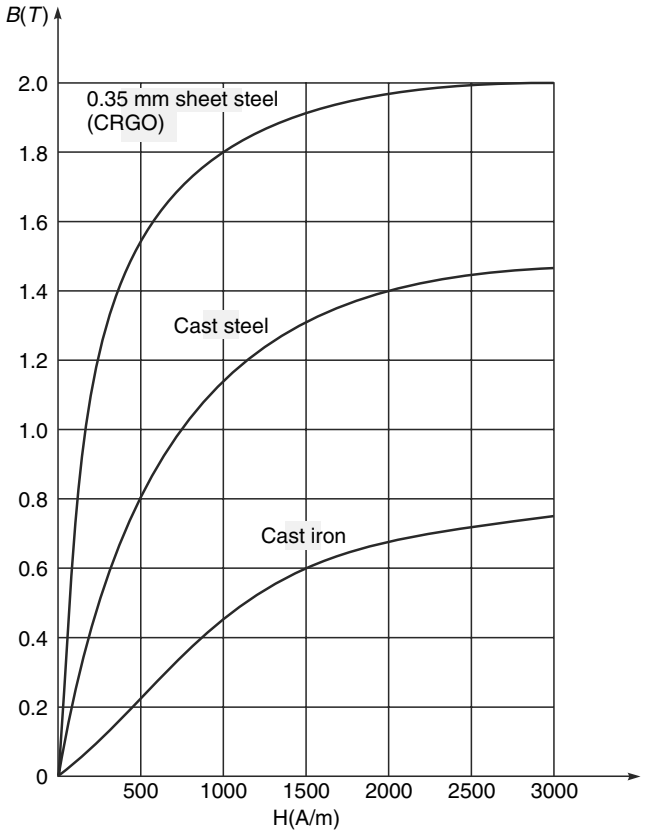


Fig. 5.12 *Magnetisation curves for important ferromagnetic materials*

5.5 ELECTROMAGNETIC INDUCTION AND FORCE

In this section, certain fundamental laws of electromagnetism will be enunciated and also certain rules will be put forth which are helpful in application of the laws.

5.5.1 Faraday's Law

Flux Linkages

If flux ϕ passes through all the N turns of a coil as shown in Fig. 5.13, the flux is said to link the coil.

The flux linkage of the coil are

$$\lambda = N\,\phi \text{ Weber-turns (Wb-T)} \tag{5.19}$$

The Faraday's law states that if the magnitude of the flux through the coil changes with time, an *emf* is induced in the coil which is given by

$$e = -\frac{\mathrm{d}\lambda}{\mathrm{d}t} = -N\frac{\mathrm{d}\phi}{\mathrm{d}t}\,V \tag{5.20}$$

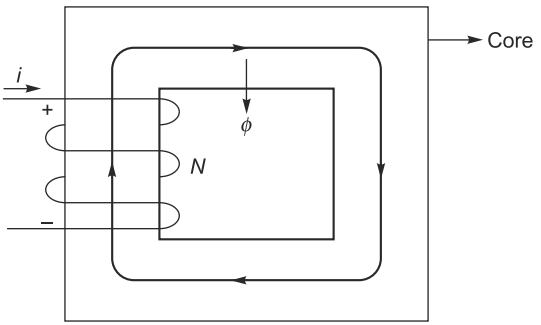


Fig. 5.13 *Flux ϕ passing through all N turns of a coil*

5.5.2 Lenz's Law

The negative sign in Eq. (5.20) means that the induced *emf* would tend to cause a current flow in the coil, which would oppose the change in flux (the original cause of emf induction). This statement is known as Lenz's law.

If the opposing polarity of emf is indicated on the coil terminals as in Fig. 5.13 then the Faraday's law need to give only the emf magnitude as

$$e = \frac{\mathrm{d}\lambda}{\mathrm{d}t} = N\frac{\mathrm{d}\phi}{\mathrm{d}t}\,V \tag{5.21}$$

Change in flux linkages of a coil may occur in two ways:

- The coil remains stationary and the flux through it changes with time. The emf so inducted is known as *statically induced emf* (*transformer emf*).
- Flux density distribution remains constant and stationary in space but the coil moves relative to it so as to change the flux linkages of the coil. The emf so inducted is known as *dynamically inducted emf* (*motional emf*).

Both the above processes of induction may occur simultaneously in a coil.

The dynamically induced emf in a conductor of length $l(m)$ placed at angle θ to a stationary magnetic field of flux density B(T) cutting across it at speed v(m/s) is given by

$$\begin{aligned} e &= |v \times B| l \text{ V} \\ &= Blv \sin\theta \text{ V} \end{aligned} \tag{5.22}$$

where θ is the angle between the direction of flux density and conductor velocity. In electric machines $\theta = 90°$, so that

$$e = Blv \text{ V} \tag{5.23}$$

This is known as the *flux-cutting rule* with the direction of emf given by $v \times B$ or by the well-known *Fleming's right-hand rule*.

Extend the thumb, first and second fingers of the right hand mutually at right angles to each other. If the thumb represents the direction of v (motion of conductor with respect to B), first finger the direction of B then the second finger gives the direction of emf along l (the conductor).

5.5.3 Lorentz Force Equation

Force of electromagnetic origin is given by

$$\mathbf{F} = l\,\mathbf{i} \times \mathbf{B} \text{ N} \tag{5.24}$$

where $\mathbf{F}$ is the force acting on a straight conductor of length l (m) carrying current i (A) placed in a uniform field of flux density B(T). The magnitude of force is given by

$$F = Bil \sin \theta \text{ N} \tag{5.25}$$

where direction is along $\mathbf{i} \times \mathbf{B}$ and θ is the angle between current direction and flux density. If $\theta = 90°$ as in electric machines

$$F = Bil \text{ N} \tag{5.26}$$

which is the well-known *Bil rule* or *Biot-Savart Law*.

The direction of force can also be found by the *Fleming's left-hand rule*.

Extend the thumb, first and second fingers of the left hand mutually at right angles to each other. If the thumb represents the direction of B, the second finger the direction of I then the first finger points in the direction of force on the conductor.

From Eq. (5.26), B can be imagined to have units of N/Am.

5.6 INDUCTANCE: SELF AND MUTUAL

5.6.1 Self-Inductance

Consider a coil of N turns wound on an iron core and carrying current i as shown in Fig. 5.14.

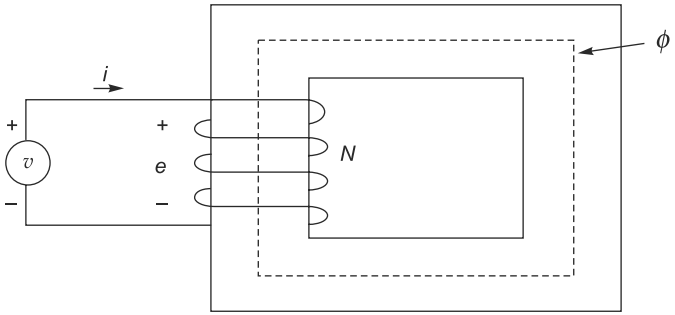


Fig. 5.14 *Self-inductance*

The coil creates flux ϕ in the core called *self-flux*, which is assumed to link all the N turns (no leakage). As the flux varies with time (caused by current varying with time) the emf induced in the coil called the *counter emf* is given by

$$e = N\frac{\mathrm{d}\phi}{\mathrm{d}t} = \frac{\mathrm{d}\lambda}{\mathrm{d}t} \text{ (opposing the current as per Lenz's law)}$$

$$= N\frac{\mathrm{d}\phi}{\mathrm{d}i}\cdot\frac{\mathrm{d}i}{\mathrm{d}t} \text{ V}$$

or

$$e = L\frac{\mathrm{d}i}{\mathrm{d}t} \text{ V}$$

where

$$L = N\frac{\mathrm{d}\phi}{\mathrm{d}t} = \frac{d\lambda}{di} \text{ H (henry)} \tag{5.27}$$

is called the *self-inductance* of the coil. The unit of inductance is henry (H) = WbT/A

Equation (5.27) is the general expression for the self-inductance of a coil at any point on the *B-H* curve of its core material. It indeed is the incremental inductance which corresponds to incremental change around and operating point on the curve.

For a *linear B-H* curve (material operated in the region of constant permeability or when the magnetic circuit has a dominant air gap), L is constant which can then be expressed as

$$L = N\frac{N\phi}{i} = \frac{\lambda}{i} \text{ H} \tag{5.28}$$

The coil flux linkages are then

$$\lambda = Li \tag{5.29}$$

From Eq. (5.28), we can derive alternative expressions for self-inductance.

$$L = \frac{N\phi}{i} = \frac{N^2\phi}{Ni}$$

But $Ni = Hl$ (Ampere's circuital law)

$$\therefore \qquad L = \frac{N^2BA}{Hl} = N^2\mu\frac{A}{l}$$

or
$$L = \frac{N^2}{\mathcal{R}} = \mathcal{P}N^2 \text{ H} \tag{5.30}$$

It is found from Eq. (5.30) that the coil self-inductance is independent of excitation current and depends upon the core geometry, permeability of the core's magnetic material and number of coil turns. In fact, inductance is proportional to the square of the number of turns of the coil.

In the general case when both the configuration and current in an inductive coil are considered then Eq. (5.29) of flux linkages modify to

$$\lambda = L(x)i \tag{5.31}$$

where x is a length / angle parameter.

The counter emf is then expressed as

$$e = \frac{\mathrm{d}\lambda}{\mathrm{d}t} = \frac{\mathrm{d}}{\mathrm{d}t}[L(x)i]$$

or
$$e = L\frac{\partial i}{\mathrm{d}t} + i\frac{\partial L}{\mathrm{d}t} \tag{5.32}$$

Inductance Core

For high inductance value, iron core with high permeability is used; see Eq. (5.30). However, in the *B-H* curve, nonlinearity causes the inductance value to vary for change in the operating point or for larger magnitude change in current value. Therefore, iron-cored inductance operation must be restricted to small current variations about the operating point. It is used in low-frequency power circuits.

For low value linear inductance, air core is used for high frequency electronic circuits.

5.6.2 Mutual Inductance

When two coils are wound on a common core or placed close to each other, a part of the flux produced by one coil also links the other coil as shown in Fig. 5.15. This leads to the concept of mutual inductance defined as

$$L_{12} \text{ (or } M_{12}) = \frac{\lambda_{12}}{i_2} H$$

$$L_{21} \text{ (or } M_{21}) = \frac{\lambda_{21}}{i_1} H \tag{5.33}$$

where λ_{12} = flux linkages of Coil 1 due to current in Coil 2
λ_{21} = flux linkages of Coil 2 due to current in Coil 1

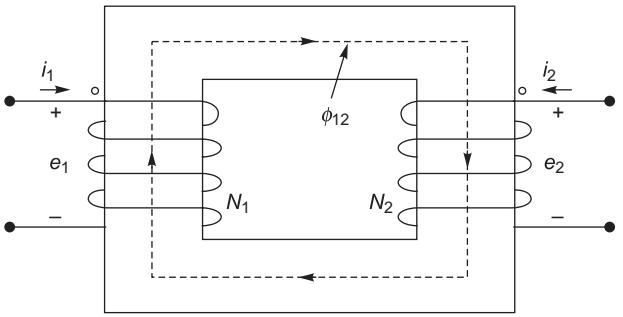


Fig. 5.15 *Mutual inductance*

For a bilateral magnetic circuit

$$M_{12} = M_{21} = M \tag{5.34}$$

In general, in a linear magnetic circuit,

$$M = k\sqrt{L_1 L_2} \tag{5.35}$$

where k is the *coefficient of coupling* (which can at most be unity). For a tight coupling,[4] i.e. all the flux linking both coils (no leakage)

$$M = \sqrt{L_1 L_2} \tag{5.36}$$

Dot Convention

Dots are used on the two coupled coils for similar terminals as shown in Fig. 5.16. Current flowing into the dotted terminal of each coil produces core flux in the same direction. If the flux varies with time, the dotted terminals have the same polarity of *emf induced*. The reader may check by assuming the flux to be increasing and applying Lenz's law.

[4] For tight coupling there is no leakage.

$$\phi_{21} = \frac{N_1 i_1}{\mathcal{R}}, \ \mathcal{R} = \text{reluctance of the magnetic circuit}$$

$$M_{21} = \frac{\phi_{21} N_2}{i_1} = \frac{N_1 N_2}{\mathcal{R}} = M_{12} = M$$

and $$L_1 = \frac{\phi_{12} N_1}{i_1} = \frac{N_1^2}{\mathcal{R}}$$

$$L_2 = \frac{N_1^2}{\mathcal{R}}$$

Hence, $$M = \sqrt{L_1 L_2}$$

When both coils are carrying current, the total flux linkages are given by

$$\lambda_1 = L_{11} i_1 + L_{12} i_2$$

$$\lambda_2 = L_{21} i_1 + L_{22} i_2 \tag{5.37}$$

where L_{11}, L_{22}, are self-inductance of the coils and L_{12}, L_{21} are mutual inductance of the coils (equal in a bilateral circuit).

The induced emf in each coil is given by[5]

$$e_1 = L_{11} \frac{di_1}{dt} + L_{12} \frac{di_2}{dt} \tag{5.38a}$$

$$e_2 = L_{21} \frac{di_1}{dt} + L_{22} \frac{di_2}{dt} \tag{5.38b}$$

From examination of the form of these equations, it easily follows that a mutually coupled coil can be modeled in the form of the circuit of Fig. 5.16 with self-inductances only. The reader can verify this by writing the two mesh equations.

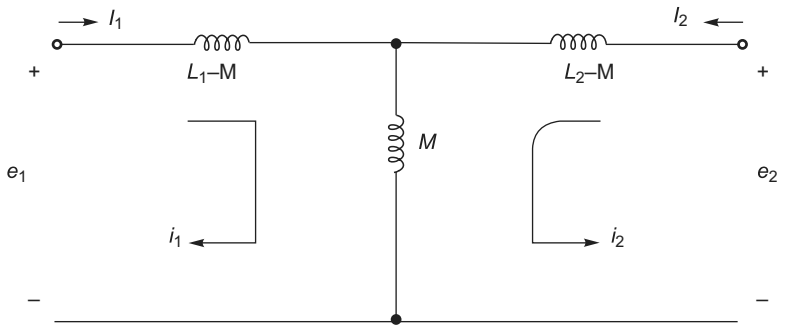


Fig. 5.16 *Dot Convention*

5.7 ENERGY STORED IN MAGNETIC SYSTEMS (LINEAR)

Figure 5.17 shows self-inductance (iron-cored) when the resistance r of the coil is lumped outside, so that L is devoid of any resistance (pure, lossless). The electrical energy drawn from the source gets stored in the magnetic system. In time

$$dW_e = ei dt = dW_f \tag{5.39}$$

where dW_f is the change in the field energy.

[5] These equations can be written in single suffix form as:

$$e_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$$

$$e_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt}$$

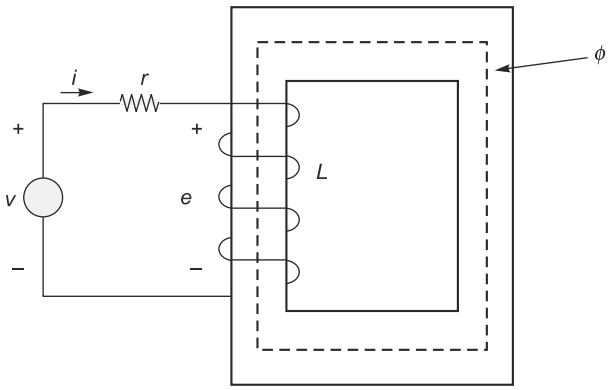


Fig. 5.17 *Self-inductance*

As $$e = \frac{\mathrm{d}\lambda}{\mathrm{d}t}$$

$$\therefore \quad dW_f = \mathrm{d}W_e = id\lambda$$

The energy absorbed by the magnetic system in establishing flux linkages λ from zero state is

$$W_f = \int_0^{\lambda} i\,\mathrm{d}\lambda$$

As $$\lambda = Li$$

$$\therefore \quad W_f = L\int_0^{i} i\,\mathrm{d}t$$

or $$W_f = \frac{1}{2}Li^2 = \frac{1}{2}i\lambda \tag{5.40}$$

This is the energy stored in the magnetic field.

The field energy expression of Eq. (5.40) can be written in term of magnetic system quantities using Eq. (5.30). Thus,

$$W_f = \frac{1}{2}\frac{N^2i^2}{\mathcal{R}\phi} = \frac{1}{2}\mathcal{R}\phi^2 \tag{5.41}$$

where $\mathcal{R}$ is the reluctance and ϕ is the flux established in the magnetic circuit.

In case of an air gap in the core, air-gap reluctance being far larger than that of the core, a major portion of the field energy would reside in the air gap.

Energy Stored in Mutual Inductance

For two coupled coils (both excited), Eq. (5.41) generalises to

$$W_f = \int_0^{\lambda_1} i_1\,\mathrm{d}\lambda_1 + \int_0^{\lambda_2} i_2\,\mathrm{d}\lambda_2 \tag{5.42}$$

From Eq. (5.37),

$$d\lambda_1 = L_{11} + \mathrm{d}i_1 + L_{12}\,\mathrm{d}i_2$$

$$d\lambda_2 = L_{21} + \mathrm{d}i_1 + L_{22}\mathrm{d}i_2$$

Substituting in Eq. (5.42) and taking $L_{21} = L_{12}$, we get

$$W_f = L_{11}\int i_1\, di_1 + L_{22}\int i_2\, di_2 + L_{12}\int (i_1\,\mathrm{d}i_2 + i_2\,\mathrm{d}i_1)$$

$$= \frac{1}{2}L_{11}i_1^2 + \frac{1}{2}L_{22}i_2^2 + L_{12}i_1 i_2 \tag{5.43}$$

Example 5.3

A cast-steel core shown in Fig. 5.18 has uniform cross section. It is wound with two coils. The coil 2 carries a current of 2 A.

(a) What should be the current of Coil 1 and its direction, for a core flux density 1.4 T in the direction indicated on the figure. For cast steel, μ_r = 3000.

(b) With both coils carrying currents as found in Part (a), find the energy stored in the core.

(c) Find the inductances L_1, L_2 and the mutual inductance between coils. There is no leakage of flux.

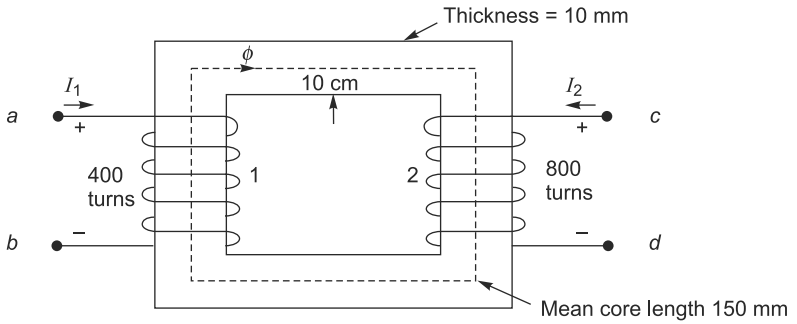


Fig. 5.18

Solution

(a) Core cross-sectional area, $A_c = (10 \times 10^{-2})\,(10 \times 10^{-3}) = 10^{-3}\mathrm{m}^2$

$B_c = 1.4$ T required,

Field intensity, $H_c = \dfrac{B_c}{\mu_0\mu_r} = \dfrac{1.4}{4\pi \times 10^{-7} \times 3000}$ AT/m

Total mmf needed, $F(\text{total}) = H_c l_c$

$$= \frac{1.4 \times 150 \times 10^{-12}}{4\pi \times 10^{-7} \times 3000} = 557\,\mathrm{AT}$$

Coil 2 produces $F_2 = 2 \times 800 = 1600$ AT

F (total) $= F_1 + F_2$

$557 = F_1 + 1600$

or $F_1 = -1043$ AT

It is found from the right-hand rule that F_2 produces flux in the desired direction. So, F_1 must oppose the flux.

$$\text{Required } I_1 = \frac{1043}{400} = 2.61 \text{ A}$$

The current direction is out of the terminal '*a*'.

(b) With coil currents as found in Part (a),

$$B_c = 1.4\ T$$

$$\phi_c = B_c A_c = 1.4 \times 10^{-3} \text{ Wb}$$

Core reluctance

$$\mathcal{R}_c = \frac{i_c}{\mu A_c} = \frac{150 \times 10^{-2}}{4\pi \times 10^{-7} \times 3000 \times 10^{-3}}$$

$$= 398 \times 10^3$$

Energy stored in core

$$W_f = \frac{1}{2} \mathcal{R}_c \phi_c^2$$

$$= \frac{1}{2} \times 398 \times 10^3 \times (1.4 \times 10^{-3})^2$$

or $W_f = 390$ mJ

(c) Self-inductance of Coil 1

$$L_1 = \frac{N_1^2}{\phi_c} = \frac{(400)^2}{398 \times 10^3} = 0.4\text{H}$$

Self-inductance of Coil 2

$$L_2 = \frac{N_2^2}{\phi_c} = \frac{(1600)^2}{398 \times 10^3} = 1.6\text{H}$$

As there is no leakage, mutual inductance is

$$M = \sqrt{L_1 L_2} = \sqrt{0.4 \times 1.6} = 0.8 \text{ H}$$

5.8 THE AC OPERATION OF MAGNETIC CIRCUITS

Consider an *N*-turn iron-core coil of Fig. 5.19 with ac excitation. The coil is assumed to be ideal with zero resistance. The induced emf in the coil must be sinusoidal for it to balance the ac applied voltage (KVL). This constrains the flux in the core to be sinusoidal. Let

$$\phi = \phi_{\max} \sin \omega t \tag{5.44}$$

where $\phi_{\max}$ = maximum core flux

$\omega = 2\pi f$ rad/s

f = frequency (of excitation) in Hz

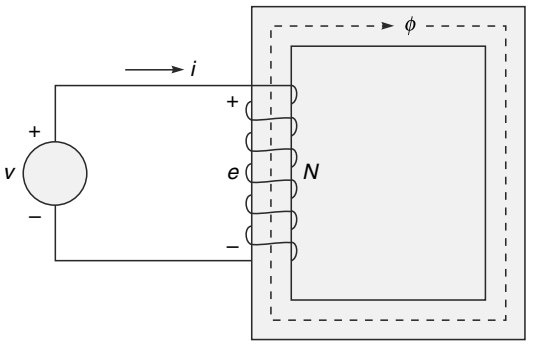


Fig. 5.19 *Magnetic circuit with ac excitation*

The coil induced emf as per Faraday's law is dz

$$v = e = N = \frac{\mathrm{d}\phi}{\mathrm{d}t} = \omega N \phi_{\max} \cos \omega t \tag{5.45}$$

and its rms value is

$$V = E = \frac{2\pi}{\mathrm{d}t} \phi N \phi_{\max} = 4.44 f N \phi_{\max} \tag{5.46}$$

or

$$V = E = 4.44 f N A_c B_{\max} \tag{5.47}$$

where A is the core area of cross-section.

It is seen from Eqs. (5.44) and (5.45) that the flux phasor lags the induced emf phasor by 90° as illustrated in phasor diagram of Fig. 5.20. This is because cos ωt leads sin ωt by 90°.

It is easily observed from Eqs. (5.45)/(5.46) that the maximum value of the core flux (sinusoidal) or flux density is dictated by the voltage applied to the coil (ideal). The excitation current[5] can then be found from the B–H curve of the core material. On the other hand, in dc excitation, the coil resistance determines the excitation current, which in turn decides the core flux density as per the B–H curve.

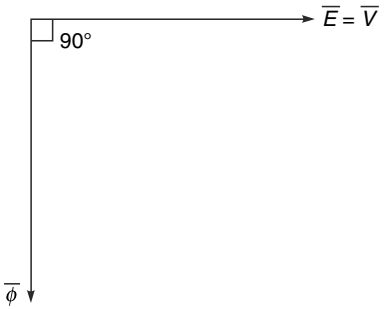


Fig. 5.20 *Phasor relationship of $\overline{E}$ ($=\overline{V}$) and $\overline{\phi}$*

Example 5.4

A ring of magnetic material has rectangular cross section. The inner diameter of the ring is 20 cm and the outer diameter is 25 cm, its thickness being 2 cm. An air gap of 1 mm length is cut across the ring. The ring is wound with 500 turns carrying a current of 2 A. The permeability of the magnetic material is 6000. Find the following:

(a) flux density in the air gap.
(b) inductance of the coil.
(c) energy stored in the magnetic material and in the air gap.

Neglect fringing and leakage.

[5]Excitation current would be sinusoidal for linear core (unsaturated), otherwise it would contain strong third harmonic (40%).

Solution

Area of cross section of ring = $\frac{5}{2} \times 2 = 5 \text{ cm}^2$

Mean length of ring = $\pi \times \left(\frac{20 + 25}{2} \right) - 0.1 = 70.6 \text{ cm}$

Length of air gap = 0.1 cm

Reluctance of ring $\mathcal{R}_r = \frac{70.6 \times 10^{-2}}{4\pi \times 10^{-7} \times 6000 \times 5 \times 10^{-4}} = 0.187 \times 10^6$

Reluctance of air gap $\mathcal{R}_g = \frac{0.1 \times 10^{-2}}{4\pi \times 10^{-7} \times 5 \times 10^{-4}} = 1.59 \times 10^6$

$\mathcal{R}$(total) = (0.187 + 1.59)106 = 1.78×10^6

Coil mmf $F = 2 \times 500 = 1000$ AT

$\phi = \mathcal{F}/\mathcal{R}(\text{total}) = \frac{1000 \times 10^3}{1.78 \times 10^6} = 0.562$ mWb

(a) $B(\text{air gap}) = \frac{0.562 \times 10^{-3}}{5 \times 10^{-4}} = 1.124$ T

(b) $L = \frac{\lambda}{i} = \frac{0.562 \times 10^{-3} \times 500}{2} = 140.5$ mH

(c) From Eq. (5.41),

$$W_f(\text{magnetic material}) = \frac{1}{2} \mathcal{R}_r \phi^2$$

$$= \frac{1}{2} \times 0.187 \times 10^6 \times (0.562)^2 \times 10^{-6} = 0.03 \text{ J}$$

$$W_f(\text{air gap}) = \frac{1}{2} \mathcal{R}_g \phi^2$$

$$= \frac{1}{2} \times 1.59 \times 10^6 \times (0.562)^2 \times 10^{-6} = 0.25 \text{ J}$$

Observe that energy stored in the magnetic ring is only 11% of the total energy stored in the magnetic circuit (ring + air gap).

5.9 HYSTERESIS AND EDDY-CURRENT LOSSES

When magnetic materials undergo cyclic variations of flux density, hysteresis and eddy-current power losses occur in them, which are together known as *core loss*, and appear in the form of heat. The core loss is important in determining temperature rise, rating and efficiency of transformers, machines and other ac-operated electromagnetic devices.

5.9.1 Hysteresis Loss

With reference to the hysteresis loop of Fig. 5.21, the energy absorbed by a ferromagnetic material per unit volume[6] as H is raised from zero to H_{max} is

$$\int_{-B_r}^{B_{max}} H\,dB = \text{area of } b_{go}$$

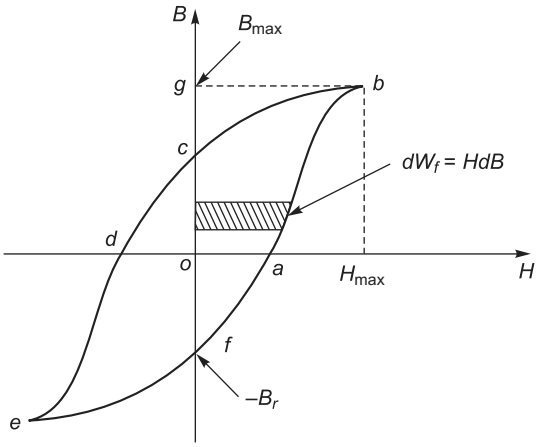


Fig. 5.21 *Hysteresis loss*

As H is reduced to zero, energy from the magnetic field is returned to the source of excitation as dB is now negative. Per unit value of energy returned is

$$\int_{B_{max}}^{0} H\,dB = \text{area of } b_{go}$$

In half cycle of H, variation energy not recovered from the material is the area of bco. In one complete cycle of variation, energy lost per unit volume is the area of the hysteresis loop.

It is established empirically that for a given volume of material, power loss on account of hysteresis is

$$P_h = k_h f B_{max}^n \text{ V W} \tag{5.48}$$

where k_h = characteristic constant of core material
n = *Steinmetz exponent*; range 1.5–2.0; typical value 1.6
V = volume of the material (m^3)

5.9.2 Eddy-Current Loss

Since core is made of conducting material, voltages induced in it by alternating flux produce circulating currents in iron. These are called *eddy currents* and are accompanied by i^2r loss which is called eddy-

6

$$W_f = \int_0^{\lambda} i\,dx = \int_0^{B} \left(\frac{Hl}{N}\right)(AN)\,dB = Al\int_0^{B} H\,dB$$

$$W_f \text{ (energy/unit volume)} = \frac{W_f}{Al}\int_0^{B} H\,dB \text{ J/m}^3$$

current loss. As induced voltages and currents are proportional to frequency and flux density (Eq. 5.47), it is reasonable to expect that the power loss will vary as

$$P_e = k_e f^2 B^2_{\max} \text{VW} \tag{5.49}$$

$$W_f = \int_0^{\lambda} i\, d\lambda$$

$$= \int_0^B \left(\frac{Hl}{N}\right)(AN)\,\mathrm{d}B = Al\int_0^B H\,\mathrm{d}B$$

$$W_t \text{ (energy/unit volume)} = W_f/Al = \int_0^B H\,\mathrm{d}B \text{ J/m}^3$$

when flux varies sinusoidally; k_e, being the characteristic constant of the core, depends upon effective resistance and length of eddy-current paths.

Thus, there are two methods used in practice to reduce the eddy-current loss considerably.

❑ **Silicon Steel** Silicon steel produced by adding 4% silicon to iron has much higher resistivity. The increased resistance of eddy-current paths reduces the resistive loss which is $i^2r = v^2/r$ for given induced voltage.

❑ **Laminating Steel** To increase the path lengths of eddy currents, the steel is cut into thin laminations (0.35 mm) along the flux paths. The laminations are lightly insulated from each other by varnish. This restricts the eddy currents to individual lamination resulting in very much elongated eddy paths and consequent reduction in eddy-current loss.

❑ **Screening Effect** The eddy currents produce their own flux in the core, which by Lenz's law pushes the main flux away from the core centre, making the flux density at the centre lower than that near the core surface. This screening effect of eddy currents is negligible at lower frequencies but may be of great importance at high frequencies as it effectively reduces the core cross section.

Example 5.5

For the magnetic circuit of Fig. 5.22, find $\bar{I}_2, \bar{V}_2$ and $\bar{V}_2/\bar{V}_1$.

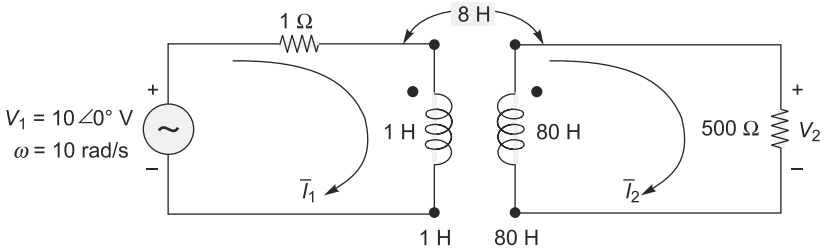


Fig. 5.22

Solution Writing the mesh equation for the two meshes, we have

$$(1 + j10 \times 1)\bar{I}_1 - j10 \times 8\bar{I}_2 = 10\angle 0° \text{(Mesh 1)}$$

$$(1 + j10)\bar{I}_1 - j80\bar{I}_2 = 10\angle 0° \tag{i}$$

$$-j10 \times 8\bar{I}_1 + (500 + j10 \times 80)\bar{I}_2 = 0 \text{ (Mesh 2)}$$

or $$j80\,\bar{I}_1 - (500 + j800)\bar{I}_2 = 0 \quad \text{(ii)}$$

From Eq. (ii), we get

$$\bar{I}_1 = [(500 + j800)/(j80)]\,\bar{I}_2 = (10 - j6.25)\bar{I}_2$$

Substituting Eq. (ii) in Eq. (i), we get

$$[(1 + j10)(10 - j6.25) - j80]\bar{I}_2 = 10 \angle 0° \quad \text{(iii)}$$

or $$\bar{I}_2 = 0.135 \angle -10.7° \text{ A} \quad \text{(iv)}$$

$\therefore$ $$\bar{V}_2 = 500\,\bar{I}_2 = 68 \angle -10.7° \quad \text{(v)}$$

$\therefore$ $$\bar{V}_2/\bar{V}_1 = 6.8 \angle -10.7°$$

Summary

- Ampere's law states that

  $F = \left(\frac{\mu i_1}{2\pi r}\right) i_2 l$ N; MKS units

  i_1 = current in a very long conductor
  $i_2 l$ = elemental current
  μ = permeability of medium
  r = distance of $i_2 l$ from the long conductor
  F acts redically outwards

- Flux density (B) is given by

  $$B = \mu\left(\frac{i_1}{2\pi r}\right) \text{ N/Am}$$

  Then $F = B\, i_2 l$ N

- Magnetic field intensity (H) is given by

  $$H = \left(\frac{i_1}{2\pi r}\right) \text{A/m}$$

  $i_1 = N\, i$, (AT); N = number of turns

  In engineering units,

  $$H = \frac{Ni}{l} \text{ AT/m}$$

  where l = length of closed flux path

- Flux is a closed magnetic line around a current such that H is tangential to it at every point.
- Direction of flux is determined by the right-hand rule.
- Flux density (B) is given by

  $B = \mu H$ Wb/m^2, tesla (T)

  where permeability of medium $\mu = \mu_0\, \mu_r$

  μ_0 = permeability of free space
  $= 4\pi \times 10^{-7}$ Wb/Am

μ_r = relative permeability of medium

- Both *B* and *H* are vectors.
  In magnetic fields of simple geometry, we deal only with their magnitudes.
- Magnetic flux piercing a surface is given by $\phi = BA$; *B* normal to area *A*. In general $\phi = BA \cos\theta$; *B* makes an angle θ with normal to *A*.
- Magnetomotive force (mmf) – Ampere-turns (AT) is also called magnetic potential; Symbol $\mathcal{F}$

  $\mathcal{F} = Hl$ AT

  l = length of flux line
- Flux around a core is given by $\phi = \frac{\mathcal{F}}{\mathcal{R}}$ Wb

  where

  Reluctance, $\mathcal{R} = \frac{1}{\mu A}$

  Permeance, $\mathcal{P} = \frac{1}{\mathcal{R}} = \frac{\mu A}{l}$

  Its dc analog is
  $\mathcal{F}$ ~ *dc* voltage (potential)
  ϕ ~ current
  $\mathcal{R}$ ~ resistance
- *B-H* characteristic of magnetic material; exhibits saturation and hysteresis. Normal magnetisation curve is used in magnetic circuit calculations.
- Terms of importance in *B-H*: characteristic residual flux, coercive force, retentivity; coercivity
- Faraday's law:

  Flux linkages $\lambda = \phi N$ Wb – *T*

  $e = \Theta \frac{d\lambda}{dt} = -N \frac{d\phi}{dt}$ *V*
- Lenz's law: The emf in Faraday's law opposes the change in flux ϕ
- Flux cutting rule: $e = Blv$ *V*
  Apply Fleming's right-hand rule for direction of emf.
- Lorentz force equation: $F = Bil$ N
  Apply *Bil* rule for Fleming's left-hand rule for direction of force.
- Self-inductance

  $L = N \frac{d\phi}{dt} = \frac{d\lambda}{dt}$ H

  $e = N \frac{di}{dt}$ *V*

  For linear case, $L = \frac{N\phi}{i} = \frac{\lambda}{i}$ H

  Also, $L = \frac{N^2}{\mathcal{R}}$ H
- Mutual inductance: $M_{12} = \frac{\lambda_{12}}{i_2}$, $M_{21} = \frac{\lambda_{21}}{i_1} H$

For bilateral magnetic circuit,

$M = M_{12} = M_{21} = k\sqrt{L_1 L_2}$, k = coupling coefficient

For tight coupling, $M = \sqrt{L_1 L_2}$

➢ Energy stored in magnetic field

$$W_f = \frac{1}{2} i\lambda = \frac{1}{2} Li^2 \text{ J}$$

or $$W_f = \frac{1}{2} \frac{N^2 i^2}{R} = \frac{1}{2} \phi^2 R \text{ J}$$

In a magnetic circuit with air gap, a major portion of the field energy resisdes in the air gap.

Exercises

Review Questions

1. State Ampere's law. How do you use the law to define a flux line and flux density?
2. Define the main magnetic quantities needed to deal with magnetic circuits. How are these inter-related?
3. What is the magnetic force which creates magnetic flux density? What name is used for it?
4. Write the expression for B at distance r from a long conductor carrying current i. What is the path along which B is constant and its direction?
5. In Question 4, a conductor of length l carries current i in the same direction as the long conductor and is parallel to it. What is the force on it and its direction? Use the left-hand rule.
6. What is permeability and relative permeability? What are the magnetic quantities it relates?
7. State Ampere's circuit law. How is it used in magnetic circuit analysis?
8. State the Ohm's law of magnetic circuit.
9. Explain what is magnetomotive force and compare it with electromotive force.
10. Define magnetic circuit reluctance and how is it analogous to electric circuit resistance? Can we use series/parallel combinations of reluctance?
11. In a magnetic circuit, the core has an air gap. Why is the reluctance of the air gap much higher than the rest of the circuit?
12. For a magnetic core with air gap, linear analysis yields acceptable result. Justify.
13. Write the expression for energy stored magnetic field. Convert the expression to energy density form.
14. In a magnetic core with air gap carrying flux ϕ, why does major portion of the stored energy reside in the air gap.
15. State the dot convention for mutually coupled coil in terms of the flux direction and also in terms of emf induced if the flux is varying.
16. For the couple circuit of Fig. 5.23, place the dot on each coil.
17. Distinguish between leakage flux and fringing flux. How are these accounted for empirically?

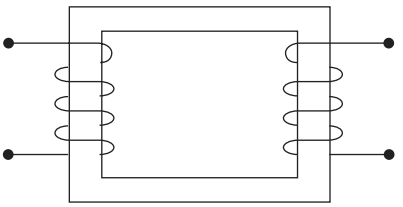


Fig. 5.23

Problems

1. A coil of 1000 turns is wound on a laminated core of sheet steel having a cross section of 25 cm^2 and a mean length of 50 cm. The stacking factor is 0.90. What is the current required to produce a core flux of 3 mWb? Use the magnetisation curve of Fig. 5.10.

Hint: *Stacking factor* = net area of cross section of steel/gross area of core cross section.

2. An air gap of 2 mm length is cut at right angles to the core cross section in the case of Problem 1. What should be the value of coil current to maintain the same flux density? Neglect fringing.
3. The coil current in Problem 2 is adjusted to 1.5 A. Find the total core flux.

   $Hint: AT = \frac{B_c}{\mu_0} l_g + H_c l_c$; $(B_g = B_c)$; $AT = 1000 \times 1.5 = 1500$

   $B_c = f(H_s)$, the magnetisation curve

   Solve these two equations numerically or graphically.
4. Solve Prob. 5.2 if the air gap of 2 mm length is cut at an angle of 45°.
5. In the magnetic circuit of Fig. 5.24, the coil $\mathcal{F}_2$ is supplying 500 AT in the direction indicated. Find the AT (in magnitude and direction) that the coil $\mathcal{F}_1$ must provide to produce a flux of 4 mWb in the air gap in the central limb from *A* to *B*. The relative permeability of the core is 4500.

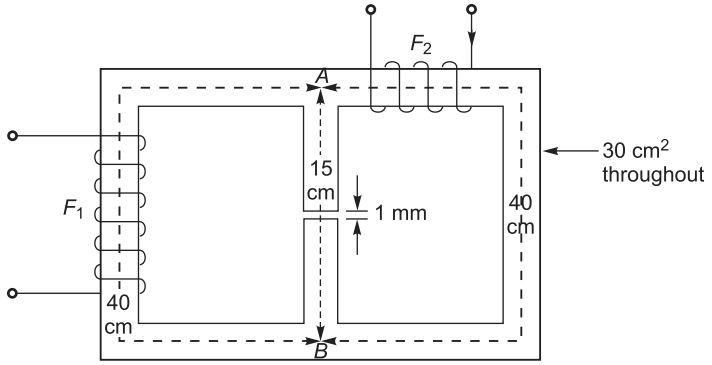


Fig. 5.24

6. For the magnetic circuit shown in Fig. 5.25, the magnetisation curve of the core is as follows:

H(AT/m)	200	400	500	600	800	1000	1400
B(T)	0.46	0.87	0.98	1.08	1.23	1.33	1.48

Calculate the exciting current required to create a flux of 0.25 mWb in the air gap. What is the flux in the central limb?

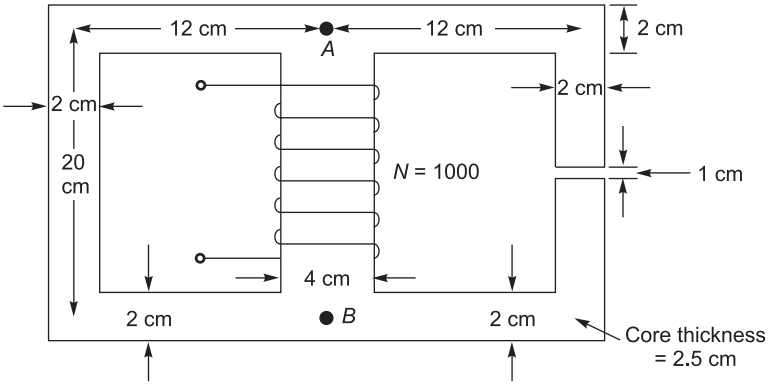


Fig. 5.25

7. In the magnetic circuit shown in Fig. 5.26, the area of cross section of the central limb is 12 cm^2 and that of each outer limb (A to B) is 6 cm^2. A coil current 0.5 A produces 0.5 mWb in the air gap. Find the relative permeability of the core material.

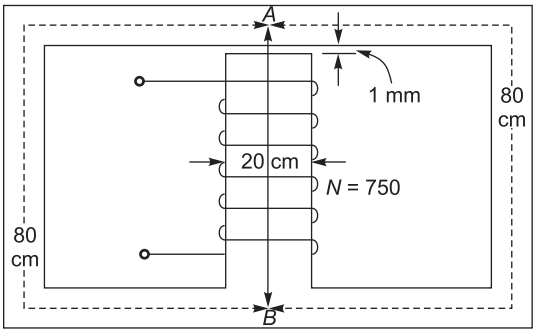


Fig. 5.26

8. For the magnetic circuit of Fig. 5.27.
   (a) Calculate the energy stored in the core and in the air gap for a coil current of 4 A. What will these values be if $\mu_r = \infty$?
   (b) Calculate the excitation current and induced emf in the coil to produce a flux of 0.4 sin 314 t mWb in the air gap.
   (c) Calculate the inductance of the coil. What will be its value for $\mu_r = \infty$?

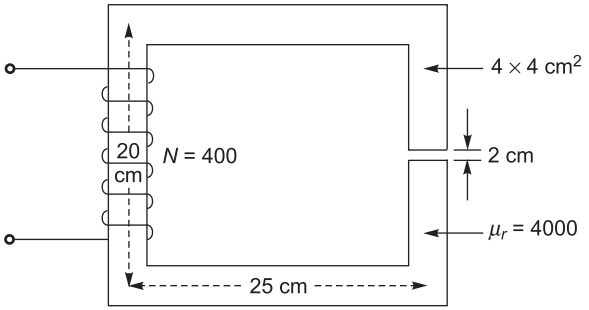


Fig. 5.27

Multiple-Choice Questions

1. Silicon steel is used for transformer core because
   (a) it reduces hysteresis loss
   (b) it reduces eddy-current loss
   (c) it increases core permeability
   (d) it reduces magnetostriction noise
2. Transformer care is built from this stampings because
   (a) it reduces eddy-current loss
   (b) it reduces hysteresis loss
   (c) it reduces both hysteresis and eddy-current loss
   (d) it increases the mechanical strength of the core

3. Maximum flux established in an ac-excited iron core is determined by
   (a) impressed frequency coil
   (b) impressed voltage only
   (c) both impressed voltage and frequency
   (d) reluctance of the core
4. The unit of flux density is
   (a) Tesla (b) ATH/m^2
   (c) Wb/m^2 (d) All three are equivalent
5. The unit of inductance is
   (a) Wb T/A (b) Vs/A
   (c) H-turns^2 (d) All three are equivalent
6. Eddy current guess are proportional to (of = frequency, B = flux density, t = laminative thickness)
   (a) f, B, t (b) f, B, t^2 (c) f, B^2, t^2 (d) f^2, B^2, t^2
7. Magnetostriction noise in ferromagnetic materials is caused by
   (a) hysteresis loss
   (b) eddy-current loss
   (c) changes in linear dimensions of crystals under dc excitation
   (d) changes in linear dimension of crystals under ac excitation
8. A coil of 1000 runs is wound on a core and a current of 1A flowing through the coil creates a core flux of 1 mWb. The energy stored in the magnetic field is
   (a) 1/a J (b) 1/2 J (c) 1 J (d) 1 2 J
9. In magnetic circuit, a current of 1 A flowing in the exciting winding produces flux of 1 Wb. If the circuit reluctance is doubled, the exciting current should be
   (a) 2 A (b) 0.5 A (c) 1 A (d) 1.5 A
10. A coil wound on a magnetic core is excited from an ac voltage source. The source voltage and its frequency are both doubled and the eddy-current loss in the core will become
   (a) half (b) remains same (c) double (d) four times

Answers

Multiple-Choice Questions

1. (b) 2. (a) 3. (c) 4. (d) 5. (d)
6. (d) 7. (a) 8. (b) 9. (a) 10. (d)

Transformers

chapter 6

Goals & Objectives

- Transformer, static device, transformation of voltage/current levels and need thereof
- Constructional features, materials
- Ideal transformer, relationship, impedance transformation
- Real transformer, development of circuit model (equivalent circuit), referring circuit parameter from one to the other side
- Determination of circuit model parameters
- PU system—choice of bases
- The performance indices—voltage regulation, efficiency
- Three-phase transformer connection

6.1 INTRODUCTION

Economical and technologically feasible voltage levels at which large chunks of electric power can be generated are typically 11–37 kV, while the most convenient utilisation voltages are 230/400 V for industrial, commercial and domestic purposes. Large industrial motors may run at 3.3, 6.6 or 11 kV. It is impossible to transmit directly, the electric power as it is generated (11–37 kV), even over modest distances. Unacceptably large power losses and voltage drops would result. As a rule of thumb, economical transmission voltage is 0.625 kV/km line-to-line, e.g. 400 kV for a line of about 640 km. It is therefore essential to *step-up voltages* at the sending (generating) end and to *step-down* at the receiving end. Usually more than one-step of step-down may be necessary. Step-up and step-down of voltage levels is accomplished by means of static electromagnetic devices called *transformers*.

The schematic diagram of a transformer is shown in Fig. 6.1. It comprises of a rectangular core, which has coils (windings) wound on the two lines and is indeed a mutually coupled circuit.

The coil excited from the ac source is called the *primary* and receives electric power from the source. The other coil is called the *secondary* and the voltage induced in it could be used to feed a load. The subscript '1' will be associated with the primary and '2' with the secondary. Primary and secondary roles in a transformer are easily reversed by the prevailing electrical conditions at the two ports. To avoid confusion, in practice, the two transformer coils are known as *HV* (*high-voltage*) and *LV* (*low-voltage*) windings.

Also shown in Fig. 6.1 are the mutual and leakage flux paths. Since a significant part of the leakage flux paths is through air, leakage fluxes ϕ_{11} and ϕ_{12} are much less than the mutual flux ϕ.

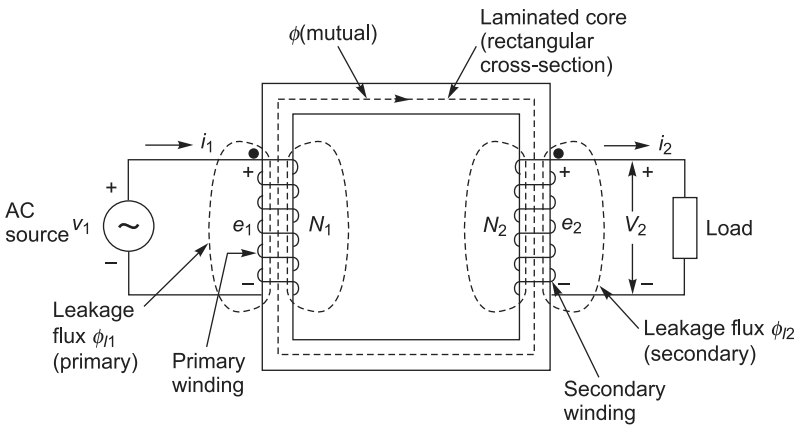


Fig. 6.1 *A two-winding transformer*

The *dots* indicated on the two coils (windings) are the polarity marks. As the mutual flux alternates, these coil ends simultaneously acquire the same polarity. Also, current flowing into the dot in one coil and out of the dot in the other coil would tend to produce core flux in the opposite directions.

The primary and secondary windings are made of *copper/aluminum* conductors.

6.1.1 Transformer Core

The transformer core is made of highly permeable iron. It is essential, so that excitation current required to establish core flux ϕ is a small percentage (2–4) of the primary current i_1; the rest being the useful component which corresponds to the load current. Further high permeable core provides tight coupling between the two windings, i.e. leakage flux is kept very low.

As the core carries alternating flux to keep low the eddy-current loss, the core is constructed with silicon steel laminations lightly insulated in the form of rectangular strips (0.35 mm thickness for 50 Hz). This type of construction is used for power transformers operated at 25–400 Hz. Core-type transformer construction is shown in Fig. 6.2(a). With some refinements, this core construction is used for audio transformers, (20 to 2000 Hz.) For transformers in electronic circuit operating at hundreds of kHz, powdered iron 'slug' is used as core with loose coupling as shown in Fig. 6.2(b). Air-cored transformers are used for radio devices and certain type of measuring and testing instruments.

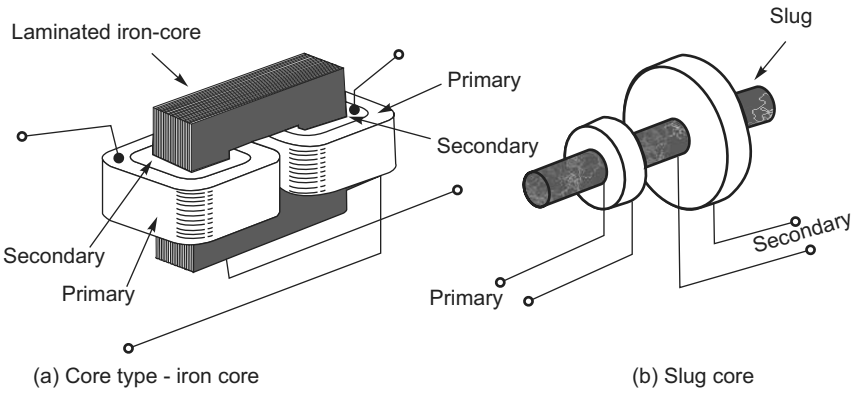


Fig. 6.2 *Transformer core types—single phase*

6.1.2 Core Types

Two types of geometrical core shapes and winding arrangements are used practically—*core type* and *shell type* as shown in cross-sectional views of Fig. 6.3 (a) and (b) of a single-phase transformer. It is easily seen, that core type has a longer mean flux path but a shorter mean length of coil turn.

The winding arrangement must be such as to reduce the leakage flux, which we will see later, causes reactive voltage drops in both primary and secondary. In a core type transformer to reduce the leakage flux, half-LV and half-HV are wound on each limb as shown in Fig. 6.3(a). For economical insulation, the LV coils are placed inside (adjoining the core) and HV coils are placed outside.

In a shell-type transformer, there are three limbs with both windings placed on the central limb as shown in Fig. 6.3(b). Half of the flux of the central limb is returned though each outer limb. To reduce leakage, LV and HV coil packets are sandwiched.

As per the statement in the first paragraph above, the core-type construction requires more iron but less copper. Therefore, this construction type is preferred, while the shell is used for special requirements (explanation beyond the scope of this book).

Housing and Cooling

To prevent ingress of moisture and deterioration of winding insulation, the built-in core and windings are placed in a steel tank filled with *transformer* oil as shown in Fig. 6.3(a). Oval or circular tubes are provided on the outside surfaces of the transformer tank, aiding in natural circulations of oil, which removes the heat of core and winding (I^2R) losses and transports it to the tank surfaces for cooling purpose. Oil circulation removes the heat generated by iron losses in the core. To prevent the coil from absorbing moisture from air and from being oxidised, the tank must be sealed and connected to the atmosphere through a narrow passage for breathing purposes. Inside this passage is placed silica gel for drying the air that the transformer breathes in. In large transformers forced cooling is provided by an oil pump outside the tank.

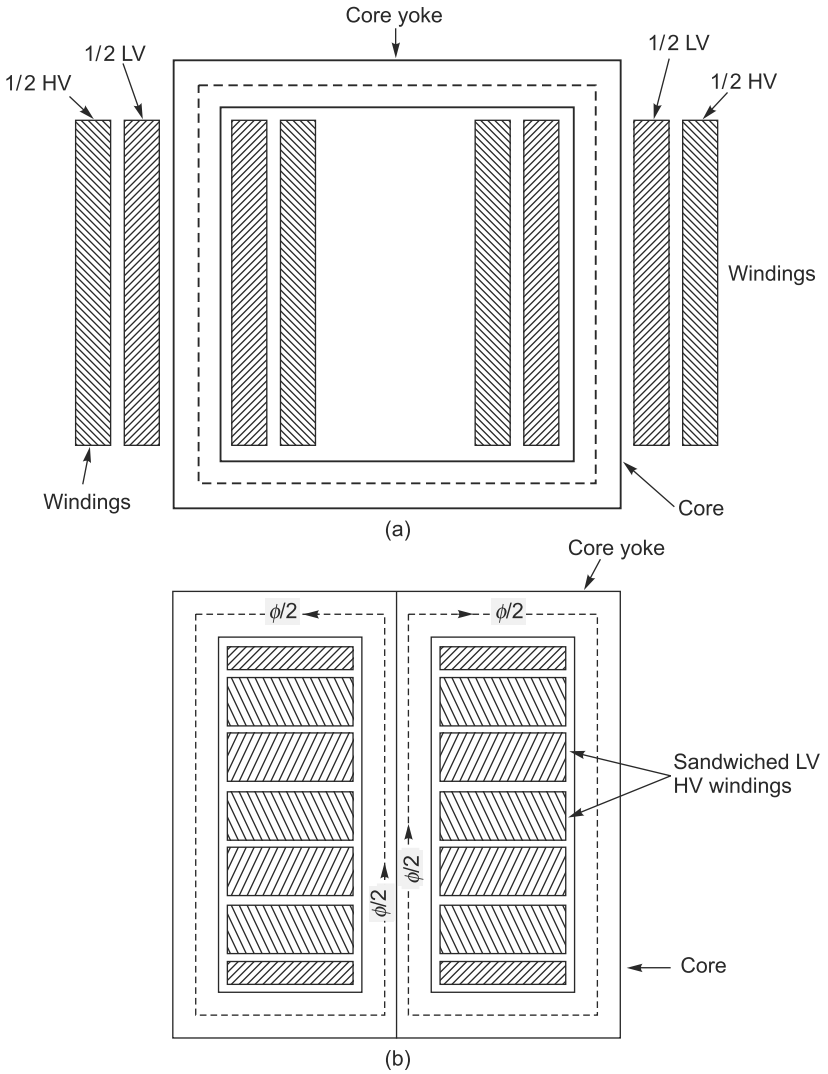


Fig. 6.3 *(a) Core-type transformer (b) Shell-type transformer*

6.1.3 Insulation

Windings made of copper/aluminum conductor (round/strip) are insulated by braided cotton, cotton tape, empire tape, etc. and then impregnated with varnish under vacuum to displace air packets inside the insulation. Windings are insulated from the core by means of Bakelite cylinders and plastic spacers are also insulated from each other. Such insulation must be spaced to allow free space for circulation of coil.

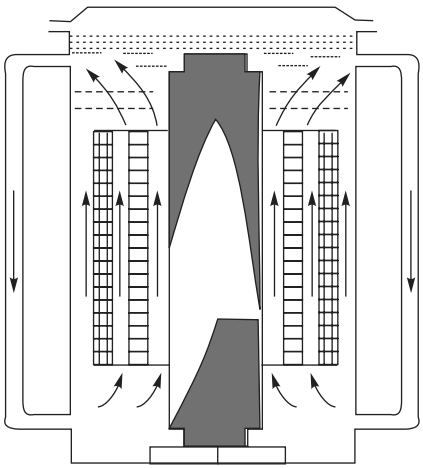


Fig. 6.4 *Natural cooling in transformers*

6.2 IDEAL TRANSFORMER (IT)

In order to develop the mathematical model of a transformer, it is convenient to visualise a circuit element termed the "ideal" transformer by making certain assumptions in the realistic transformer. These assumptions only introduce insignificant model errors and are as follows:

- The transformer windings are resistance-less. This in effect means that ohmic power losses and resistance voltage drops in the actual transformer are neglected.
- The transformer core material has infinite permeability so that it requires zero mmf to create flux in the core.
- The leakage flux is negligible, i.e. no reactive voltage drops in windings.
- The transformer core losses are negligible.

The diagrammatic representation of an ideal transformer is provided in Fig. 6.5 showing the core to carry mutual flux, primary winding connected to sinusoidal voltage and secondary winding connected to a load. As the source voltage applied to the primary is sinusoidal, all voltage and current in this electromagnetic device are sinusoidal whose instantaneous values are indicated on the diagram. Using standard symbols, we can write these as rms value or as phasor.

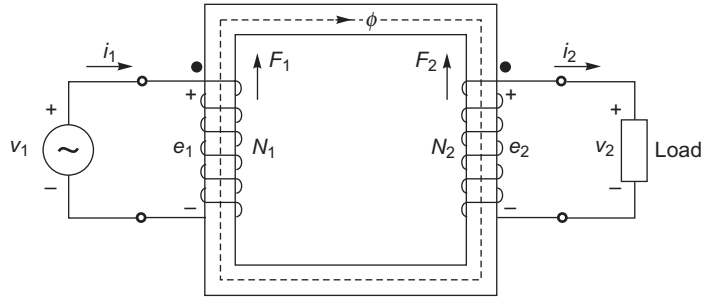


Fig. 6.5 *Ideal transformer (IT)*

6.2.1 Voltages and emfs

As the primary and secondary circuits are linked through the mutual flux, we begin with flux, which is expressed as

$$\phi = \phi_{\max} \sin wt;\ \omega = 2\pi f \text{ rad/s} \tag{6.1}$$

The emf induced in primary winding balances the applied voltage as per KVL.

Thus, $$v_1 = e_1 = N_1 \frac{d\phi}{dt} = \omega N_1 \phi_{\max} \cos \omega t \tag{6.2}$$

The secondary induces emf, which equals the load voltage and is similarly given by

$$v_2 = e_2 = \omega N_2 \phi_{\max} \cos \omega t \tag{6.3}$$

In terms of rms values,

$$V_1 = E_1 = \sqrt{2}\,\pi f N_1 \phi_{\max} \tag{6.4}$$

and $$V_2 = E_2 = \sqrt{2}\,\pi f N_2 \phi_{\max} \tag{6.5}$$

We find that the voltage and emfs are in phase and the flux lags by 90° (sin *wt* lags cos ωt by 90°).

6.2.2 Transformation Ratio

It is found from the above equations that the voltage transformation ratio of rms values is

$$\frac{V_1}{V_2} = \frac{E_1}{E_2} = \frac{N_1}{N_2} = a \text{ (turn ratio)} \tag{6.6}$$

It is seen from these equations that in an ideal transformer, the voltages are in direct ratio of turns with no change in phase angle.

The maximum value of the flux is found from Eqs (6.4) and (6.5) to be

$$\phi_{\max} = \frac{E_1}{\sqrt{2}\pi f N_1} = \frac{E_2}{\sqrt{2}\pi f N_2};\ \sqrt{2}\pi = 4.44 \tag{6.7}$$

It is seen that $\phi_{\max}$ is determined by the applied voltage and its frequency and is independent of current. This is a general result and as we shall see in later chapters, applies also to ac machines.

The phasor diagram showing the primary and secondary voltage including emfs and flux is drawn in Fig. 6.6 wherein, as said already, the flux phasor Φ lags $\bar{E}_1$ and $\bar{E}_2$, by 90°.

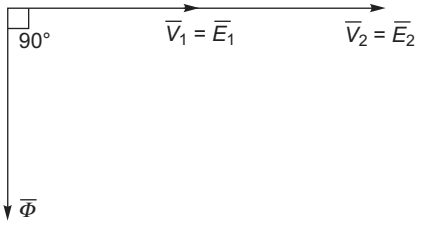


Fig. 6.6 *Phasor diagrams of ideal transformer, currents not shown*

Currents

The current drawn by the secondary load is

$$i_2 = \sqrt{2}\, I_2 \cos (wt - \theta);\ \theta = \text{phase angle assumed lagging} \tag{6.8}$$

By Lenz's law, this current causes the mmf to oppose the core flux ϕ. In phasor terms, secondary mmf is

$$\bar{F}_2 = \bar{I}_2 N_2, \bar{I}_2 = I_2 \angle -\theta \tag{6.9}$$

As the core flux cannot change, being governed by primary applied voltage and frequency, a current is drawn from the source to cause mmf $\bar{F}_1$ equal and opposite to $\bar{F}_2$.

Thus, $\bar{F}_1 = \bar{F}_2$

or $\bar{I}_1 N_1 = \bar{I}_2 N_2$ (6.10)

which yield the *current transformation ratio*

$$\frac{\bar{I}_1}{\bar{I}_2} = \frac{N_1}{N_2} = \frac{1}{a} \quad (6.11)$$

We find that an ideal transformer *transforms the current in the inverse ratio of turns* and the phase is preserved. In terms of rms values,

$$\frac{I_1}{I_2} = \frac{N_2}{N_1} = \frac{1}{a} \quad (6.12)$$

The complete phasor diagram of the ideal transformer is drawn in Fig. 6.7 showing currents as well.

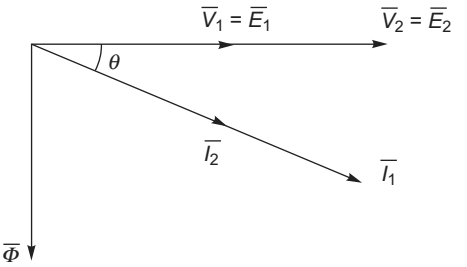


Fig. 6.7 *Phasor diagram of ideal transformer*

❑ **Important Note** The transformation ratio holds for emfs induced by the mutual flux. This equals the voltage ratio for the ideal transformer because there is no voltage drop. The current transformation applies to the secondary current and its primary current equivalent. These concepts will get clarified in Sections 6.3 and 6.4.

Equivalent Circuit

The equivalent circuit of an ideal transformer is drawn in Fig. 6.8.

Here, $\bar{V}'_2 = a\bar{V}_2$ (6.13)

and $\bar{I}'_2 = \frac{1}{a}\bar{I}_2$ (6.14)

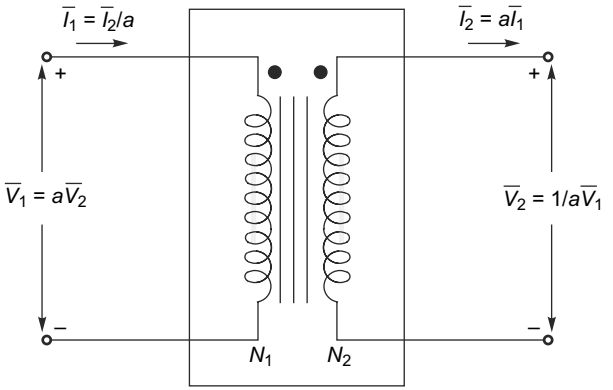


Fig. 6.8 *Equivalent circuit of IT ($a = N_1/N_2$)*

They are called 'the secondary voltage and current referred to the primary'. Similarly, we define

$$\bar{V}'_1 = \frac{1}{a}\bar{V}_2 \quad (6.15)$$

$$\bar{I}'_1 = a\bar{I}_1 \tag{6.16}$$

as 'the primary voltage and current referred to the secondary'.

The three vertical lines are indicative of the core. It is not necessary to draw these in every diagram.

It may be remarked here that V_2 applied to the secondary winding of an ideal transformer produces the same maximum core flux as V_1 applied to the primary winding (Eq. (6.8)).

6.2.3 Impedance Transformation

In Fig. 6.9, an impedance $\bar{Z}_2$ is connected on the secondary side of the ideal transformer. The impedance as seen in the primary side is found as

$$\frac{\bar{V}_2}{\bar{I}_2} = \bar{Z}_2 \tag{6.17a}$$

or

$$\frac{(N_2/N_1)\bar{V}_1}{(N_2/N_1)\bar{I}_1} = \bar{Z}_2$$

$$\frac{\bar{V}_1}{\bar{I}_1} = \left(\frac{N_1}{N_2}\right)^2 \bar{Z}_2 \tag{6.17b}$$

$$= a^2\bar{Z}_2 = \bar{Z}'_2 \tag{6.18}$$

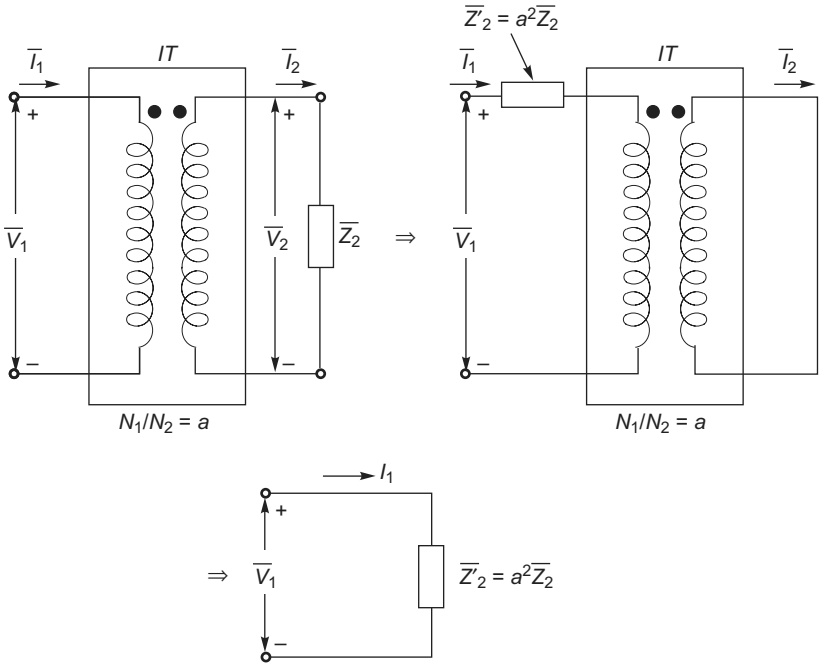


Fig. 6.9 *Impedance-transforming property of IT*

The impedance transformation property [Eq. (6.18)] is illustrated diagrammatically in Fig. 6.9. $\bar{Z}'_2$ is called 'the secondary impedance referred to the primary', vice versa applies equally, i.e. $\bar{Z}'_1 = (1/a^2)\bar{Z}_1$. The *impedance transforms from one side of the ideal transformer to the other in the direct square ratio of turns*.

Equation (6.18) can be put in the admittance form as

$$\bar{Y}'_2 = \frac{1}{a^2}\bar{Y}_2 \tag{6.19}$$

i.e. the admittance transforms from one side of the ideal transformer to the other in the inverse square ratio of turns.

The impedance-transforming property of the transformer is employed in impedance matching in electric circuits.

Example 6.1

An ideal transformer has a turn ratio of 100/300. The LV winding is connected to a source of 3.3 kV, 50 Hz. An impedance of (100 + *j* 35) Ω is connected across the secondary terminals. Calculate (a) the value of maximum core flux, (b) the primary and secondary currents, (c) the real and reactive powers supplied by the source to the transformer primary, and (d) the value of impedance which connected directly across the source would draw the same real and reactive power as in (c).

Solution

(a) From Eq. (6.7),

$$\phi_{\max} = \frac{V_1}{\sqrt{2}\pi f N_1} = \frac{3.3 \times 1000}{\sqrt{2}\pi \times 50 \times 100}$$

$$= 0.149 \text{ Wb}$$

(b) $V_2 = 3.3 \times (300/100) = 9.9$ kV

$$\bar{I}_2 = \frac{9.9 \times 1000}{(100 + j35)} = 93.44 \angle -19.3° \text{ A}$$

$$\bar{I}_1 = (300/100) \times 93.44 \angle -19.3°$$

$$= 280.03 \angle -19.3° \text{ A}$$

(c) $$\bar{S} = \bar{V}_1 \bar{I}_1^* = \bar{V}_2 \bar{I}_2^*$$

$$= 9.9 \times 93.44 \angle 19.3° \text{kVA}$$

$$= (873.1 + \text{j}305.7)$$

Hence, $P_1 = 873.1$ kW, $Q_1 = 305.7$ kVA

(d) $$\bar{Z}_1 = \bar{Z}'_2 = a^2 \bar{Z}_2$$

$$= (100/300)^2 (100 + j\,35)$$

$$= 11.11 + j\,3.89\ \Omega$$

6.3 ACCOUNTING FOR FINITE PERMEABILITY AND CORE LOSS

In a real transformer, the core has finite permeability and to establish flux in the core, the primary winding would draw a current component called magnetising current from the source over and above the load current.

A real core will also have power loss (core loss) because it carries alternating flux. It can be modelled as a resistance R_i (or conductance G_i) across the primary voltage source.

The net exciting current[1] drawn by the primary to create core flux is then

$$\bar{I}_0 = \bar{I}_m + \bar{I}_i \tag{6.20}$$

where $\bar{I}_m = -j B_m \bar{V}_1$ = magnetising current

$\bar{I}_i = G_i \bar{V}_1$ = core (iron) loss current, in phase with $\bar{V}_1$

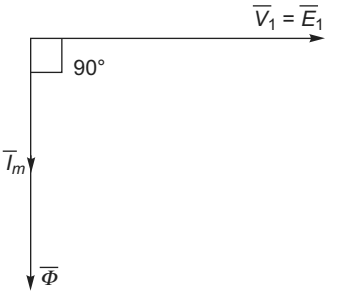


Fig. 6.10 *Magnetising current phasor diagram*

The phasor diagram of the exciting current is drawn in Fig. 6.11. Therefore, the angle θ_0 in the phasor diagram is close to 90°. It also means that the *exciting current I_0 has a low lagging power factor*.

The circuit model of the transformer at this stage of development is drawn in Fig. 6.12. The only assumption that is still made is that the windings are resistance-less and their leakage flux is negligible.

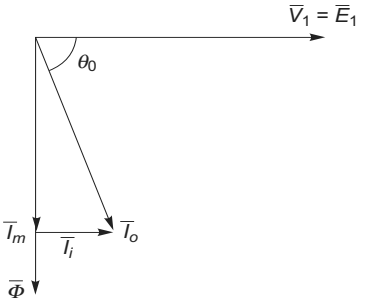


Fig. 6.11 *Exciting current phasor diagram*

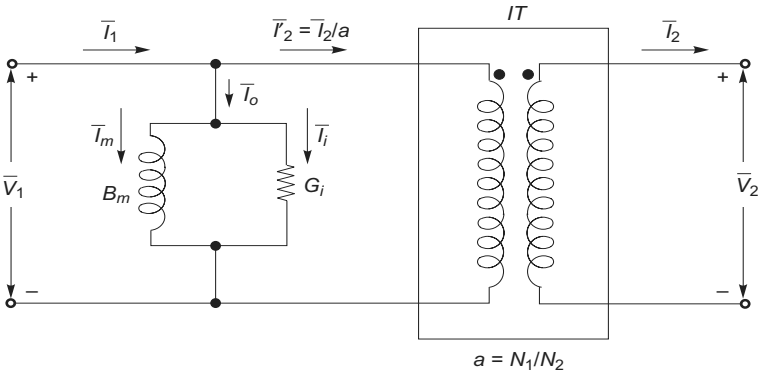


Fig. 6.12 *Circuit model of transformer (resistance and leakage neglected)*

[1] Loosely the term magnetising current will be used to mean exciting current.

It is seen from Fig. 6.12 that the resultant current (under load) drawn from the primary is

$$\bar{I}_1 = \bar{I}_0 + \bar{I}'_2 \tag{6.21}$$

The magnetising current in a transformer is in the range 2–5% of the rated current. Further, it being mainly reactive (θ_0 close to 90°), rms magnitude-wise is

$$I_1 \approx I'_2 = I_2/a \tag{6.22}$$

It is also clear from Fig. 6.12 that on no-load ($I'_2 = I_2/a = 0$), the transformer primary would draw only the exciting current from the source, which therefore is synonymous with the term *no-load current* (hence, the symbol I_0).

6.4 CIRCUIT MODEL OF TRANSFORMER

Both primary and secondary of a transformer have winding resistances. Apart from this, the two windings have leakage flux; ϕ_{l1} linking only the primary and ϕ_{l2} linking only the secondary (see Fig. 6.1), which induces the primary and secondary windings to possess leakage inductances and therefore, leakage reactances at steady sinusoidal operation. The ideal primary and secondary windings along with the core (which now carries only the mutual flux ϕ_m) indeed constitute the ideal transformer. Let windings resistances be r_1, r_2 and winding reactances (inductive) be x_1 and x_2.

The complete circuit model (commonly called *equivalent circuit*) is drawn in Fig. 6.13. It comprises the following circuit elements.

1. Magnetising shunt branch—B_m and G_i in parallel
2. Primary resistance r_1 and leakage reactance x_1 in series
3. Ideal transformer (turn ratio $N_1/N_2 = a$)
4. Secondary resistance r_2 and leakage reactance x_2 in series

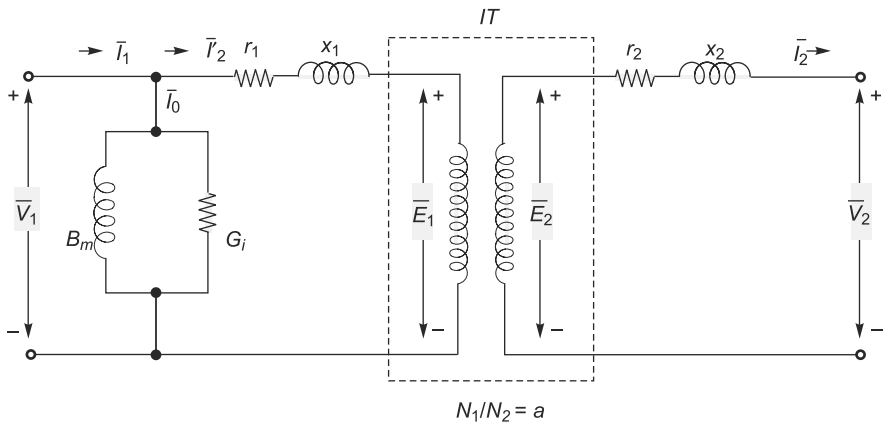


Fig. 6.13 *Equivalent circuit*

By the technique of impedance transformation, these can be transferred to one side of the transformer say the primary. Then equivalent series resistance and reactance of the transformer referred to the primary side are

Equivalent resistance $$R = r_1 + r'_2 = r_1 + a^2 r_2 \tag{6.23}$$

Equivalent resistance $$X = x_1 + x'_2 = x_1 + a^2 x_2 \tag{6.24}$$

The transformer circuit model (equivalent circuit) of Fig. 6.13 with secondary resistance and reactance, referred to the primary side, gets modified to the form shown in the figure where

$$\bar{I}'_2 = \bar{I}_2/a \tag{6.25}$$

$$\bar{V}'_2 = a\bar{V}_2 \tag{6.26}$$

In the circuit model of a transformer, it is not necessary to carry the ideal transformer as these voltage and current conversions Eqs (6.25) and (6.26) can always be carried out computationally.

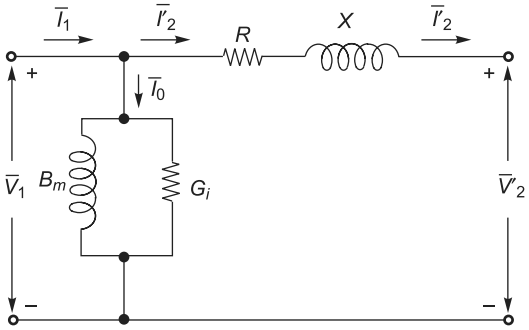


Fig. 6.14 *Circuit model of a transformer (IT left out)*

The magnetising shunt branches in the circuit model of Fig. 6.15 do not affect voltage computation and may therefore be ignored. Further, since R is much smaller in a transformer than X, R may also be ignored. These two steps lead to the simplified circuit models of Fig. 6.15. It is also unnecessary to carry the superscript 'dash' on current and voltage.

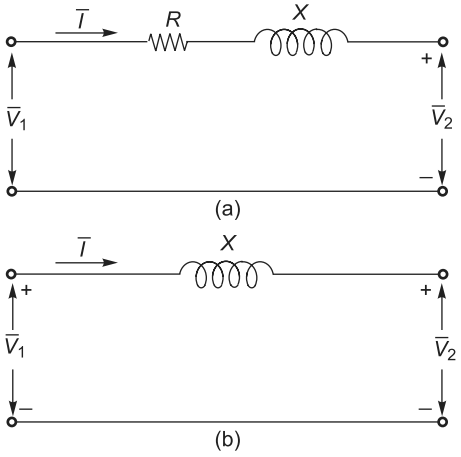


Fig. 6.15 *Simplified circuit model of a transformer*

Phasor Diagram

The phasor diagram corresponding to the circuit model of a transformer is drawn in Fig. 6.16 where θ_2 is secondary phase angle θ_1 = primary phase angle.

θ_1 is slightly more than θ_2
δ = angle by which V_1 load V_2, very small
ϕ lags E_1 by 90°, not shown is phasor diagram.

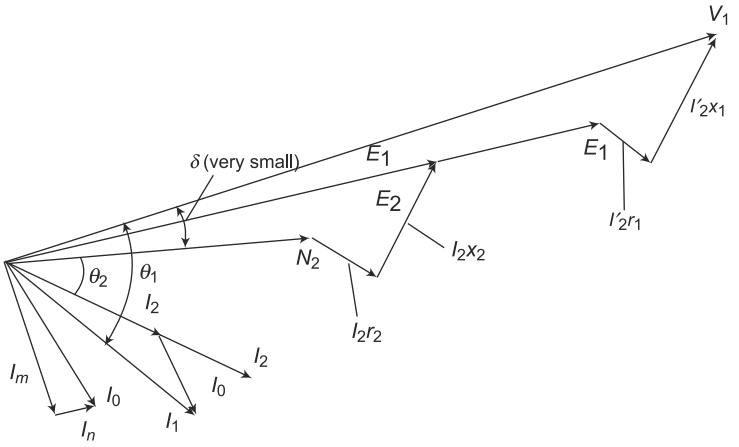


Fig. 6.16 *Transformer phasor diagram as per circuit model (not to scale)*

Alternative

If we use $e = -V\dfrac{d\theta}{dt}$, the flux phasor ϕ will lead E_1, E_2 by 90°. I_1 will be in phase opposition to I_2.

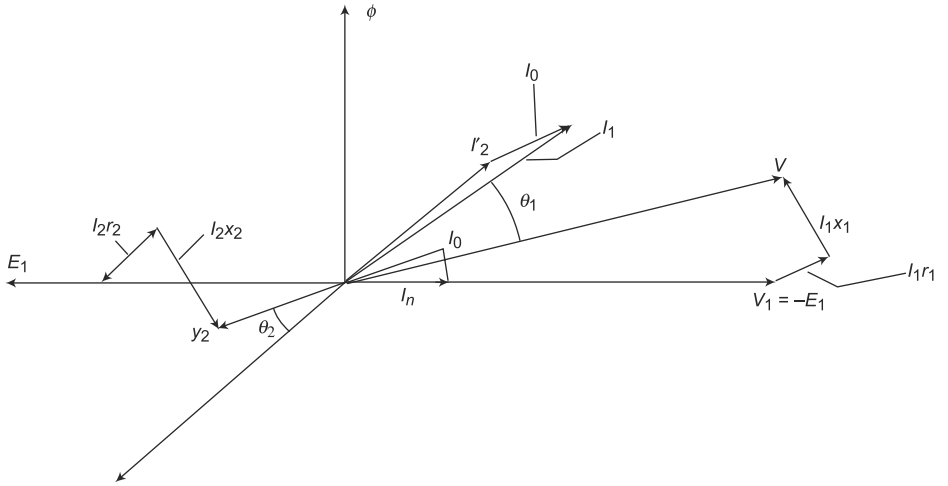


Fig. 6.17 *Transformer exact phasor diagram (not to scale)*

Summary

- It is seen from the complete circuit model of a transformer that because of voltage drops in the primary and secondary resistances and leakage reactances, we have

$$\frac{\bar{V}_1}{\bar{V}_2} \approx \frac{\bar{E}_1}{\bar{E}_2} = \frac{N_1}{N_2} = a$$

as the turn ratio is the ratio of induced emfs. However, as the series voltage drops are very small, it is sufficiently accurate to assume that

$$\frac{\bar{V}_1}{\bar{V}_2} \approx \frac{\bar{N}_1}{\bar{N}_2} = a$$

like in an ideal transformer.

- We observe from the circuit model that it has a shunt branch (B_m and G_i) across the source voltage $\bar{V}_1$ and a series branch (R and X) between $\bar{V}_1$ and $\bar{V}_2$. Therefore, we can treat these independently; shunt branch for finding exciting current $\bar{I}_0$ and the series branch for calculating voltage drop $(\bar{V}_1 - \bar{V}_2)$. The input current can then be found as the sum of the two currents—exciting current plus load current, i.e. $\bar{I}_1 = \bar{I}_0 + \bar{I}_2$.

Example 6.2

A 150 kVA, 2400/240 V single-phase transformer has the following parameters

$r_1 = 0.2\ \Omega$ $r_2 = 2 \times 10^{-3}\ \Omega$

$x_1 = 0.6\ \Omega$ $x_2 = 6 \times 10^{-3}\ \Omega$

and $R_i = 10\ \text{k}\Omega$ $X_m = 1.6\ \text{k}\Omega$

(a) Calculate the equivalent resistance and leakage reactance as seen on the HV side.

(b) Convert the resistance and reactance values referred to LV side.

(c) At rated current, calculate the impedance voltage drop on the HV side. Also, calculate the voltage drop as a percentage of the rated voltage.

(d) With the secondary open (no load), what current will be drawn from HV side (2400 V source). What is its pf?

Solution We will take the turn ratio same as the ratio of rated voltage. Thus,

Turn ratio, $a = \dfrac{2400}{240} = 10$

(a) As seen on HV side,

$$R = 0.2 + (10)^2 \times 2 \times 10^{-3}$$

$$= 0.2 + 0.2 = 0.4\ \Omega$$

$$X = 0.6 + (10)^2 \times 6 \times 10^{-3} = 1.2\ \Omega'$$

(b) As referred to the LV side,

$$R(LV) = \frac{1}{(10)^2} \times 0.4 = 4 \times 10^{-3}\ \Omega$$

$$X(LV) = \frac{1}{(10)^2} \times 1.2 = 12 \times 10^{-3}\ \Omega'$$

(c) With reference to Fig. 6.8,

$$I'_2 = \frac{150 \times 1000}{2400} = 62.5\,A$$

Series impedance

$$\bar{Z} = R + jX = 0.4 + j1.2$$

or $Z = 1.265\ \Omega$

Voltage drop = $I'_2 Z = 62.5 \times 1.265 = 79$ V

Percentage voltage drop = $\frac{79}{2400} \times 100 = 3.29\%$

(d) With secondary open (no load), only the shunt magnetising branch will draw current from the 2400 V source.

$$\therefore \quad I_m = \frac{2400}{X_m} = \frac{2400}{1.6 \times 10^3}$$

$$= 1.5 \text{ A}$$

$$\therefore \quad I_i = \frac{2400}{R_i} = \frac{2400}{10 \times 10^3}$$

$$= 0.24 \text{ A}$$

$$\bar{I}_0 = 0.24 - j1.5\,\text{A} = 1.52 \angle -81^\circ\,\text{A}$$

pf = cos 81° = 0.156 lagging

Example 6.3

A 200 kVA, 1100/415 V, 50 Hz single-phase transformer has 80 turns of secondary. Calculate

(a) approximate value of primary turns,

(b) the full-load secondary current and approximate value of primary current,

(c) maximum core flux, and

(d) the secondary impedance which would fully load the transformer and its value as seen on the primary side.

Solution

Assumption: We take the transformer to be ideal and turn ratio to be the same as the voltage ratio.

(a) $\frac{N_1}{N_2} = \frac{11000}{415}$; $\quad N_1 = \frac{11000}{415} \times 80 = 2120.48$

As turns must be integral, we take $N_1 = 2120$

$$a = \frac{N_1}{N_2} = \frac{2120}{80}$$

(b) Full load = 200 kVA

Voltage applied to primary

$$V_1 = 11000 \text{ V}$$

Secondary voltage,

$$V_2 = 11000 \times \frac{80}{2120} = 415.9 \approx 415\,\text{V}$$

$$I_2 = \frac{200 \times 10^3}{415} = 481.9\ \text{A}$$

$$I_1 = 481.9 \times \frac{80}{2120} = 16.19\ \text{A}$$

The primary current value is approximate because we have taken the transformer to be ideal, which means that the exciting current drawn from the source has been neglected. As the exciting current is very small and has a phase angle close to 90°, this is a fair approximation.

(c) Full-load secondary kVA = 200; series impedance of transformer ignored

$$\frac{(415)^2}{Z_2} \times 10^{-3} = 200$$

Z_2 (for full loading) = 0.861 Ω
As seen on primary

$$Z'_2 = a^2 Z_2 = \left(\frac{2120}{80}\right)^2 \times 0.861 = 6046\,\Omega$$

Example 6.4

A transformer has 150 primary turns and 75 secondary turns. Its primary is excited at 200 V and the secondary is loaded with an impedance of $5 \angle 30^\circ\ \Omega$. Calculate the primary current and its pf. State assumptions made.

Solution *Assumption:* Transformer is ideal

Given $\bar{Z}_2 = 5 \angle 30^\circ \Omega$

$$\bar{I}_2 = \frac{200 \angle 0^\circ}{5 \angle 30^\circ} = 40 \angle -30^\circ\ \text{A}$$

Primary current, $I_1 = \left(\frac{N_2}{N_1}\right) I_2$

or $$I_1 = \frac{75}{100} \times 40 \angle -30^\circ = 20^\circ \angle -30^\circ \Omega$$

Power factor = cos 30° = 0.860 lagging

Example 6.5

An audio-frequency transformer is employed to couple a 60 Ω resistive load to a source of 6 V in series with a resistance of 2400 Ω.

(a) Determine the transformer turn ratio to ensure that maximum power is transferred to the load.

(b) Calculate the value of the maximum power and corresponding load current and voltage.

Solution As per maximum power theorem, the load resistance reflected to the source side must equal source resistance. Thus,

(a) $$\left(\frac{N_1}{N_2}\right)^2 \times 60 = 2400$$

or $$\frac{N_1}{N_2} = \sqrt{40} = 6.325$$

(b) Maximum load power, P_L (max)

$$= \frac{1}{2}\left[\frac{(60)^2}{2400 + 2400}\right] = 0.375 \text{ W}$$

Current drawn from source,

$$I_1 = \frac{6}{2400 + 2400} = 1.25 \times 10^{-3} \text{ A}$$

Load current, $$I_L = I_2 = \left(\frac{N_1}{N_2}\right) I_1 = 1.25 \times 10^{-3} \sqrt{40} = 0.79 \text{ mA}$$

Load voltage $$V_L = V_2 = \left(\frac{N_1}{N_2}\right) \times \frac{1}{2} \times 6 = \frac{3}{6.325} = 0.474 \text{ V}$$

6.5 PER-UNIT SYSTEM

It is often convenient to scale electrical quantities in per unit of the base or reference values of these quantities. The basic per-unit (pu) scaling equation is

$$\text{Per-unit value} = \frac{\text{Actual value}}{\text{Base value}} \tag{6.27}$$

The pu system offers the advantage that the device parameters tend to fall in a relatively narrow range, making the erroneous values conspicuous. Also in computations, one does not have to deal with very small and very large numbers. In a power system (with many transformers of different voltage ratio), ideal transformers are no longer necessary in the model.

Base values are related to each other by the usual electrical laws. For a single-phase system,

$$P_B, Q_B, (\text{VA})_B = V_B I_B \tag{6.28a}$$

$$R_B, X_B, Z_B = \frac{V_B}{I_B} \tag{6.28b}$$

$$G_B, B_B, Y_B = \frac{I_B}{V_B} \tag{6.28c}$$

$(\text{VA})_B$ and V_B are first to be selected. Then it follows from Eq. (6.28b) that

$$Z_B = \frac{V_B^2}{(\text{VA})_B} = \frac{1000(\text{kV})_B^2}{(\text{kVA})_B} \tag{6.29}$$

Then $$Z(\text{pu}) = \frac{Z(\Omega) \times (\text{VA})_B}{V_B^2} \tag{6.30}$$

In large devices and systems, it is more practical to use base values in kVA/MVA and kV. Equation (6.30) can then be written as

$$Z(\text{pu}) = \frac{Z(\Omega) \times (\text{kVA})_B}{1000(\text{kV})_B^2} \tag{6.31a}$$

or

$$Z(\text{pu}) = \frac{Z(\Omega) \times (\text{MVA})_B}{(\text{kV})_B^2} \tag{6.31b}$$

In changing Z(pu) from one set of base values to another,

$$Z(\text{pu})_{\text{new}} = Z(\text{pu})_{\text{old}} \times \frac{(\text{MVA})_{B,\text{new}}}{(\text{MVA})_{B,\text{old}}} \times \frac{(\text{kV})_{B,\text{old}}^2}{(\text{kV})_{B,\text{new}}^2} \tag{6.32}$$

In a three-phase star-connected system (equivalent star can always be found)

$(\text{MVA})_{P,B}$ = MVA base per phase

$(\text{MVA})_{3P,B}$ = MVA base 3-phase

$(\text{kV})_{P,B}$ = kV base line-to-neutral

$(\text{kV})_{L,B}$ = kV base line-to-line

Then

$$(\text{kV})_{L,B} = \sqrt{3}\,(\text{kV})_{P,B} \tag{6.33}$$

$$(\text{MVA})_{3P,B} = 3(\text{MVA})_{P,B} \tag{6.34}$$

It can be easily shown that

$$V_P(\text{pu}) = V_L(\text{pu}); \text{ no factor of } \sqrt{3} \tag{6.35}$$

$$(\text{MVA})_P\,(\text{pu}) = (\text{MVA})_{3P}(\text{pu}); \text{ no factor of 3} \tag{6.36}$$

$$I_{P,B} = I_{L,B} = \frac{(\text{MVA})_{3P,B}}{\sqrt{3}\,(\text{KV})_{LB}} \tag{6.37}$$

Now

$$Z_B = \frac{((\text{kV})_{L,B}/\sqrt{3}))^2}{(1/3)(\text{MVA})_{3P,B}} = \frac{(kV)_B^2, B}{(\text{MVA})_{3P,B}} \tag{6.38}$$

$$Z_{(\text{pu})} = \frac{Z(\Omega) \times (\text{MVA})_{3P,B}}{(\text{kV})_{L,B}^2} \tag{6.39}$$

By definition,

$$Z_{\Delta,B} = 3\,Z_{Y,B} \tag{6.40}$$

It then follows that

$$Z_Y(\text{pu}) = Z_\Delta(\text{pu}) \tag{6.41}$$

Since it is a common practice to use three-phase MVA, and line-to-line kV bases, suffixing can be simplified as

$$(\text{MVA})_{3P,B} \rightarrow (\text{MVA})_B$$

$$(\text{kV})_{L,B} \rightarrow (\text{kV})_B \tag{6.42}$$

Advantages of PU System

1. *Choice of Bases:* Voltage bases on the two sides of a transformer should be in direct ratio of transformation (and current bases in the inverse ratio). Its advantage is that the pu values of transformer parameters on either side are the same. The reason is not hard to find as shown below.

$$Z(\text{pu}) = \frac{I(\text{HV})Z(\text{HV})}{V(\text{HV})}$$

$$= \frac{I(\text{LV})}{V(\text{LV})} \times \left[\frac{N(\text{LV})}{N(\text{HV})}\right]^2 \times Z(\text{HV})$$

$$= \frac{I(\text{LV})Z(\text{IV})}{V(\text{LV})} \tag{6.43}$$

This eliminates the need of ideal transformers for the circuit models of transformers with different transformation ratios in a power system.

It is convenient to choose the primary voltage as base on the primary side and the secondary voltage as the base on secondary side. The rating of the transformer is taken as its VA/kVA/MVA base.

2. The transformer, or in general, the device parameters in pu, lie in a narrow range, in some characteristic of the device. There is no need to deal with very small and very large numbers.

Example 6.6

A 50 kVA, 1100/220 V has primary and secondary resistance and leakage reactance as below:

	Resistance	Leakage reactance
Primary (HV)	0.125 Ω	0.625 Ω
Secondary (LV)	0.005 Ω	0.025 Ω

(a) Calculate the impedance of the transformer referred to HV and LV.

(b) Find the pu impedance of the transformer both from HV side and LV. Are both these values equal?

Solution

(a) Referred to HV side:

$$\bar{Z}_1 = (0.125 + j0.625) + \left(\frac{1100}{220}\right)^2 (0.005 + j0.25)$$

$$= 0.25 + j1.25\ \Omega$$

Referred to LV side:

$$\bar{Z}_1 = (0.005 + j0.025) + \left(\frac{220}{1100}\right)^2 (0.125 + j0.625)$$

$$= (0.01 + j0.05)\ \Omega$$

(b) $(\text{kVA})_B = 50$ or $(\text{MVA})_B = 0.05$

$\text{HV side } (\text{kV})_B = 1.1$

$\text{LV side } (\text{kV})_B = 0.22$

As found from HV side:

$$\bar{Z}(\text{pu}) = (0.25 + j1.25) \times \frac{0.05}{(1.1)^2}$$

$$= 0.01 + j0.052$$

As found from LV side:

$$\bar{Z}(\text{pu}) = (0.25 + j1.25) \times \frac{0.05}{(1.1)^2}$$

$$= 0.01 + j\,0.052$$

As found from LV side:

$$\bar{Z}(\text{pu}) = (0.01 + j0.05) \times \frac{0.05}{(0.22)^2}$$

$$= 0.01 + j0.052$$

Example 6.7

A single-phase, 600 kVA, 2400/600 V transformer has the following circuit-model parameters:

$r_1 = 0.05\ \Omega$, $r_2 = 0.004\ \Omega$

$x_1 = 0.025\ \Omega$, $x_2 = 0.016\ \Omega$

$R_i = 1667\ \Omega$, $X_m = 417\ \Omega$. (as seen on HV side)

(a) Draw its equivalent circuit as seen from LV side.

(b) Convert the circuit of part (a) to pu form.

Solution

(a) As seen on LV side:

$$R + jX = (0.004 + j\,0.016) + \left(\frac{600}{2400}\right)^2 (0.05 + j\,0.025)$$

$$= 0.007125 + j\,0.01756\ \Omega$$

Shunt branch as seen on LV side:

$$R_i(\text{LV}) = 1667 \times \left(\frac{600}{2400}\right)^2 = 104.2\ \Omega$$

$$X_m(\text{LV}) = 417 \times \left(\frac{600}{2400}\right)^2 = 26.1\ \Omega$$

The circuit is drawn in Fig. 6.18.

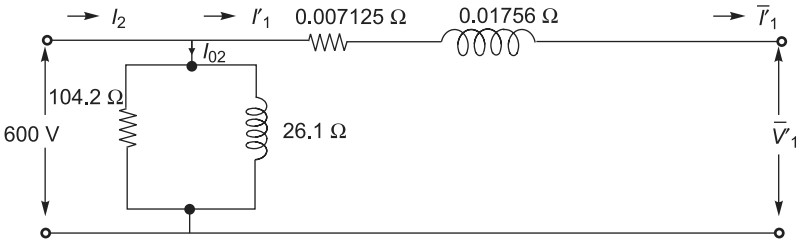


Fig. 6.18

It may be noted that because of voltage drops in $(R + j\,X)$,

$$V'_1\left(\frac{2400}{600}\right) \neq V_1 = 2400$$

Further turn ratio, $\frac{N_1}{N_2} \approx \frac{2400}{600}$

Pu parameter values:

$(\text{MVA})_B = 0.6, (\text{kV})_B = 0.6$

$$(R + jX) = (0.007125 + j0.01756) \times \frac{0.6}{(0.6)^2}$$

$$= 0.012 + j\,0.0293 \text{ pu}$$

$$R_i = 104.2 \times \frac{0.6}{(0.6)^2} = 173.7 \text{ pu}; \; X_m = 26.1 \times \frac{0.6}{(0.6)^2} = 43.5$$

(b) Circuit in pu is drawn in Fig. 6.19.

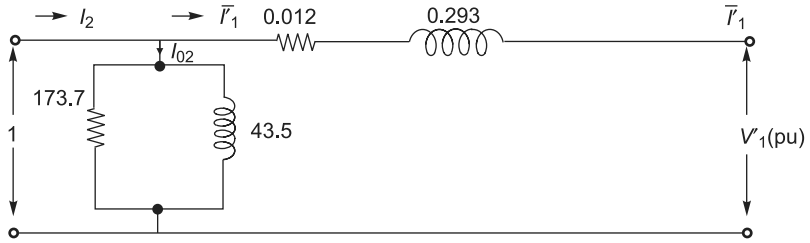


Fig. 6.19

6.6 DETERMINATION OF PARAMETERS OF CIRCUIT MODEL OF TRANSFORMER

It is not practical to test a transformer for its voltage-drop characteristic and its efficiency by a direct loading test. Such a test would suffer from three disadvantages, viz.

(i) loss of energy during testing,
(ii) it may not be practical to arrange for load except for small size transformers, and
(iii) losses as administered by direct loading would be in serious error as these are found by the difference of the input and output power readings which are close to each other, the losses being very small. It is well known that errors in meter readings add up and become a much larger percent of the difference.

It is therefore standard practice in transformer testing to determine the transformer losses and the parameters of the circuit model by means of *nonloading* tests. The transformer performance is then computed from the circuit model.

Transformer parameter determination necessitates two tests, viz. open-circuit test and short-circuit test.

6.6.1 Open-Circuit (OC) Test or No-Load Test

The transformer is excited at rated voltage (and frequency) from one side while the other side is kept open-circuited as shown in Fig. 6.20(a). It is usually convenient to conduct such a test from the LV side. The circuit model under open-circuit is drawn in Fig. 6.20(b); it follows from Fig. 6.14 by setting $I'_2 = 0$.

Let the meter readings be

voltage (V) = V_1

current (A) = I_0 (6.44)

and power (W) = P_0 = core loss (P_i)

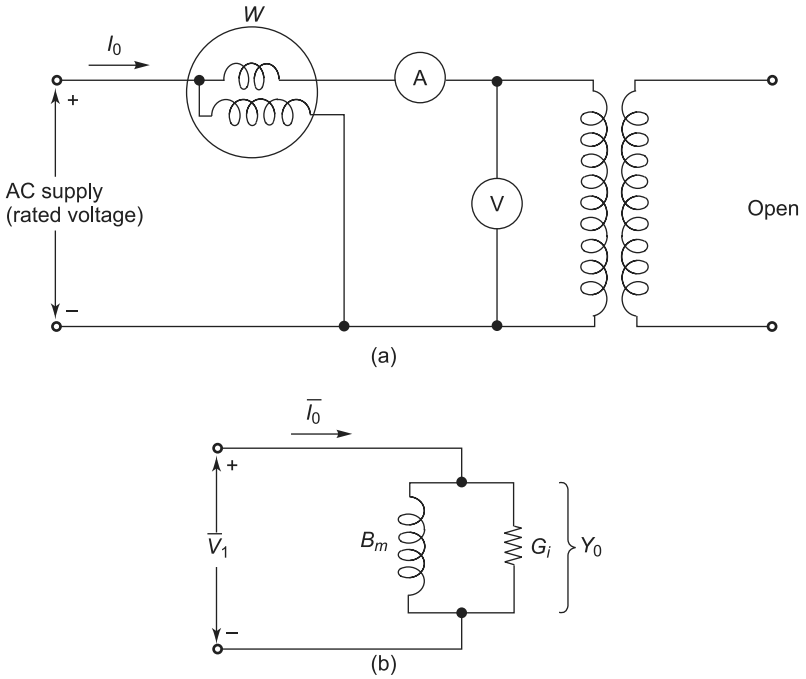


Fig. 6.20 *(a) Circuit diagram for OC test (b) Circuit model as seen on open-circuit*

It then follows that

$$Y_0 = \frac{I_0}{V_1} \tag{6.45}$$

$$G_i = \frac{P_0}{V_1^2} \tag{6.46}$$

and $$B_m = \sqrt{Y_0^2 - G_i^2} \tag{6.47}$$

By connecting a voltmeter on the secondary side, the OC test also yields the voltage ratio of the transformer, which is practically its turn ratio a.

The values of G_i and B_m as computed can be transferred to the other side of the transformer, if so desired.

It is seen that the OC test yields (i) core loss, and (ii) parameters of the shunt branch of the transformer model.

The OC test is usually conducted from the LV side as low voltage small current supply is needed for the test.

Example 6.8

A 50 kVA, 2200/110 V transformer is connected to 110 V supply with metering. With the 2200 V side open-circuited, the meter readings are 110 V, 10 A, 400 W. Compute the parameters of the shunt branch of the equivalent circuit as seen from the LV and HV sides.

Solution OC test on LV side—shunt branch parameters:

$$Y_0 = \frac{10}{110} = 0.091 \ \text{℧}$$

$$G_i = \frac{400}{(110)^2} = 0.033 \ \text{℧}$$

$$B_m = (Y_0^2 - G_1^2)^{1/2} = 0.085 \ \text{℧}$$

As seen on HV side:

$$G_i \text{ (HV)} = 0.033 \times \left(\frac{110}{2200}\right)^2 = 8.25 \times 10^{-3} \ \text{℧}$$

$$B_m \text{ (HV)} = 0.085 \times \left(\frac{110}{2200}\right)^2 = 21.25 \times 10^{-3} \ \text{℧}$$

6.6.2 Short-Circuit (SC) Test

This test determines the series parameters of the transformer-circuit model. The transformer is shorted on one side and is excited from a reduced voltage (rated frequency) source from the other side as shown in Fig. 6.21. The transformer circuit model under short-circuit conditions is drawn in Fig. 6.22(a). As the primary current is limited only by the resistance and leakage reactance of the transformer, V_{sc} needed to circulate full-load current is only of the order of 5–8% of the rated voltage. At this reduced voltage, the exciting I_0 which is 2 to 5% of the rated current gets reduced to 5% of 2%, which is 0.1% to 8% of 5% = 0.4% of the rated current.

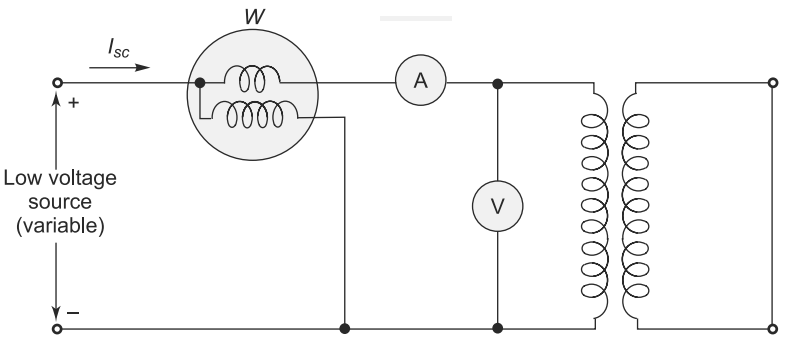


Fig. 6.21 *Short-circuit (SC) test on transformer*

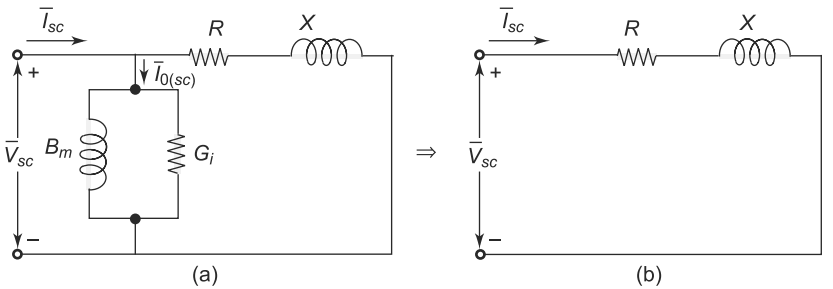


Fig. 6.22 *Circuit model under SC conditions*

The magnetising shunt branch of the circuit model can therefore be conveniently dropped resulting in the circuit of Fig. 6.22(b).

For convenience of the supply voltage and current needed, the SC test is usually conducted from the HV side and the LV side is short circuited.

In conducting the SC test, as in Fig. 6.21, the source voltage is gradually raised till the transformer draws *full-load* current. The meter readings under these conditions are

voltage (V) = V_{SC}
current (A) = I_{SC} (6.48a)
power input (W) = $P_{SC} = I^2R$ loss or *copper loss* Pc
(total in the two windings)

From the circuit model of Fig. 6.22(b),

$$Z = \frac{V_{SC}}{I_{SC}} = \sqrt{R^2 + X^2} \tag{6.48b}$$

Equivalent resistance $$R = \frac{P_{SC}}{(I_{SC})^2} \tag{6.49}$$

Equivalent reactance $$X = \sqrt{Z^2 - R^2} \tag{6.50}$$

It is thus seen that the SC test yields information about (i) full-load copper loss, and (ii) equivalent resistance and reactance of the transformer.

Together OC and SC tests determine all the four parameters of the transformer circuit model of Fig. 6.14—two shunt parameters (G_i, B_m) and two series parameters (R, X).

Example 6.9

A 25 kVA, 2200/220 V; 50 Hz single-phase transformer is found to have the following paramaters:

$r_1 = 2\ \Omega$ $r_2 = 0.025\ \Omega$
$x_1 = 7\ \Omega$ $x_2 = 0.07\ \Omega$
$X_m = 16000\ \Omega$ (HV)

Find the following:

(a) No-load current, its pf and power when excited from the LV side.
(b) With the LV side shorted, the HV side voltage needed to circulate full-load current. What is exciting current compared to full-load current?
(c) What is the power factor under part (b)?

Solution

(a) Turn ratio, $a = \frac{2200}{220} = 10$

No-load, LV excited at 220 V:

$$X_m\,(\text{LV}) = \frac{16000}{(10)^2} = 160 = 13.75\ \text{mA}, 90^\circ \text{ lagging}$$

Only magnetising current will be drawn. The core loss current is zero (negligible).

$$I_m = \frac{220}{160} \times 10^3 = 13.75\ \text{mA}, 90^\circ \text{ lagging}$$

pf = 0, $P_0 = 0$

Note: There be a small amount of core loss power drawn, which is being ignored here.

(b) Referred to HV side:

$$R = 2 + 0.025\ (10)^2 = 4.5\ \Omega$$

$$X = 7 + 0.07\ (10)^2 = 14\ \Omega$$

$$Z = \sqrt{R^2 + X^2} = \sqrt{(4.5)^2 + (14)^2} = 14.7\Omega$$

Full-load current, $I(fl) = \dfrac{25 \times 10^3}{2200} = 11.36\,\text{A}$

$$V_{SC} = ZI_{SC} = 14.7 \times 11.36 = 167\ \text{V}$$

It is $\dfrac{167}{2200} \times 100 = 7.59\%$ of rated voltage.

At this voltage, magnetising current = $\dfrac{167}{16000} \times 10^2 = 1.044\ \text{mA}$

It is $\dfrac{10.44 \times 10^{-3}}{11.36} \times 100 = 0.09\%$.

So magnetising current can be neglected in the SC test

(c) SC pf = $\left[\cos \tan^{-1}\left(\dfrac{X}{R}\right) = \cos\left(\tan^{-1}\dfrac{14}{4.5}\right)\right]$

Example 6.10

A 50 kVA, 2200/220 V transformer when tested gave the following results:

OC test, measurements on LV side: 405 W, 5 A, 220 V

SC test, measurements on HV side: 805 W, 20.2 A, 95 V

(a) Draw the circuit model of the transformer referred to the HV and LV sides. Label all the parameters.

(b) Calculate the pu parameters of the transformer.

Solution OC test (LV side):

$$Y_0 = \frac{5}{220} = 0.0227\ \text{℧}$$

$$G_i = \frac{405}{(220)^2} = 0.0084\ \text{℧}$$

$$B_m = [(0.0227)^2 - (0.0084)^2]^{1/2} = 0.021\text{℧}$$

SC test (HV side):

$$Z = \frac{95}{20.2} = 4.7\Omega$$

$$R = \frac{805}{(20.2)^2} = 1.97\Omega$$

$$X = [(4.7)^2 - (1.97)^2]^{1/2} = 4.27\ \Omega$$

(a) Circuit model referred to HV side:

$$a = \frac{2200}{220} = 10$$

$$G_i = 0.0084 \times \frac{1}{(10)^2} = 0.084 \times 10^{-3}\ \text{℧}$$

$$B_m = 0.021 \times \frac{1}{(10)^2} = 0.021 \times 10^{-3}\ \text{℧}$$

$$R = 1.97\ \Omega$$

$$X = 4.27\ \Omega$$

The circuit model is drawn in Fig. 6.23(a).

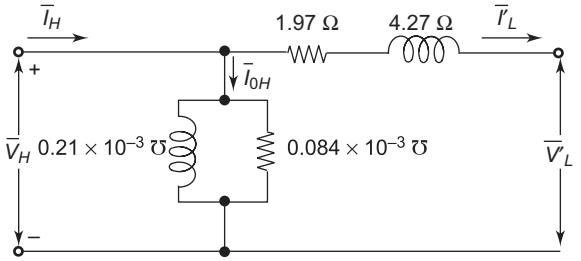


Fig. 6.23(a)

Circuit model referred to LV side:

$$G_i = 6.4 \times 10^{-3}$$

$$B_m = 21 \times 10^{-3}$$

$$R = 1.97 \times \frac{1}{(10)^2} = 0.02\,\Omega$$

$$X = 4.97 \times \frac{1}{(10)^2} = 0.043\,\Omega$$

The circuit model is drawn in Fig. 6.23(b).

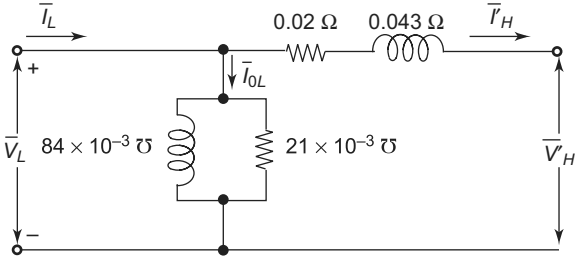


Fig. 6.23(b)

(b) The pu value of parameters are the same as calculated from any side. Let us use HV side as base.

$$(\text{kVA})_B = 50$$

$$(\text{kV})_B = 2.2 \text{ kV}$$

Then

$$Z_B = \frac{1000 \times (2.2)^2}{50} = 96.8\ \Omega$$

$$Y_B = \frac{1}{96.8} = 0.0103\ \text{℧}$$

The pu circuit model are found from Fig. 6.23(b). The circuit can now be drawn by the reader.

6.7 VOLTAGE REGULATION

Domestic, commercial and industrial loads demand a nearly constant voltage supply. It is therefore essential that the output voltage of a transformer stays within narrow limits as load and its power factor vary. The leakage reactance is the chief cause of voltage drop in a transformer and must be kept as low as possible by design and manufacturing techniques.

The voltage regulation of a transformer at a *given power factor* is defined as

$$\%\ \text{voltage regulation} = \frac{V_{2,0} - V_{2,f1}}{V_{2,f1}} \times 100 \tag{6.51}$$

where $V_{2,fl}$ is the full-load secondary voltage (it is assumed to be adjusted to the rated secondary voltage) and V_{2o} is the secondary voltage when the load is thrown off.

Examination of the circuit model of the transformer reveals that for voltage computation, the shunt branch can be left out, resulting in simple series circuit drawn in Fig. 6.24(a). The phasor diagram showing circuit current and voltage is drawn in Fig. 6.24(b) for *lagging power factor*. Some explanation is in order:

- Resistive voltage drop $\bar{I}R$ is parallel to load current $\bar{I}$
- Reactive voltage drop $j\bar{I}X$ lead $\bar{I}$ by 90°
- Input voltage $\bar{V}_1$ leads load voltage $\bar{V}_2$ by angle δ, which if necessary can be determined from the phasor diagram
- Additional geometrical construction shown dotted in the figure

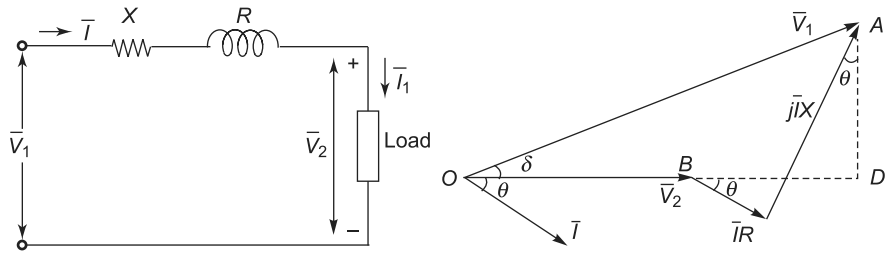


Fig. 6.24 *(a) Circuit model (b) Phasor diagram (not proportional)*

The corresponding phasor equation of the circuit is $\overline{V}_1 = \overline{V}_2 + \overline{I}\,R + j\overline{I}\,X$.

As in a transformer, *IR* and *IX* voltage drops are much smaller in magnitude compared to V_1 and V_2, the angle between $\overline{V}_1$, and $\overline{V}_2$ in Fig. 6.24(b) is only a few degrees such that

$$V_1 \approx OD$$

$$V_1 - V_2 \approx BD$$

$$= I(R\cos\theta + X\sin\theta);\ \theta \text{ lagging} \tag{6.52a}$$

$$= I(R\cos\theta - X\sin\theta);\ \theta \text{ leading} \tag{6.52b}$$

The reader is advised to draw the phasor diagram for leading pf.

When the load is thrown off,

$$V_{20} = V_1$$

$$\therefore \quad V_{20} - V_2 = V_1 - V_2$$

Then

% voltage regulation,

$$R_{\text{eg}} = \frac{V_{20} - V_2}{V_2} \times 100$$

$$= \frac{I(R\cos\theta + X\sin\theta)}{V_2} \times 100 \tag{6.53}$$

For maximum voltage regulation [from Eq. (6.53)],

$$\frac{d(R_{\text{eg}})}{\mathrm{d}\theta} = 0 = -R\sin\theta + X\cos\theta$$

or $$\tan\theta = \frac{X}{R}$$

or $$\text{pf} = \cos\theta = \frac{R}{(R^2 + X^2)^{1/2}};\ \text{lagging} \tag{6.54}$$

From Eq. (6.52), voltage regulation is zero when

$$R\cos\theta - X\sin\theta = 0;\ \theta \text{ leading}$$

or $$\tan\theta = \frac{R}{X}$$

or $$\text{pf} = \cos\theta = \frac{X}{(R^2 + X^2)^{1/2}};\ \text{leading} \tag{6.55}$$

Leading θ larger than that given in Eq. (6.55) would result in negative voltage regulation, i.e. secondary voltage on full load is higher than the no-load voltage.

6.8 NAMEPLATE RATING

The voltage ratio of a transformer is specified as V_1 (rated)/V_2 (rated), where V_1 (rated) and V_2 (rated) are the primary and secondary voltage at full load and specified pf. Since the voltage drop in a transformer is only a few percent, this ratio is also taken as the turn ratio N_1/N_2 for all practical purposes, i.e.

$$\frac{V_1(\text{rated})}{V_2(\text{rated})} \approx \frac{N_1}{N_2}$$

A transformer depending upon its size can carry only a certain current, called full-load current, without overheating. The transformer rating is then

$$\text{kVA (rating)} = \frac{V(\text{rated}) \times I(\text{full-load})}{1000}$$

It could also be expressed as VA (rated) for small transformers and in MVA (rated) for very large size transformers.

The pu impedance of a transformer on its rated voltage and kVA bases is given by

$$Z(\text{pu}) = \frac{I(\text{full-load})Z(\Omega)}{V(\text{rated})}$$

$$= \frac{\text{kVA(rated)}Z(\Omega)}{1000(\text{kV(rated)})^2}$$

where I (full load), V(rated) and $Z(\Omega)$ pertain to any side of the transformer.

The percentage impedance is defined as

$$\%Z = Z(\text{pu}) \times 100$$

$$= \frac{I(\text{full-load})Z(\Omega)}{V(\text{rated})} \times 100$$

Obviously, it has also the meaning of per cent voltage drop under full-load.

Example 6.11

The resistances and leakage reactances of a 10 kVA, 50 Hz, 2300/230 V distribution transformer are r_1 = 3.96 Ω and r_2 = 0.0396 Ω, x_1 = 15.8 Ω. and x_2 = 0.158 Ω subscript 1 refers to HV ami 2 in LV winding.

(a) The transformer delivers rated kVA at 0.8 pf lagging to a load on the LV side. Find the HV side voltage necessary to maintain 230 V across load terminals. Also, find the percentage voltage drop.

(b) lf a capacitor bank is connected across the load, what should be the kVA capacity of the bank to reduce the voltage regulation to zero. What should be the HV side voltage under these circumstances?

Solution

(a) Referred to HV side:

Equivalent resistance

$$R = 3.96 + 0.0396 \times (10)^2 = 7.92\ \Omega$$

Equivalent reactance

$$X = 15.8 + 0.158 \times (10)^2 = 31.6\ \Omega$$

With reference to Fig. 6.23(a),

$$V_2 = 230 \times 10 = 2300\ \text{V (referred to HV)}$$

At rated kVA load,

$$I = \frac{10 \times 1000}{2300} = 4.35 \text{ A}, \cos\theta = 0.8 \text{ lagging}$$

$$V_1 - V_2 = I(R\cos\theta + X\sin\theta)$$

$$= 4.35\,(7.92 \times 0.8 + 31.6 \times 0.6) = 110 \text{ V}$$

$$V_1 = 2300 + 110 = 2410 \text{ V}$$

$$V_{20} = V_1 = 2410 \text{ V}$$

$$\text{Voltage regulation} = \frac{2410 - 2300}{2300} \times 100\% = 4.78\ \%$$

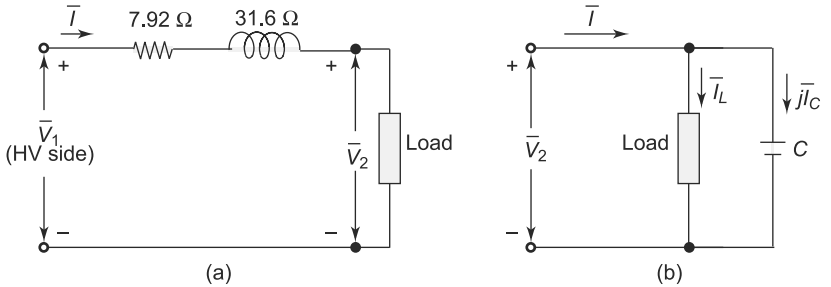


Fig. 6.25

(b) For zero voltage regulation:

$$\text{pf} = \cos\theta = \frac{X}{(R^2 + X^2)^{1/2}}$$

$$= \frac{31.6}{[(7.92)^2 + (31.6)6]^{1/2}} = 0.97 \text{ leading}$$

$$\theta = 14.1° \text{ leading}$$

A capacitor C is placed in parallel with the load to improve the power factor to 0.97 leading [Fig. 6.25(b)]

$$\bar{V}_2 = 2300 \angle 0° \text{ V}$$

Load current $$\bar{I}_L = 4.35\,(0.8 - j0.6) = 3.48 - j2.61$$

$$\bar{I} = \bar{I}_L + jI_C = 3.48 - j2.61 + jI_C$$

For $$\theta = 14.10°$$

$$\tan 14.1° = \frac{I_C - 2.61}{3.48}$$

or $$I_C = 3.48 \text{ A}$$

Rating of capacitor bank $$= \frac{2300 \times 3.48}{1000} = 8 \text{ kVA}$$

Since voltage regulation is zero

$$V_1 = 2300 \text{ V}$$

Example 6.12

A 100 kVA transformer has primary and secondary turns of 400 and 100 respectively. Its primary and secondary resistance and reactances are

$r_1 = 0.3\ \Omega$ $r_2 = 0.015\ \Omega$

$x_1 = 1.1\ \Omega$ $x_2 = 0.055\ \Omega$

The supply voltage is 2400 V.

Calculate

(a) Equivalent resistance and reactance on the primary side

(b) Voltage regulation and secondary voltage at a power factor of (i) 0.8 lagging, and (ii) 0.8 leading

(c) The power factor for zero voltage regulation.

Solution Turn ratio, $a = \dfrac{400}{100} = 4$

(a) Referred to primary:

$$R = 0.3 + (4)^2 \times 0.015 = 0.54\ \Omega$$

$$X = 1.1 + (4)^2 \times 0.055 = 1.98\ \Omega$$

(b) For calculating full-load current, we do not know the secondary voltage. We approximate it as the turn ratio equivalent of the primary voltage; a departure from the strict definition of voltage regulation. So on primary side

$$I_1 = \frac{100 \times 1000}{2400} = 41.67\ \text{A}$$

(i) 0.8 lagging pf:

$$\text{Voltage drop} = 41.67\ (0.54 \times 0.8 + 1.98 \times 0.6) = +67.5\ \text{V}$$

$$\text{Voltage regulation} = \frac{+67.5}{2400} \times 100 = +2.81\%$$

$$\text{Secondary voltage} = \frac{2400 - 67.5}{4} = 583\ \text{V}$$

(ii) 0.8 leading pf:

$$\text{Voltage drop} = 41.67\ (0.54 \times 0.8 - 1.98 \times 0.6) = -31.5\ \text{V voltage rise}$$

$$\text{Voltage regulation} = \frac{-31.5}{2400} \times 100 = -1.31\%$$

$$\text{Secondary voltage} = \frac{2400 - 31.5}{4} = 607.9\ \text{V}$$

(c) For zero voltage regulation:

$$0.54 \cos\theta - 1.98 \sin\theta = 0$$

or $$\tan\theta = \frac{1.98}{0.54} = 3.67$$

$$\text{pf} = \cos\theta = 0.263 \text{ leading}$$

6.9 EFFICIENCY

The efficiency of transformer (or, in fact, any other device) is

$$\eta = \frac{\text{output power}}{\text{input power}}$$

or
$$\eta = \frac{\text{output}}{\text{output + losses}} = 1 - \frac{\text{losses}}{\text{output + losses}} \tag{6.56}$$

The transformer has two losses:

- Core (iron) loss P_i which is a constant loss[2]
- Copper (I^2R) loss, P_c (both windings), a variable loss.

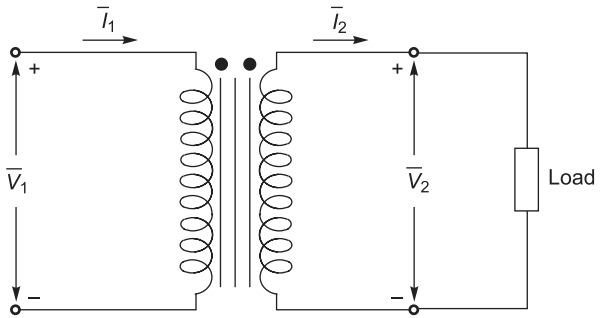


Fig. 6.26 *Transformer on load*

With reference to Fig. 6.26, a transformer on load,

$$\text{output} = V_2 I_2 \cos \theta_2$$

where $\cos \theta_2$ = load pf

From Eq. (6.57),

$$\eta = \frac{V_2 I_2 \cos\theta_2}{V_2 I_2 \cos\theta_2 + P_i + I_2^2 R_2} \tag{6.57}$$

where R_2 is the equivalent transformer resistance referred to secondary.

Reorganising Eq. (6.57)

$$\eta = \frac{V_2 \cos\theta_2}{V_2 \cos\theta_2 + (P_i / I_2 + I_2 R_2)} \tag{6.58}$$

For a given pf, the efficiency varies with the load current, maximum efficiency is achieved when Eq. (6.58) has minimum denominator, i.e.

$$I^2{}_2 R_2 = P_i \tag{6.59}$$

or copper loss = iron loss

or variable loss = constant loss

[2] Operation at constant voltage and frequency.

From Eq. (6.59), the efficiency is maximum at a load current of

$$I_2 = \sqrt{\frac{P_i}{R_2}}$$

and at a load of $V_2 I_2 \cos\theta$

1. *Power transformers*: These are the transformers employed at transmission level where the load throughout the day is nearly constant. These are designed to have η_{max} at full load.
2. *Distribution transformers*: The load at distribution level has considerable variations during the day. So these transformers are designed to have η_{max} at about $3/4^{th}$ full-load.

Example 6.13

A transformer is rated 10 kVA, 50 Hz 2300/230 V. Its equivalent resistance and reactance on the HV sides are 7.92 Ω and 3.16 Ω respectively. It has a core loss of 75 W at rated voltage of 2300 V.

(a) It is supplying a load of 10 kvA at 0.8 pf lagging at rated voltage 230 V. For this, the supply voltage on the HV side is 2410 V.

Compute its efficiency of operation. Assume the core loss to be proportional to the square of the applied voltage.

(b) By shunt capacitor, the power factor of the load in part (a) is reformed to 0.97 lagging. As a result, the supply voltage on the HV side needed is 2300 V, which means zero voltage regulation. Compute the transformer efficiency under the operating condition.

(c) Find the maximum efficiency of the transformer for a load of 0.8 pf.

Solution

(a) HV side voltage, $V_1 = 2410$ V

Core loss at this voltage, $P_i = 75 \times \left(\frac{2410}{2300}\right)^2 = 82.2$ W

Load current, $I = \frac{10 \times 10^{-3}}{2300} = 4.35$ A, HV side

Copper loss, $P_C = (4.35)^2 \times 7.92 = 150$ W

Total loss, $P_L = 82.3 + 150 = 232.3$ W

Power output, $P_0 = 10 \times 0.8 = 8$ kW

The efficiency is then found to be

$$\eta = \frac{8}{8 + 0.232} \times 100 = 97.2\%$$

(b) HV voltage, $V_1 = 2300$ V

$P_i = 75$ W

Power output, $P_0 = 9.7$ kW at 0.97 lagging

$$I = \frac{9.7 \times 10^3}{2300 \times 0.97} = 4.35 \text{ A}$$

$P_c = (4.35)^2 \times 7.92 = 149.8$ W

$P_L = 75 + 149.8 = 224.8$ W

$$P_0 = 9.7 \text{ kW}$$

$$= \frac{9.7}{9.7 + 0.228} \times 100 = 97.7\%$$

(c) For maximum efficiency

$$I^2R = P_i$$

or $$I^2 \times 7.92 = 75$$

It is assumed above that $P_i = 75$ W remains constant as the voltage drop in the transformer is small and V_1 and V_2 are both close to the rated values.

Now

$$I = \left(\frac{75}{7.92}\right)^{1/2} = 3.08 \text{ A}$$

$$\text{Load} = 2300 \times 3.08 = 7.08 \text{ kVA at 0.8 pf}$$

$$= 86.5\% \text{ of full load}$$

$$P_0 = 3.08 \times 2300 \times 0.8 = 5.667 \text{ kW}$$

$$P_L = 2 \times 75 = 150 \text{ W}$$

$$\eta = \frac{5.667}{5.817} = 97.4 \text{ s}$$

6.10 THREE-PHASE TRANSFORMERS

Three identical single-phase transformers can be connected to form a three-phase bank. Primary and secondary sides of the bank can be connected in star/delta with various possible arrangements as

- star/star
- delta/delta
- star/delta or delta/star

Instead of three single-phase transformers, it costs about 15% less to have a single three-limb core as shown in Fig. 6.27 with primary and secondary of a phase wound on each limb. Like the sum of the currents in three-phase in zero, the sum of the fluxes in the three limbs at any instant is zero providing for continuous flux paths. For reasons of economy, this arrangement (three-limb core) is popularly used. Of course, if one phase is out, the complete transformer must be replaced.

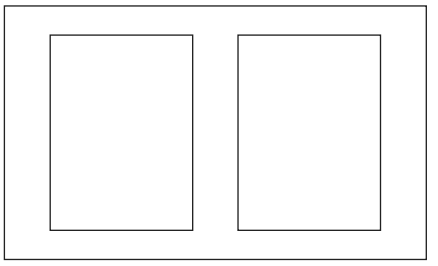


Fig. 6.27 *Three-phase transformer core*

In finding voltages and currents in a three-phase transformer along with the ratio of transformation between the coupled windings, one must employ the line and phase relationship of star/delta connections with the assumption that the transformer is feeding a balanced load. Figure 6.28 shows a three-phase transformer connected in delta on the primary side and star on the secondary side. In this figure, the coupled windings are drawn parallel to each other for ease of identification. Various line and phase voltages and currents are indicated on the figure (these follow easily). For a phase-to-phase transformation ratio of a : 1 (delta/star)

$$\frac{V_{\text{line}}(\text{star})}{V_{\text{line}}(\text{delta})} = \frac{\sqrt{3}\,V/a}{V} = \frac{\sqrt{3}}{a}$$

and

$$\frac{I_{\text{line}}(\text{star})}{I_{\text{line}}(\text{delta})} = \frac{aI/\sqrt{3}}{I} = \frac{a}{\sqrt{3}}$$

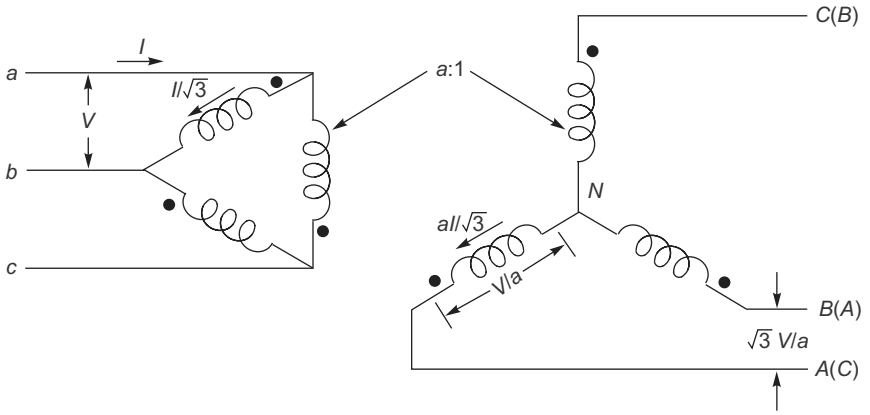


Fig. 6.28 *Delta/star transformer connection (phase shift +30°)*

Phase Shift

In star/star and delta/delta connection, the line voltages and currents are in phase on the primary and secondary sides. However, in a delta/star connection, the line voltages and currents undergo a shift in phase which can be ±30° or ± 90° depending upon the connections.

The delta/star connection of Fig. 6.28 with polarity marks indicated is a commonly used connection. The phasor diagram for voltages is shown in Fig. 6.29. The phase sequence is assumed to be *abc*/*ABC*.

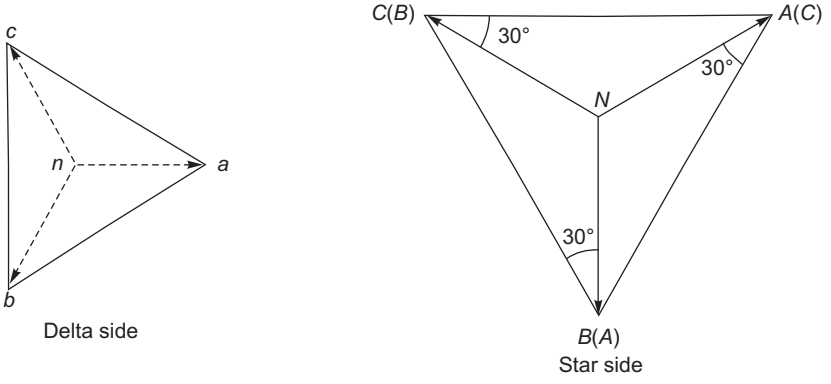


Fig. 6.29 *Voltage phasor diagram of delta/star connection of Fig. 6.28*

It is observed from above that the line voltages on star side, lead the line voltages on delta side by 30°, viz. V_{ab} by 30°. The phase shift would become –30° by changing the phase sequence to *acb*/ACB, viz. V_{AC} by 30°. Relabelling the terminals on the star side, as shown within brackets, would make the phase shift –90° viz. V_{AB} lags V_{ab} by 90°. The reader may relabel to make the phase shift +90°. The line currents would undergo the same phase shift as line voltages in balanced three-phase loading.

In power system applications of transformers, it is standard practice to connect the transformers (Δ/Y) such that the phase shifts by +30° in going from LV side to HV side.

Star/Delta Connection

It is the most commonly used connection as the delta side provides a low impedance path for third harmonic current to flow, thereby reducing third harmonic voltage on the lines. At transmission level, the low voltage side is connected delta and the high voltage side is connected star. This provides for neutral grounding connection for high-voltage transmission. However, at distribution level, the delta-star with star connection on low voltage side is employed to provide a neutral wire for feeding three-phase and single-phase loads.

Example 6.14

A three-phase transformer consisting of three 1-phase transformers with turn ratio of 10 : 1 (primary : secondary) is used to supply a three-phase load of 120 kVA at 400 V on the secondary side. Calculate the primary line current and voltage if the transformer is connected (a) Δ/Y (b) Y/Δ. What is the line-to-line transformation ratio in each case?

Solution

(a) Δ/Y-connection (Fig. 6.30a):

$$I = \frac{120 \times 1000}{\sqrt{3} \times 400} = 173.2 \text{ A}$$

$$\text{Primary line-to-line voltage} = \frac{aV}{\sqrt{3}} = 10 \times \frac{400}{\sqrt{3}} = 2309 \text{ V}$$

$$\text{Primary line current} = \frac{\sqrt{3}I}{a} = 1.732 \times 173.2 \times \frac{1}{10} = 30 \text{ A}$$

Line-to-line transformation ratio (primary/secondary):

$$= \frac{aV/\sqrt{3}}{V} = \frac{a}{\sqrt{3}} = \frac{10}{\sqrt{3}}$$

(b) Y/Δ-connection (Fig. 6.30b)

$$I = 173.2 \text{ A}$$

$$\text{Primary line-to-line voltage} = \sqrt{3}aV = \sqrt{3} \times 10 \times 400 = 6928 \text{ V}$$

$$\text{Primary line current} = \frac{1}{a\sqrt{3}} = \frac{173.2}{10 \times 1.732} = 10 \text{ A}$$

$$\text{Line-to-line transformation ratio} = \frac{\sqrt{3}aV}{V} = \sqrt{3}a = 10\sqrt{3}$$

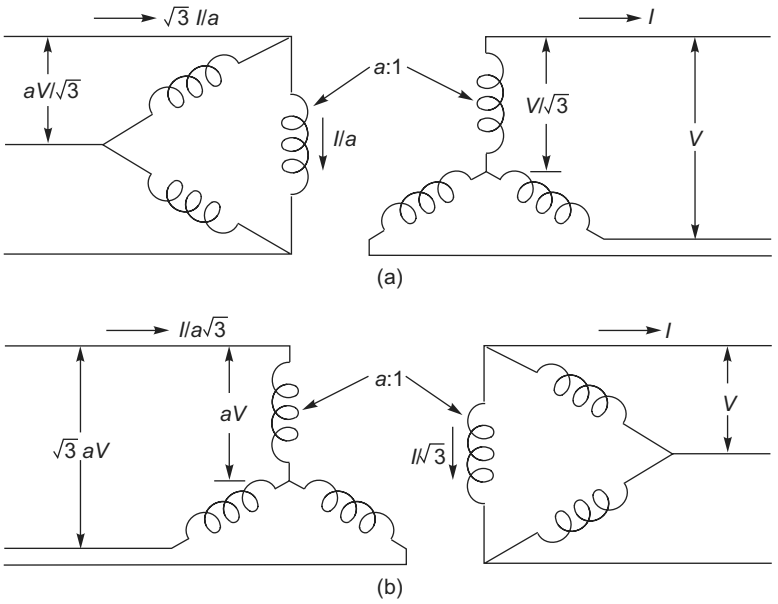


Fig. 6.30

Summary

- A transformer comprises of two mutually coupled coils wound on a magnetic core to carry the mutual flux, thereby making the coupling very tight.
- A transformer which can raise the voltage level of the source and correspondingly bring down the current level is called a step-up transformer OR if it can bring down the voltage level and raise the current level then it is called a *step-down* transformer.
- The windings are made of conducting wires, copper or aluminium and the core is made of lightly insulated *laminated* (thin sheet joined together) *silicon steel*.
- The winding connected to the source is called the *primary* and the second winding that feeds the load is called the *secondary*.
- To avoid confusion, the windings are referred to as HV and LV windings.
- The transformers have two types of cores—core type and shell type; the core type is most common in use.
- Core type: core is rectangular with half LV and half HV on opposite limbs with LV placed inside next to core. This split winding arrangement reduces leakage flux and is economical insulation-wise.
- Ideal transformer transforms voltage in direct ratio of primary and secondary turns and transforms currents in the inverse ratio of turns. Symbolically,

  $$\frac{V_1}{V_1} = \frac{N_1}{N_1} = \frac{I_2}{I_2} = a\text{(turn ratio)}$$

  It transforms impedance from one side to the other in direct square ratio of turns and admittance in inverse square ratio of turns. Thus,

$$Z_1 = \left(\frac{N_1}{N_2}\right)^2 Z_2, \quad Y_1 = \left(\frac{N_2}{N_1}\right)^2 Y_2$$

- The transformer core flux is

$$\phi_{max} = \frac{V_1}{\sqrt{2}\pi f N_1} = \frac{V_2}{\sqrt{2}\pi f N_2}; \ \sqrt{2}\pi = 4.44$$

- In a real transformer, the relationship holds for induced emfs but is approximately acceptable for voltages. Observe that the relationship is independent of primary and secondary currents.
- Core flux lags induced emfs by 90°.
- In a real transformer, *magnetising current* (I_m) is drawn by the primary (which is connected to the source). It lags the applied voltage by 90°.
- Magnetising current is accompanied by the core loss current (I_i) in phase with the applied voltage.
- Exciting current of a transformer is $\overline{I}_0 = \overline{I}_m + \overline{I}_i$; lags applied voltage by slightly less than 90° as $I_i << I_m$
- Exciting current of a transformer is far less than its rated load current.
- Power (active and reactive) is transferred from the primary to secondary side by the load current and not by the exciting current. In fact, the exciting current produces flux in the core so that the transformer can carry load current.
- Secondary AT = N_2I_2 are equal and opposite the load component of primary AT = N_1I_1 such that core flux does not change.
- Each transformer winding has resistance and leakage reactance (caused by leakage flux).
- Transformer resistance and reactance can be referred to any one side as

  $R_1 = r_1 + a^2r_2, \qquad X_1 = x_1 + a^2x_2;$

  a = turn ratio = $\frac{N_1}{N_2}$

  $R_2 = r_2 + \frac{1}{a^2}r_1, \ X_2 = x_2\frac{1}{a^2}x_1$
- A transformer circuit model (also called equivalent circuit) comprises
  - magnetising branch (G_i || B_m) in shunt across the applied voltage,
  - series branch ($R + jX$) connecting the source to the ideal transformer, and
  - ideal transformer; it may not be shown in the circuit diagram; usually omitted.
- Transformer losses:
  - Core loss (P_i); constant for constant applied voltage
  - Copper loss (P_c); variable proportional to the square of the load current
- Determination of circuit model (equivalent circuit) parameters by two tests, OC and SC
- *OC (Open Circuit) Test*: One side excited at rated voltage, the other side left open.

  Three meter readings taken:

  V_1, I_0, $P_0 = P_i$ (core loss)

  $Y_0 = \frac{V_1}{I_0}, \ G_i = \frac{P_0}{I_0^2}, \ B_m = \sqrt{Y_0^2 - G_i^2}$

➢ *SC (Short Circuit) Test*: One side shorted, low voltage applied on the other side.

Three meter readings taken.

V_{sc}, I_{sc}, P_{sc} (copper loss)

$$Z = \frac{V_{SC}}{I_{SC}},\ R = \frac{P_{SC}}{I_{SC}^2},\ X = \sqrt{Z^2 - R^2}$$

There are equivalent values on the test side.

➢ *Per Unit System*

$(KVA)_B$ or $(MVA)_B$ taken as transformer rating (convenient) voltage bases must be in ratio of transformation. It is convenient to use rated voltage on each side.

$(KV)_B$ (HV) and $(kV)_B$ (LV)

$$Z_B = \frac{(KV)_B^2}{(MVA)_B}$$

$$Y_B = \frac{1}{Z_B}$$

Then

$$Z(\text{pu}) = \frac{Z(\Omega)}{Z_B},\ Y(\text{pu}) = \frac{Y(\Omega)}{Y_B}$$

For a three-phase system, use three-phase (KVA) or (MVA) as base and line-to-line kV as base. The above relations apply. Z(pu) and Y(pu) are per phase values on equivalent star.

➢ % Voltage regulation = $\dfrac{V_{2.0} - V_{2.1f_1}}{V_{20\,f_1}} \times 100$

V_{20} = secondary voltage when full-load is thrown off with circuit represented on any side

Voltage regulation = $\dfrac{V_2 - V_1}{V_2} \times 100$

$V_2 - V_1$ = voltage drop $\approx I\,(R \cos\theta \pm X \sin\theta)$; + for lagging, − for leading

➢ Efficiency (η) = $\dfrac{\text{Output power}}{\text{Input power}}$

For η (max), $P_C = I_2^2 R_2 = P_2$ or $I_2 = \sqrt{\dfrac{P_i}{R_2}}$

➢ Three-phase transformer—three identical single-phase transformers connected in star/delta, the most common configuration at transmission level is LV side, delta connected and HV side star connected; neutrals on HV side are grounded.

At distribution level, HV side is delta connected and LV side is star connected; neutral of star is used to supply single-phase load.

➢ Depending upon line labelling and phase sequence, the line voltage on the two sides of a star/delta transformer got shifted by ±30° or ±90°. The labelling used in practice is 30°.

Exercises

Review Questions

1. What is a transformer? Explain the function it fulfils as an element of a power system.
2. Explain the constructional differences between core and shell-type transformers.
3. Explain briefly the ideal transformer as a circuit element. Can voltage and current ratios be adjusted independently?
4. Explain the operation and application of the impedance transforming property of an ideal transformer.
5. State how the LV and HV windings are arranged in a core-type transformer. Explain the reason.
6. What is the phase relationship between the core flux, the magnetising current and the induced emfs in the primary and secondary winding of a transformer? Draw the phasor diagram.
7. What is the transformation ratio of a transformer? Why is it not identical to voltage ratio of a transformer?
6. What determines the maximum value of flux in a transformer core when excited from the primary side? Does the value of flux change substantially when the secondary is loaded? Explain the reason.
9. Explain how the OC/SC tests separate out the core loss and copper loss.
10. A transformer is excited from the primary side at rated voltage but with secondary open. Would it draw any current? If so, what is action of this current and its components?
11. Why cannot the SC test separate out the primary and secondary resistances and leakage inductances?.
12. Justify that under SC test the core loss is negligible.
13. Prove that in the system, if the voltage bases are selected in the ratio of transformation, the pu impedance of the transformer is same as either side.
14. State and prove the condition for maximum efficiency of a transformer.
15. Draw the phasor diagram of a transformer as seen from any one side for zero voltage regulation.
16. From the phasor diagram of Question 15, derive the approximate condition for zero voltage regulation.
17. Justify the statement that in the circuit model of a transformer in a power system, the magnetising branch can be ignored.
18. Explain the meaning of all the items in the nameplate of a transformer.
19. How can we refer the transformer winding resistance and leakage reactance from one side to the other?
20. From the percentage impedance given as the name plate, how can you find the voltage to be applied for full load current to flow in SC test?
21. Draw the equivalent circuit of a transformer. Identify the test by which the value of each circuit element can be found.

Problems

1. A single-phase transformer is rated 600/200 V, 25 kVA, 50 Hz.
   (a) Calculate the magnitude of primary and secondary currents when the transformer is fully loaded (use IT model).
   (b) What should be the impedance of the load in ohms to fully load the transformer when connected on (i) 600 V side, and (ii) 200 V side (use IT model)?
   (c) What would be the value of the maximum core flux when the transformer is excited at rated voltage on either side, given $N_1 = 60$ turns?
   (d) If the transformer is operated from a 60 Hz source, what should be its voltage rating for the maximum core flux to stay at the same value as in part (c)?
   (e) If the 600 V side is excited at 600 V, 40 Hz, what would be the core flux and the secondary voltage? What effect do you expect to observe in the core under these conditions?
2. A 25 kVA, 600/200 V transformer is subjected to an SC test. The voltage applied on one side, with the other shorted, is 5.2% of the rated voltage. The transformer draws rated current and a power of 242 W during the test.

(a) Compute equivalent resistance and leakage reactance of the transformer in ohms on either side and in pu.
(b) Compute the core flux as a percentage of core flux at rated voltage.
(c) From part (b), justify that all the 242 W constitute ohmic losses.

3. A 25 kVA, 600/200 V transformer is found by the SC test from the 600 V side to have equivalent resistance 0.139 Ω and equivalent reactance 0.735 Ω, as seen from the HV side. A load impedance of $\bar{Z}_L = 1.48 + j1.04\ \Omega$ is connected across the secondary.
(a) Find currents in both windings assuming transformer to be ideal.
(b) Solve part (a) again by taking the transformer impedance into account.
(c) Calculate voltage regulation of the transformer.
4. The 25 kVA, 600/200 V transformer when subjected to SC test from the 600 V side is found to have equivalent resistance of 0.139 Ω. and equivalent reactance of 0.73542. The transformer is now OC tested from a 600 V source with the secondary open. The transformer draws a power of 195 W.

   Compute the efficiency of the transformer when loaded with $\bar{Z}_L = 1.48 + j\ 1.04\ \Omega$. on the secondary side.
5. A 50 kVA, 1100/220 V, 50 Hz transformer has an HV winding resistance of 0.125 Ω and a leakage reactance of 0.625 Ω. The LV winding has corresponding values of 0.005 Ω, and 0.025 Ω, respectively. Find the equivalent impedance of the transformer referred to HV and LV sides. Find the pu impedance of the transformer.
6. Consider the transformer of Problem 5 to give its rated output at (a) 0.8 lagging pf, and (b) 0.8 leading pf on the LV side. Find the HV terminal voltage and % regulation. Use pu system.
7. The transformer of Problem 5 has a core loss of 580 W. Find its efficiency at 3/4th full load, 0.8 lagging pf.
8. A 50 kVA, 1100/220 V, 50 Hz transformer has an HV winding resistance of 0.125 Ω and a leakage reactance of 0.625 Ω. The LV winding has corresponding values of 0.005 W and 0.025 W respectively. Wehn excited from 1100 V source gets shorted at LV terminals. Find the steady-state current which would be drawn by the HV if the source voltage is assumed to remain constant.
9. The transformer of Problem 5 is fully loaded on the secondary side at (a) 0.8 lagging, and (b) 0.8 leading pf while it is fed on the primary side at 1100 V. Calculate the voltage at the secondary terminals.
10. The circuit model of a 5 kVA, 200/400 V, single-phase transformer, referred to the LV side, is shown in Fig. 6.31.
    (a) An OC test is conducted from the HV side at 400 V. Calculate the power input, power factor and current (magnetising) drawn by the transformer.
    (b) An SC test is conducted from the LV side by allowing full-load current to flow. Calculate the voltage required to be applied, the power input and power factor.

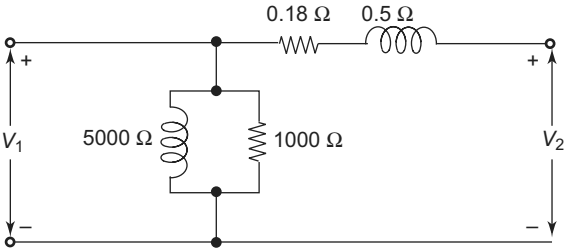


Fig. 6.31

11. The following test results were obtained on a 20 kVA, 2200/220 V transformer:
    OC test (LV): 220 V, 1.1 A, 125 W
    SC test (HV): 52.7 V, 6.4 A, 287 W
    (a) The transformer is loaded at unity pf on secondary side with a voltage of 220 V. Determine the maximum efficiency and the load at which it occurs.

(b) The transformer is fully loaded. Determine the load pf for zero voltage regulation.

12. A Δ/Y connected three-phase transformer as shown in Fig. 6.29 has a voltage ratio of 22 kV (Δ)/345 kV (Y) (line-to-line). The transformer is feeding 500 MW and 100 MVAR to the grid (345 kV). Determine the kVA and voltage rating of each unit and compute all currents and voltages in both magnitude and phase in lines and all the windings (three primaries and three secondaries). Assume the transformer units to be ideal.
13. Three identical transformers each rated 6.6/22 kV, 3 MVA, are connected in Y/Y. The transformer bank is fed from a source of line voltage $6.6\sqrt{3}$ kV . The secondary side feeds a delta-connected load composed of three equal impedances. Assuming the individual transformers to be ideal find
    (a) the value of Z in ohms to fully load the bank (i.e. 9 MVA),
    (b) the current in each leg of the load (Δ connected), and
    (c) the current in each transformer primary and secondary.
14. The three transformers of Problem 13 are connected in Δ/7 and are fed from 6.6 kV (line-to-line) source on Δ side. The load comprises three Δ-connected impedances. Assuming all the three transformers to be ideal solve for all parts of Problem 14. Also, find the primary and secondary side-line currents.

Multiple-Choice Questions

1. The core in a large power transform is built of
   (a) contain (b) mild steel (c) fertile (d) silicon steel
2. P_i = core loss, P_c = copper loss = A transform has maximum efficiency which.
   (a) $P_i/P_c = 2$ (b) $P_i/P_c = 1.5$ (c) $P_i/P_c = 1$ (d) $P_i/P_c = 0.5$
3. A transformer has $R \approx 0$ and a pu reactance of 0.1. Its voltage regulation on full-load with a pf angle of 30° leading is
   (a) 5% (b) –5% (c) 10% (d) –10%
4. Power input to a transformer on load at rated voltage comprises predominantly
   (a) copper loss (b) hysteresis loss (c) core loss (d) eddy-current loss
5. A transformer operates most efficiently at ¾ full load. Its iron loss (P_1) and full load copper loss (P_c) are related as
   (a) $P_i/P_c = 16/9$ (b) $P_i/P_c = 4/3$ (c) $P_i/P_c = ¾$ (d) $P_i/P_c = 9/16$
6. The core of a transform is laminated, which is lightly insulated by varnish is to reduce
   (a) hysteresis loss (b) eddy-current loss
   (c) both hysteresis and eddy-current loss (d) core reluctance
7. In an ideal transformer, the impedance transforms from one side to other
   (a) direct square ratio of turns (b) direct ratio of turns
   (c) increase square ratio of turns (d) inverse ratio of turns
8. The no-load current in a transformer wrt the primary voltage
   (a) leads by 90° (b) lags by 90°
   (c) leads by slightly less than 90° (d) lags by slightly less than 90°
9. In a transformer, the flux phasor
   (a) leads the induced emf phasor by 90°
   (b) lags the induced emf phasor by 90°
   (c) is in phase with the induced emf phasor
   (d) is in phase opposition to the induced emf phasor
10. In a transformer, zero voltage regulation is achieved at a load pf which is
    (a) leading (b) lagging (c) unity (d) zero

Answers

Multiple-Choice Questions

1. (d) 2. (c) 3. (b) 4. (c) 5. (d) 6. (c) 7. (c) 8. (b) 9. (a) 10. (a)

dc Machines

chapter 7

Goals & Objectives

- To familiarise with constructional details; the commutation
- Winding types, lap-winding connections to commutation and brushes
- Derivation and clarity of relationships for emf and torque, power conversion
- To distinguish between generating and motoring machine
- To picturise armature reaction in space relationship to the main field, effects and remedy
- To acquire clear understanding of communication, effect of reactance emf and remedy, the interpoles
- The field excitation and excitation types, machine types
- Characteristics of dc generator
- Open-circuit characteristic of a dc machine
- Versatility of dc motor speed and torque controlled by the field (stator) and the armature (rotor)
- Speed-torque characteristics of the three motor types and their methods of speed control
- Starting of dc motors

7.1 INTRODUCTION

A dc machine is constructed in many forms and for a variety of purposes, from the 3 mm stepper drawing a few μA, 1.5 V in a quartz crystal watch to the giant 100 MW or more rolling mill motor. It is a highly versatile and flexible machine. It can satisfy the demands of load requiring high starting, accelerating and retarding torques. A dc machine is also easily adaptable for drives with a wide range of speed control and fast reversals.

The dc motors are used in rolling mills, in traction and in overhead cranes. They are also employed in many control applications as actuators and as speed or position sensors. With ac being universally adopted for generation, transmission and distribution, there are almost no practical uses now of the dc machine as a power generator. Its use as a motor-generator (ac motor-dc generator) for feeding dc drives has also been replaced in modern practice by rectifier units. In certain applications dc motors act as generators for brief periods in the 'regenerative' or 'dynamic braking' mode, especially in electric traction systems.

The use of an electric field winding, which supplies electric energy to establish a magnetic field in the magnetic circuit, results in great diversity and a variety of performance characteristics. The armature winding is connected to the external power source through a *commutator-brush* system [see Fig. 7.6(a), item 6] which is a mechanical rectifying (switching) device.

The objective of this chapter is to analyse the behaviour of the dc machine and present the physical concepts regarding its steady-state performance.

7.2 CONSTRUCTIONAL AND OPERATIONAL FEATURES

A dc machine has field poles on the rotor, which are dc excited. The rotor constitutes the armature, which carries the armature windings as shown in the cross-sectional view of an elementary 2-pole dc machine with a single armature coil in Fig. 7.1. As the rotor rotates, an alternating emf is induced in the coil, which, under load, would carry alternating current. In order to have dc voltage at the terminals and to feed dc load current, the alternating armature current has to be *rectified*.

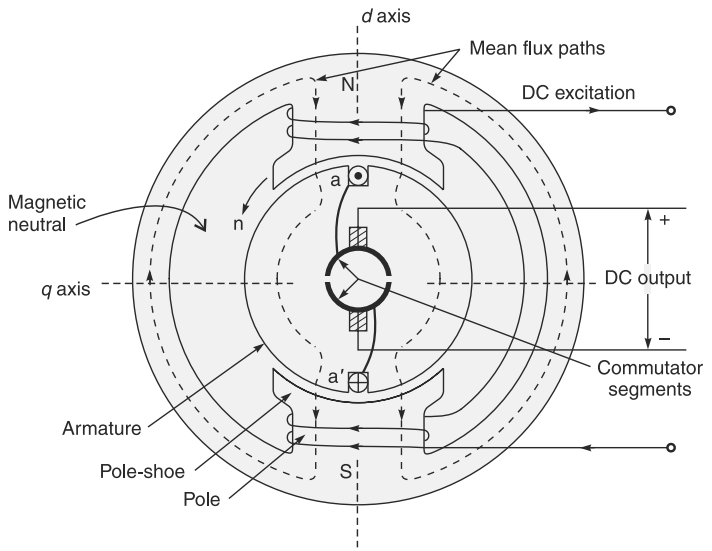


Fig. 7.1 *A 2-pole elementary dc machine*

Rectification is accomplished by a mechanical rectifier called the *commutator*, which is carried on the rotor shaft and so rotates along with armature. In the elementary machine, the commutator comprises two *copper segments* insulated from each other by thin mica insulation and are also insulated from the shaft as shown in Fig. 7.1. The coil ends are connected to the segment, and two *carbon brushes* in sliding contact with the segments conduct current to the external circuit. It is easily seen that as the armature current and emf reverses, the brush contacts reverse simultaneously such that brush voltage and current are unidirectional.

As constant unidirectional brush voltage is the aim, the B-wave is the made flat topped by (i) uniform air-gap under the poles, and (ii) making the pole shoes wider. For this reason, the dc poles are always salient kind with each pole shoe covering about 70% of the pole pitch (π rad) as shown in Fig. 7.1. Typical B-wave of a dc machine and the rectified coil emf wave (brush voltage) are sketched in Fig. 7.2(a) and (b) respectively.

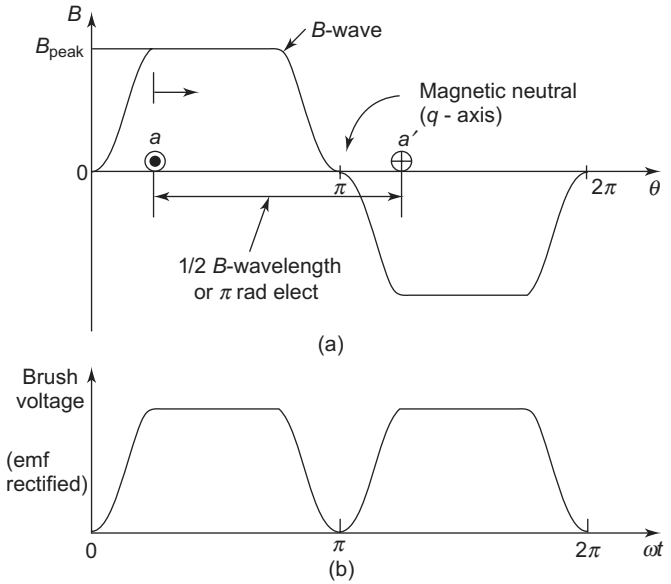


Fig. 7.2 *B-wave and brush voltage in a dc machine*

Smooth dc voltage would be obtained when the armature is wound with several coils placed in slots. Two coils slide round the armature and as many commutator segments to each of which two coil-ends are connected.

The cross-sectional view of a 2-pole dc machines with 12 coils (24 coil sides) connected to 12 commutator segments which are tapped by 2 brushes is shown in Fig. 7.4. As the armature and commutator segments pass the brushes, the coil side current passing under each pole remains the same, while coils connected to segments 1 and 2 are shorted (have zero induced emf being in the interpolar region) undergo current reversal, the process of commutation.

Axes of dc Machine

It is convenient to identify two axes of a dc machine (applies to all electric machine).

The axis of the magnetic pole (middle of the pole) is called the *d*-axis and the axis midway between poles (inter-polar region) is called the *q*-axis, which is at 90° elect degrees to the *d*-axis.

The two axes are identified on the 2-pole dc machine of Fig. 7.1.

Longitudinal and cross-sectional views of a dc machine are drawn in Fig. 7.5(a) and (b) respectively. All the important machine parts, their location and general shape are clearly brought out by these figures, which would be referred to repeatedly.

7.3 ARMATURE WINDINGS AND COMMUTATION

In a practical dc machine, there may be more than two poles and there are a number of armature coils (single or multi-turn) accommodated in slots in two layers. The coils are full-pitched and one side of a coil is in top in one slot and its second side is in bottom of a slot, one pole pitch (π radians) away. To each segment are connected the coil ends of two different coils; starting end of one coil and finishing end of the other. Therefore, *there are as many commutator segments as the number of armature coils. The armature coils are connected in two possible ways—lap winding and wave winding*. We shall consider lap winding only.

Lap Winding

In a book of first level, the purpose is to explain as to how the coils are wound and how are they connected to the commutator segments.

We shall take the example of 4-*pole*, *12-armature slots*, *single-turn coils and 2 coil-sides per slot*. The best way to draw a winding diagram is in developed form, which is explained below.

Developed Diagram

Imagine the armature surface to be cut parallel to the axis of rotation and laid out on a plane with poles underneath and slots on top, with top-layer coil-sides shown by solid lines and bottom-layer coil-sides shown by dotted lines, as in Fig. 7.3. The commutator segments appear on the lower side of the diagram numbered consecutively. The coil-sides are numbered top and bottom consecutively. As the last coils on each side cannot be shown connected, the connectivity is indicated by coil-side numbering scheme. We find

Number of coils = number of slots = 12; two coil-sides/slot

Number of commutator segments =12

Number of slots under each pole = 12/4 = 3

Coil span (full pitch) =12/4 = 3 slots

The current direction of coil-sides ($2 \times 3 = 6$) over the poles alternates is as shown in the diagram. In the coil-side numbering scheme adopted, odd-numbered coil-sides are in top layer and even numbered coil-sides are in the bottom layer. In all, the coil-side numbers for the example in hand are 1 to 24.

Coil span in terms of coil-sides = $2 \times 3 + 1 = 7$

Thus coil-sides 1 and 8 form one coil, 3 and 10 form the next coil, and so on. Further, the coils are diamond shaped.

The winding proceeds with the starting end of one coil connected to a commutator segment and the finishing end to the next consecutive commutator segment, to which the starting end of the next consecutive coil is also connected. The winding thus progresses with partially overlapping coils till the winding closes onto itself. It is also observed that the winding progresses by one commutator segment for each coil, which means that

Commutator pitch = 1 segment

In the winding diagram of Fig. 7.3, coil-side 1 is connected to segment 1 and coil-side 8 (of the same coil) to segment 2, to which is connected coil-side 3 of the next coil and so forth.

Brushes and Parallel Paths

The brushes are placed at the commutator segments where the current in both coil ends connected to that segment either comes out or goes in. It is seen from the diagram that this happens at commutator segment numbers 1, 4, 7 and 7. Thus, there are four brushes equal to the number of poles and the adjoining brushes are

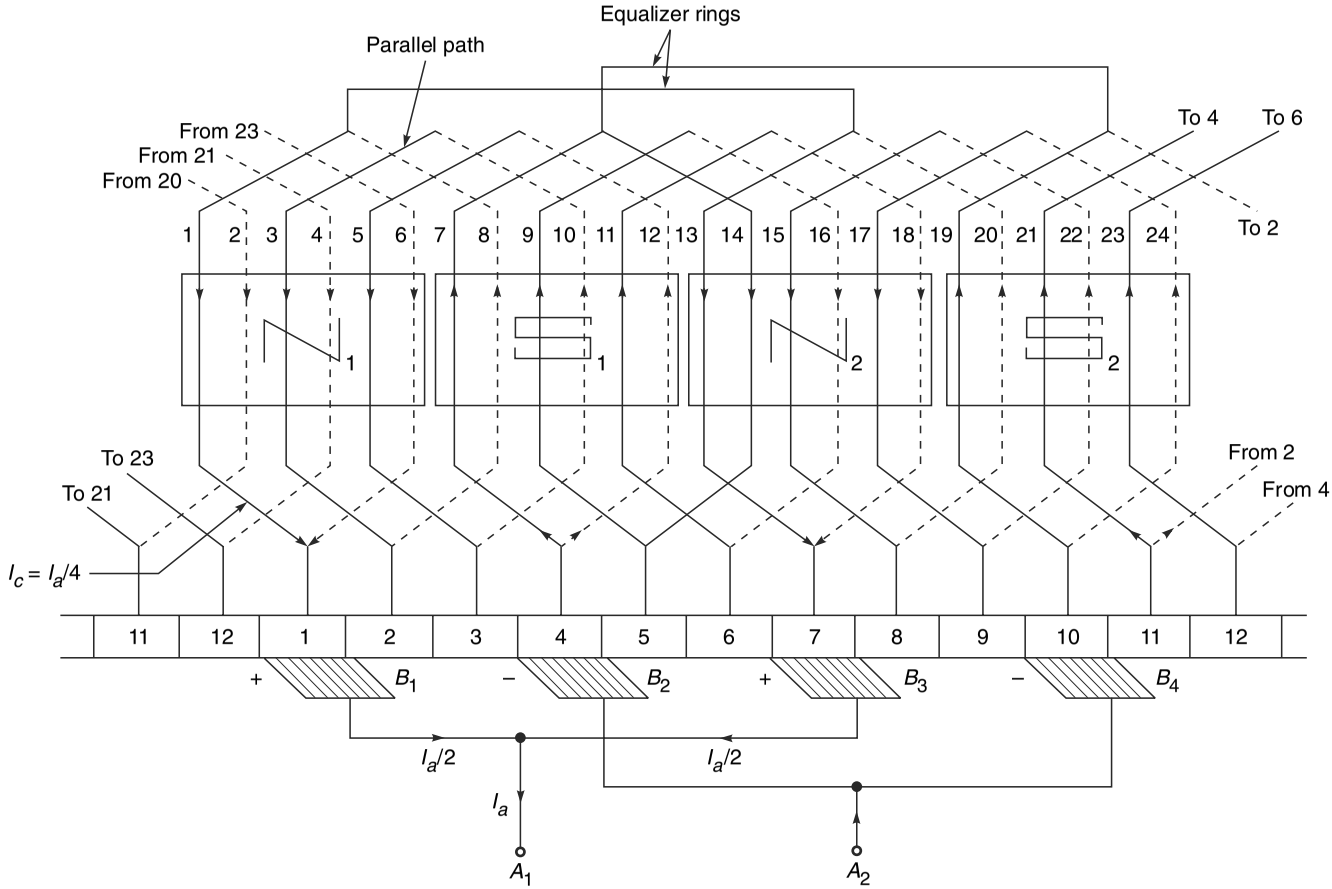


Fig. 7.3 *2-pole lap-winding, 12 armature slots; single-turn coils and 2 coil-sides/slot*

12/4 = 3 segments apart. Further, the alternate brushes are positive (current coming out) and negative (current going in). Similar polarity brushes are connected in parallel as shown in the diagram.

Further, the winding can be divided into four parallel paths (equal to number of poles); each parallel path having 12/4 = 3 coils in series spread over two adjoining poles. Also, each parallel path coils are getting connected to opposite polarity brushes. As the armature rotates, one coil goes out of a parallel path and simultaneously another comes in. Thus, at any instant, the same number of series-connected coils are similarly disposed under a given pole pair and hence the brush voltage is dc (constant).

Two cross-sectional view of dc machine exhibiting armature winding. Commutator and brushes are shown in Fig. 7.1

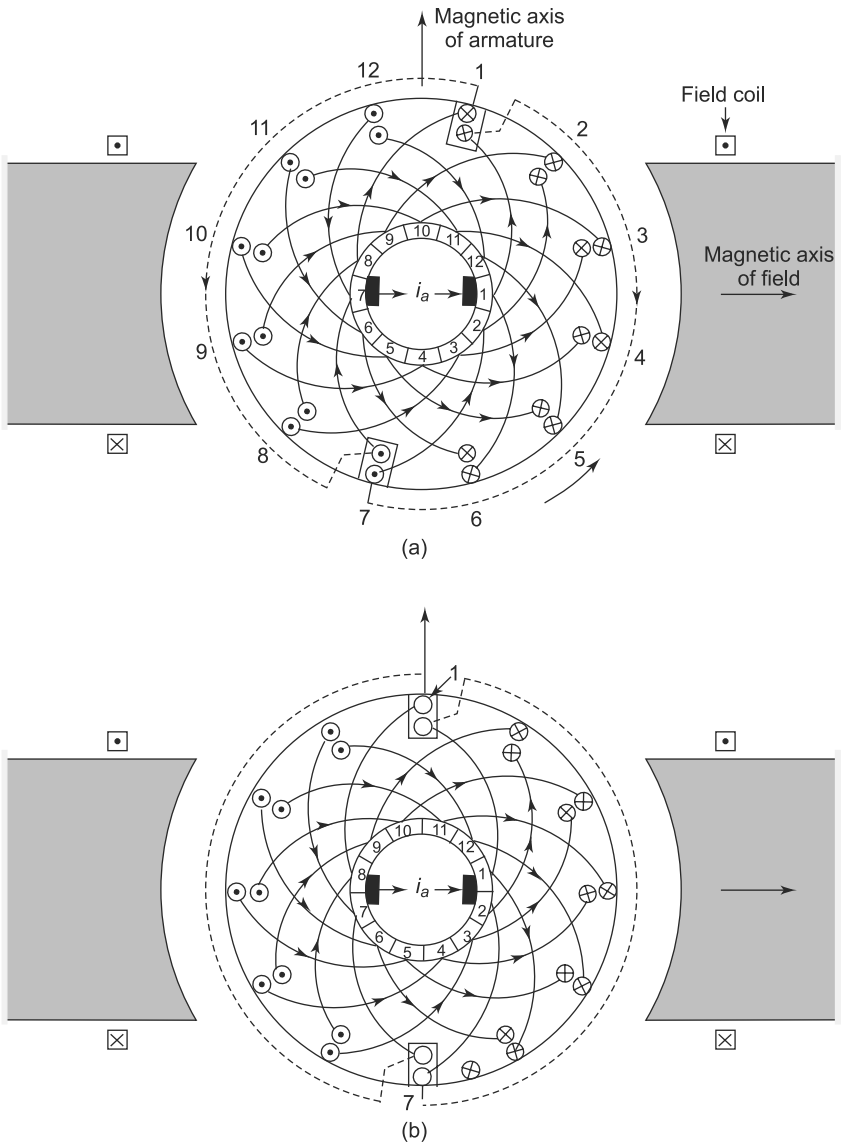


Fig. 7.4 *(a) dc machine armature winding with commutator and brushes, (b) Current directions for two positions of the armature*

One more observation is made from the winding diagram of Fig. 7.3 that because of diamond shaped coils, the brushes are physically located opposite the middle of the poles (the *d*-axis) but electrically these are connected to the coils in the inter polar region (the *q*-axis).

Ring Diagram

The ring diagram of the lap winding of Fig. 7.3 is drawn in Fig. 7.5 with the commutator in actual circular form while the coils connected between adjacent segments are shown schematically. The location of brushes, their external connections and the pole pairs under which the various coil sets (three coils each) lie are also indicated therein. It is seen that the winding is a closed one. As the parallel-path emfs are equal and the way they are connected, the sum of emfs is zero and so current would not flow in the absence of the load current.

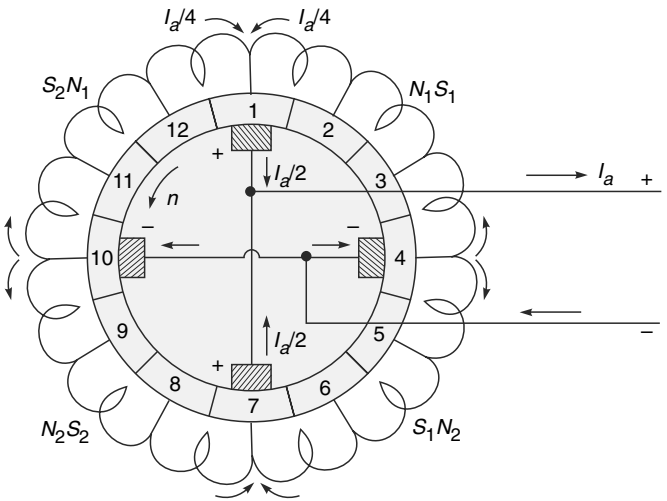


Fig. 7.5 *Ring diagram of lap winding of Fig. 7.3*

Equaliser Rings

Irrespective of the statement made above, the sum of emfs may not be exactly zero because of the slight differences in flux/pole of all poles. As the closed-path resistance is very small, a large current might flow in the windings. This is prevented by providing equaliser rings shown in Fig. 7.3. These rings are placed on the other side of the armature, connecting the points of equipotential. Any derivation of the potential difference is eliminated as the current flow in the rings is of negligible resistance, but no currrent flows in closed armature windings.

To summarise for *lap winding*:

No. of parallel paths, $A = P$ (7.1a)

No. of brushes $A = P$ (7.1b)

Conductor current $I_c = I_a/A$ (7.1c)

where I_a is the armature current (See Figs 7.3 and 7.4).

In a *wave winding*, the coil connections instead of lapping backward move forward from a coil under one pole pair to a coil under the next pole pair and so forth. The wave-winding diagram is not under the scope of this book but the conclusions are as under.

No. of parallel paths $A = 2$ (independent of number of poles) (7.2a)

No. of brushes = 2 (minimum needed but P brushes are used in practice) (7.2b)

$$\text{Conductor current } I_c = I_a/A = I_a/2 \tag{7.2c}$$

The interested reader may consult reference. [the book "Electric Machines", 4th edn, TMH, by the same authors]

Some further observations can be made from Fig. 7.3. The brushes are located mechanically opposite the main pole centres, i.e. in the magnetic axes of the poles, but because of the diamond shape of armature coils, these get connected to coil sides lying in or close to the interpolar region (magnetic neutral axis). Further, as a coil moves out of the influence of a given pole pair, the current in this coil must reverse. This process of current reversal, which is essential to a dc machine operation is known as *commutation*.

The reversal of current is opposed by the static coil emf ($L\,di/dt$) and therefore must be aided in some fashion for smooth current reversal, which otherwise would result in sparking at the brushes. The aiding emf is dynamically induced into the coils undergoing commutation by means of *compotes* or *interpoles* which are series excited by the armature current. These are located in the interpolar region of the main poles and therefore, influence the armature coils happens only when these undergo commutation. This will be dealt at length in Section 7.6.

Figures 7.5 (a) and (b) give the longitudinal and cross-sectional views of a dc machine, wherein the interpoles are clearly indicated as distinct from the main poles. Also, observe in Fig. 7.5(b) the construction of the commutator segments and how these are connected to the armature coils and the brushes.

7.4 emf AND TORQUE

7.4.1 emf Equation

Full-pitch armature coils are assumed. Let

Φ = flux/pole

Imagine the coil in Fig. 7.2(a), to lie in the interpolar region linking all the flux of one pole. Thus, its flux linkages are

$$\lambda_1 = N_c\Phi$$

where N_c is the number of coil turns. As the coil moves through one pole pitch, its flux linkages change to

$\lambda_2 = -N_c\Phi$ (it now links the flux of opposite polarity)

During this movement, change of flux linkages of the coil is

$$\Delta\lambda = -2N_c\Phi \tag{7.3}$$

For a P-pole machine, the time of travel through one pole pitch is

$$\Delta t = \frac{2\pi}{P\omega_m} s \tag{7.4}$$

where ω_m is the armature speed in mechanical rad/s. Hence, the average coil emf induced is

$$E_c = -\frac{\Delta\lambda}{\Delta t} = \Phi\omega_m N_c P \tag{7.5}$$

Let C_p = coils/parallel path

Then the armature emf is

$$E_a = \frac{\Phi\omega_m (C_p N_c) P}{\pi}$$

But $C_p N_c = \dfrac{Z}{2A}$ = turns/parallel path

where Z is the total number of armature conductors.

Hence, $$E_a = \frac{\Phi \omega_m Z}{2\pi}\left(\frac{P}{A}\right) = K_a \Phi \omega_m \tag{7.6}$$

where $K_a = \dfrac{ZP}{2\pi A}$ = machine constant

Equation (7.6) can also be written as

$$E_a = \frac{\Phi n Z}{60}\left(\frac{P}{A}\right) = \frac{2\pi}{60} K_a \Phi n \tag{7.7}$$

where n is the armature speed in rpm.

7.4.2 Torque Equation

Average force on an armature conductor is

$$f_{\text{av}} = B_{\text{av}}\, l\, I_c \tag{7.8}$$

where l is the active conductor length, and I_c is the conductor current. Average torque on armature caused by one conductor is

$$t_{\text{av}} = B_{\text{av}}\, l\, I_c\, r \tag{7.9}$$

where r is the mean air-gap radius. Total torque developed by armature conductors is

$$T = B_{\text{av}}\, I_c l Z r \tag{7.10}$$

Now $$B_{\text{av}} = \frac{\Phi P}{2\pi r l} \tag{7.11}$$

Therefore,

$$T = \frac{1}{2\pi}\Phi I_c ZP$$

$$= \frac{1}{2\pi}\Phi I_a Z\left(\frac{P}{A}\right) \text{Nm} \tag{7.12}$$

$$= K_a \Phi I_a \text{ Nm} \tag{7.13}$$

Notice that K_a is the same constant in the emf Eq. (7.6) and torque Eq. (7.13).

7.4.3 Power Balance

Mechanical power

$$T\omega_m = K_a \Phi \omega_m I_a = E_a I_a \text{ W} \tag{7.14}$$

Observe that $E_a I_a$ is the electrical power converted to mechanical form and vice versa. From Eq. (7.14),

$$T = \frac{E_a I_a}{\omega_m} \text{ Nm} \tag{7.15}$$

The magnetic circuit of the machine is assumed linear because of the presence of the air gap whose reluctance is more that the reluctance of the iron path (see Example 7.1) under this assumption.

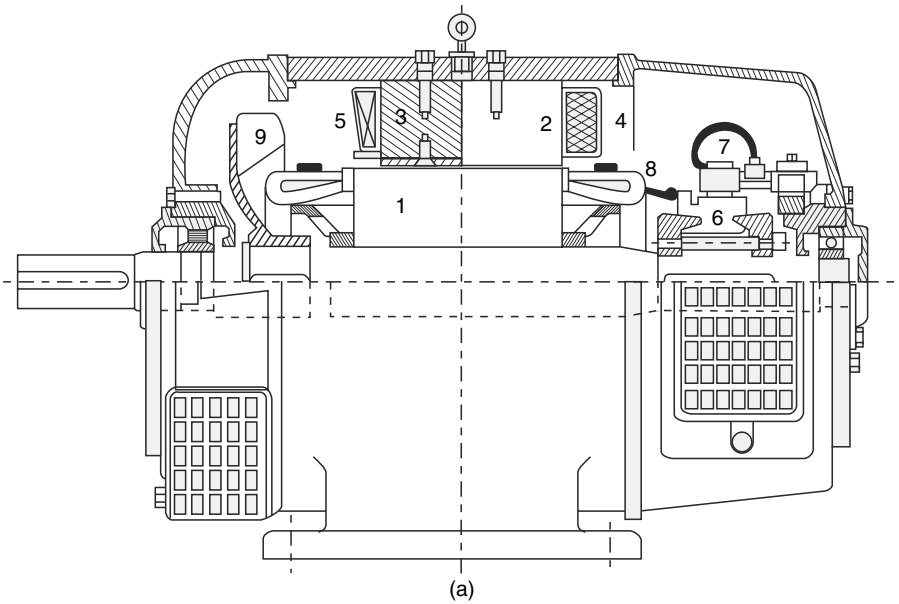
$$\Phi = K_f I_f \tag{7.16}$$

where I_f is the field current. Substituting in Eqs (7.6) and (7.13),

$$E_a = K_a K_f I_f \omega_m = K'_a K_f \omega_m \tag{7.17}$$

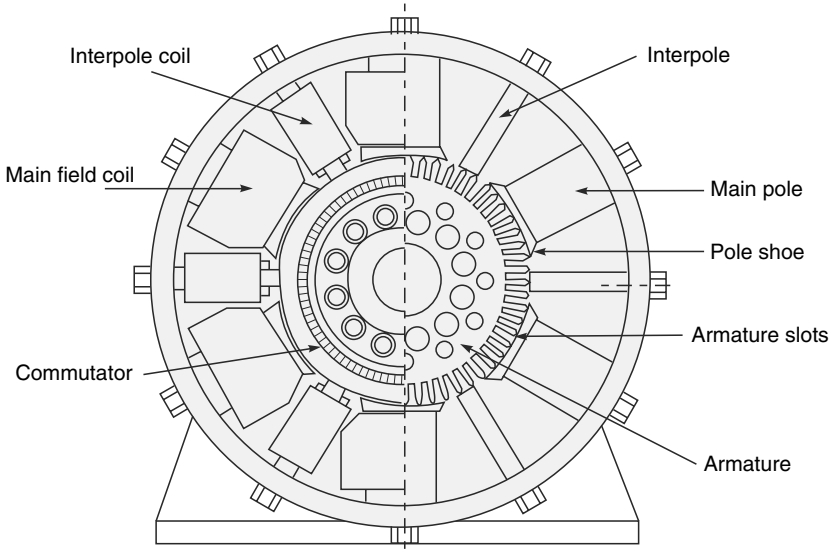
and $$T = K_a K_f I_f I_a = K'_a I_f I_a \tag{7.18}$$

where $K'_a = K_a K_f$



(a)

1. Armature core
2. Main field pole
3. Interpole
4. Main pole winding
5. Interpole winding
6. Commutator
7. Brush and brush holder
8. Armature winding overhang
9. Fan



(b)

Fig. 7.6 *(a) Longitudinal sectional view of a dc machine (b) Cross-sectional view of a dc machine*

Example 7.1

A 6-pole dc machine armature has 36 slots, 2 coil-sides/slot, 8 turns/coil and is wave wound. The pole-shoe is 18 cm long and the mean air-gap diameter is 25 cm. The average flux density over one/pole pitch is 0.8 T. Find the gross torque and mechanical power output when the machine is operating as a motor at 1200 rpm with an armature input current of 10 A.

Solution

$$Z = 36 \times 2 \times 8 = 576$$

$A = 2$ wave winding

$$\Phi = \frac{\pi \times 0.25}{6} \times 0.18 \times 0.8 = 0.0188 \text{ Wb}$$

Induced emf $$E_a = \frac{\Phi n Z}{60} \frac{P}{A}$$

$$= \frac{0.0188 \times 1200 \times 576}{60} \times \left(\frac{6}{2}\right)$$

$$= 650 \text{ V}$$

Gross mechanical power developed $= E_a I_a$

$$= \frac{650 \times 10}{1000} = 6.5 \text{ kW}$$

$$\text{Torque developed} = \frac{6.5 \times 1000}{\left(\frac{2\pi \times 1200}{60}\right)} = 51.72 \text{ Nm}$$

7.5 CIRCUIT MODEL

The circuit model of a dc machine is given in Fig. 7.7. The armature circuit has induced emf E_a and a series resistance of $R_a (= R_p/A$, where R_p is the resistance of a parallel path). The brush voltage drop is constant of the order of 2 V, which is either ignored or its effect included in R_a by linearising it. The field has a resistance R_f fed with field current $I_f (= V_f/R_f)$ and is shown at 90° to the brush axis (this angle is 90° electrical in an actual machine; Fig. 7.1). The field provides the per pole flux which induces the emf E_a in the armature when it runs at speed n. The power converted (mechanical to electrical or vice versa) is $E_a I_a$.

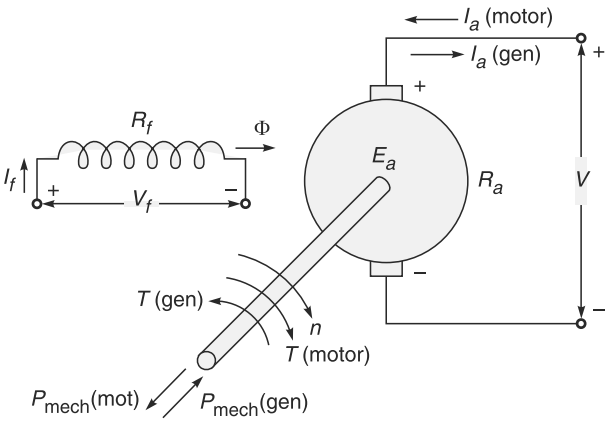


Fig. 7.7 *Circuit model of dc machine*

7.5.1 Generating Mode

I_a (armature current) flows in the direction of E_a as shown in Fig. 7.7. For the armature circuit,

$$V \text{ (terminal voltage)} = E_a - I_a R_a; \; E_a > V \tag{7.19}$$

$$P_{\text{mech}} \text{ (in net)} = E_a I_a \text{ (mechanical power converted to electrical form)} \quad (7.20a)$$

$$P_{\text{mech}} \text{ (in gross)} = E_a I_a + \text{rotational losses} \quad (7.20b)$$

where rotational losses = mechanical loss + core loss

$$P_0 \text{ (electrical output)} = E_a I_a - I^2{}_a R_a \text{ (armature copper loss)} \quad (7.20c)$$

7.5.2 Motoring Mode

I_a flows in the opposite direction to E_a as shown in Fig. 7.7. E_a in a motor is therefore known as *back emf*. For the armature circuit,

$$V \text{ (terminal voltage)} = E_a + I_a R_a;\ V > E_a \quad (7.21)$$

$$P_i \text{ (electrical input)} = VI_a \quad (7.22a)$$

$E_a I_a$ (electrical power converted to mechanical form)

$$= VI_a - I^2{}_a R_a \text{ (armature copper loss)} \quad (7.22b)$$

$$P_{\text{mech}}(\text{out gross}) = E_a I_a \quad (7.23a)$$

or $$P_{\text{mech}}(\text{out net}) = E_a I_a - \text{rotational losses} \quad (7.23b)$$

The dc Machine Ratings

- ❑ **Generator** Output in kW, terminal voltage and prime mover speed.
- ❑ **Motor** Output in kW, terminal voltage and speed at full-load.

Example 7.2

A 215 V dc machine has an armature resistance of 0.4 Ω. It is supplying 5 kW as a generator when run at 1000 rpm and is excited to give a terminal voltage of 215 W. At what speed would it run as a motor if it is fed at the same terminal voltage, draws the same armature current, but the flux/pole is increased by 10%?

Solution As generator,

$$I_a = \frac{5 \times 1000}{215} = 23.26\,\text{A}$$

$$E_{ag} = 215 + 0.4 \times 23.26 = 224.3\ \text{V}$$

or $$224.3 = K_a \Phi_g \times \left(\frac{2\pi \times 1000}{60}\right) \quad (i)$$

As motor $$E_{am} = 215 - 0.4 \times 23.26 = 205.7\ \text{V}$$

or $$205.7 = K_a \Phi_m \times \left(\frac{2\pi n}{60}\right) \quad (ii)$$

Dividing Eq. (ii) by Eq. (i),

$$\left(\frac{\Phi_m}{\Phi_g}\right)\left(\frac{n}{1000}\right) = \frac{205.7}{224.3}$$

$$n(\text{motor}) = \frac{205.7}{224.3} \times \frac{1}{1.1} \times 1000$$
$$= 834 \text{ rpm}$$

Example 7.3

A 200 kW, 400 V, separately excited dc motor runs at 600 rpm. It has 864 lap-connected conductors. The full load armature copper loss is 8 kW. Calculate the useful flux/pole.

Solution Figure 7.8 shows the connection diagram of the motor. It is assumed that 200 kW is the armature input at full load.

$$I_a = \frac{200 \times 1000}{400} = 500 \text{ A}$$

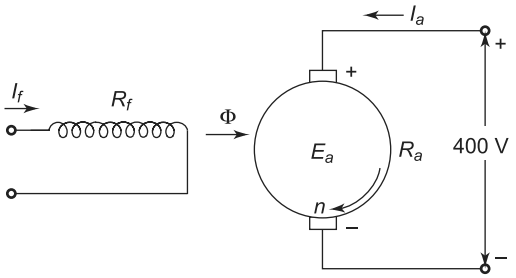


Fig. 7.8

Full load copper loss

$$I_a^2 R_a = 8 \text{ kW}$$

$$R_a = \frac{8 \times 1000}{(500)^2} = 0.032\ \Omega$$

$$E_a = V - I_a R_a$$
$$= 400 - 500 \times 0.032 = 384 \text{ V}$$

But $$E_a = \frac{\Phi n Z}{60}\left(\frac{P}{A}\right); \frac{P}{A} = 1 \text{ for lap-connected armature}$$

or $$384 = \frac{\Phi \times 600 \times 864}{60}$$

or $$\Phi = 0.044 \text{ Wb}$$

7.6 ARMATURE REACTION

When the dc machine armature carries current, it causes its own mmf distribution known as armature reaction. Figure 7.9 shows the cross-sectional view of a 2-pole machine. All the conductors under the north pole carry current in one direction and those under the south pole in the opposite direction. As the armature rotates, this pattern of current distribution remains fixed in space (i.e. stationary w.r.t the main poles as is necessary for torque production. In Fig. 7.9, the conductors 1, 1′, 2, 2′, etc. form a coil with peak ampere-turns AT_a, whose axis is along the brush axis (d-axis) or at 90° elect to the main pole axis (d-axis), independent of the armature rotation. As many conductors move out of the influence of one pole, the same number moves in. Therefore, the conductor current pattern is fixed in space and so the AT_a axis is stationary along the q-axis and the direction of AT_a is also fixed. Such an armature reaction is known as *cross-magnetising*.

It is seen from Fig. 7.9 that armature reaction AT opposes the main pole AT at one pole tip and strengthens it at the other pole tip (this is the cross-magnetising effect). The flux density wave in the air gap therefore gets distorted from the trapezoidal shape at no-load, $I_a = 0$ (Fig. 7.2), such that the flux density increases in one half of the main poles and decreases in the other half as shown in Fig. 7.7.

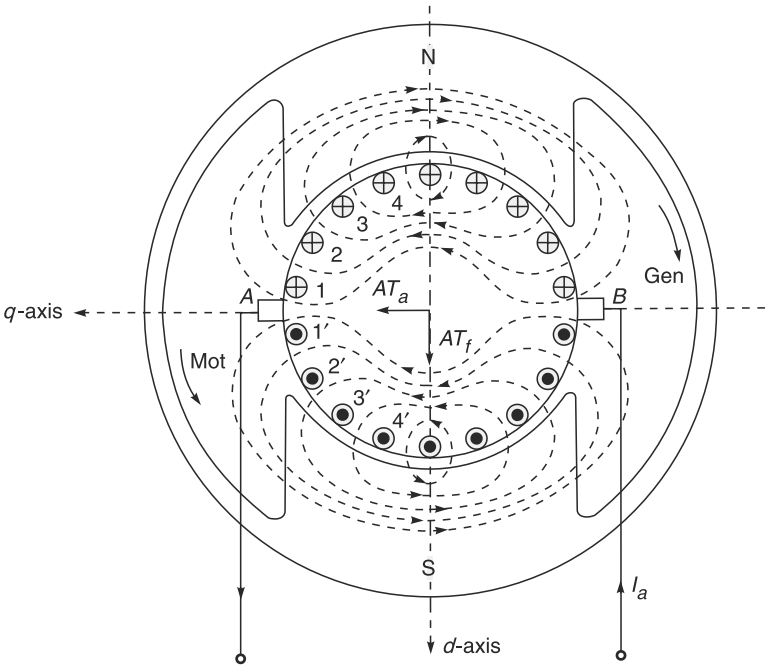


Fig. 7.9 *Armature reaction in a dc machine*

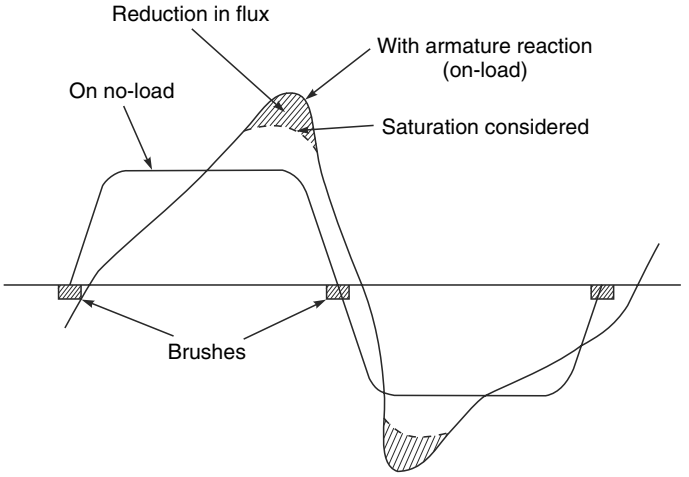


Fig. 7.10 *Distortion of B-wave in dc machine air gap*

The decrease in flux in one half of the pole is balanced by an equal increase in the other half so long as the magnetic material of the poles is in an unsaturate region. Thus in the linear region of magnetisation, the flux/pole remains unaffected by armature reaction even though the *B*-wave gets distorted. In the saturation region of magnetisation, the increase in flux in one-half of the pole is less than the decrease in the other resulting in net reduction in flux/pole.

Compensating Winding

Armature reaction varies with the armature current. In case of a sudden change in motor load, the armature reaction flux ϕ_a changes at a sharp rate. It induces large statically induced emfs in armature coils, which appear across commutator segments, causing these to flash over, resulting in complete short circuit of the machine commutator. Hence, AT_a must be compensated by compensating winding placed in slots cut out in the main pole shoes with windings axis along the q-axis. These windings have a few turns connected in series with armature such that these are excited by I_a. This is illustrated in Fig.7.11.

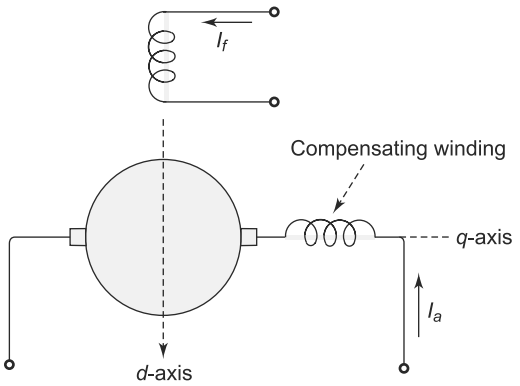


Fig. 7.11 *Connections of compensating winding*

7.7 COMMUTATION

When an armature coil moves under the influence of one pole-pair, it carries constant current in one direction. As the coil moves into the influence of the next pole-pair, the current in it must reverse (see Figs 7.4 and 7.5). This reversal of current in a coil is called *commutation*. Several coils (equal to number of poles in a lap winding) undergo commutation simultaneously. During the process of commutation, the coil-sides of the coil lie in the interpolar region and the coil is shorted by the brush (this can be easily observed from Fig. 7.4). The change in current is opposed by the reactance emf induced in the coil because of its leakage inductance (*Lenz's law*). As a result, the coil current does not reverse fully at the end of the commutation period when the coil has moved into the influence of the next pole-pair. The balance current then sparks across the brush. Continuous heavy sparking at the brushes damages the commutator severely, reducing its life span, apart from causing intense radio disturbance in the neighboring region.

To aid the process of commutation, speed emf (dynamically induced) is injected in the commutating coil to oppose the reactance emf. This speed emf must obviously be in the direction in which the current will flow in the coil after commutation. The speed emf is obtained by placing narrow *series-excited* poles in the interpolar region as shown in Fig. 7.12(a) so as to influence only the commutating coils. These poles are known as *interpoles* or *compoles*. In Fig. 7.12(a), the reader should verify "(by right-hand rule) that the direction of speed emf induced in the coil-sides of the commutating coils is in the appropriate direction with the polarity of interpoles indicated in the figure.

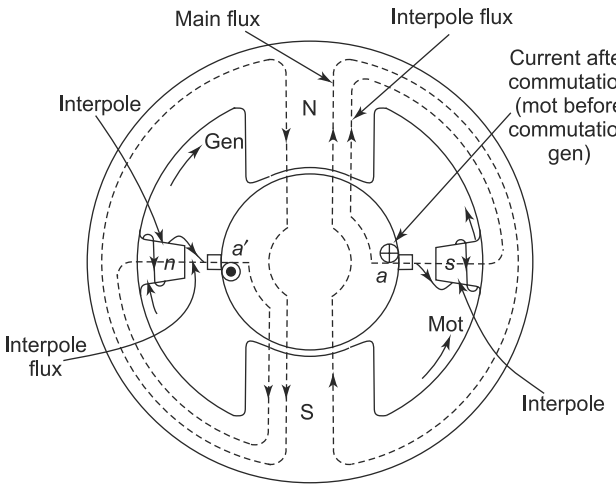


Fig. 7.12(a) *Interpoles in a dc machine*

7.8 METHODS OF EXCITATION AND MAGNETISATION CHARACTERISTICS

The field of a dc machine is excited by either of the following two methods or by a combination of these.

Voltage Excitation

The field winding has a large number of turns of thin wire and is excited from a voltage source (self or separate). The field resistance is therefore high and the field carries a small current. Such a field winding is known as *shunt field winding* illustrated in Fig. 7.12(b).

Current Excitation

The field is excited here by a few turns of thick wire (low resistance) connected in series with the armature. This is the series field windings also shown in Fig. 7.12(b). As it carries the armature current, the excitation varies with load.

A dc generator can be excited in the following two modes:

- *Separate excitation* (requiring a separate dc voltage source), and
- *Self-excitation* (excited from its own voltage/current).

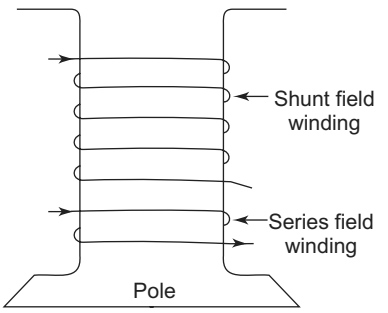


Fig. 7.12(b) *Shunt and series field*

7.8.1 Excitation Methods

The dc motors field windings can be excited in several ways.

❑ **Separate Excitation** The shunt-field winding is excited from an independent voltage source as in Fig. 7.13(a).

❑ **Shunt Excitation** The shunt-field winding is connected across the armature as in Fig. 7.13(b).

❑ **Series Excitation** The series-field winding is connected in series with the armature as in Fig. 7.13(c).

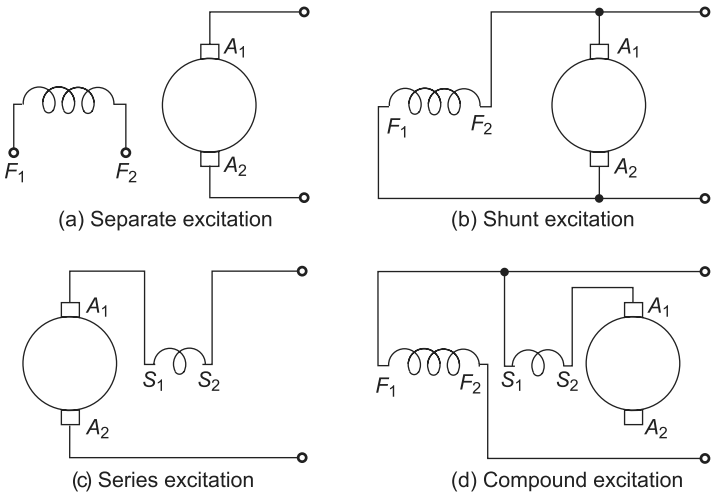


Fig. 7.13 *Excitation of dc machine*

❑ **Compound Excitation** Both shunt and series-field windings are connected in shunt across the armature and in series with the armature respectively as in Fig. 7.13(a).

The compound excitation could be *cummulative* with series field aiding the shunt field or *differential* with series field opposing the shunt field. The differential compound excitation is rarely used.

7.8.2 Magnetisation Characteristic

$\Phi - I_f$ or $E_a - I_f$ (since $E_a \propto \Phi$) as for a given machine speed is the magnetisation characteristic of the machine. It can be obtained by separately exciting the machine, as in Fig. 7.14(a), when the machine ran as a generator by a prime mover at a constant speed (rated speed) with open-circuited armature. Under this condition of operation, $E_a = V_{OC}$. That is why this is also called *Open-Circuited Characteristic* (*OCC*). The field current I_f is varied by means of a regulating resistance in series with the field. The readings of V_{OC} and I_f are recorded for plotting OCC. Note that R_f is the total resistance in the field circuit. A typical characteristic is exhibited in Fig. 7.14(b). In the initial linear part of the characteristic, the air-gap effect predominates and the dotted tangential line is called the *air-gap line*. At $I_f = 0$, the residual flux in the magnetic circuit causes a small induced voltage, viz. the residual voltage. At higher values of I_f, saturation effect in iron of the machine begins to show up. For economic reasons, the machine is normally operated in a slightly saturated state. As the machine speed is changed, every point on the magnetisation curve translates proportionally up or down as illustrated.

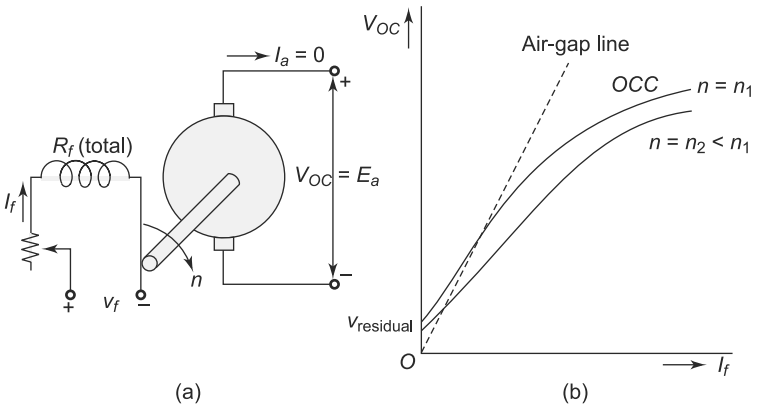


Fig. 7.14 *Open-circuit characteristic (OCC) of dc machine*

7.8.3 Self-Excited Generator (Shunt Generator)

In a shunt generator, the field is connected across the generator terminals with the generator running at fixed speed (rated speed) as shown in Fig. 7.15(a). At no-load ($I_L = 0$),

$$I_a = I_f \text{ (very small)} \tag{7.24}$$

$$\therefore V\text{(terminal voltage)} = E_a - I_f R_a \approx E_a \tag{7.25}$$

Thus, V–I_f is the magnetisation curve. For the field circuit

$$V = I_f R_f \ (R_f\text{-line}) \tag{7.26}$$

The no-load voltage (V_0) is thus given by the intersection of the magnetisation characteristic and the R_f line as shown in Fig. 7.15(b).

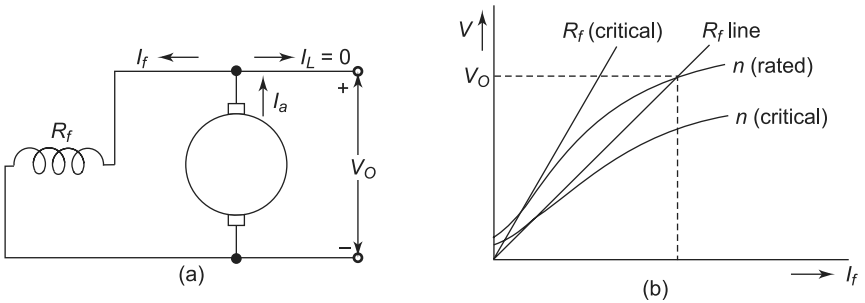


Fig. 7.15 *(a) Shunt generator on no-load (b) No-load voltage of shunt generator*

The value of R_f, when the R_f line is tangential to the magnetisation characteristic (same as the air-gap line) is called the *critical resistance*, R_{fc}. For field resistance more than this value, the no-load voltage of the shunt generator would be very small (close to residual value), which means that the generator fails to excite. For a given R_f, if the machine speed is reduced, the critical operation again visits. Such a speed (for a given R_f) is called the *critical speed*. It also easily follows that for a given speed, the no-load voltage (V_0) can be adjusted by variation of field resistance R_f by means of an external series resistance called the regulating resistance.

Example 7.4

The OCC data of a dc generator at 1800 rpm is given below:

$V_{OC}(V)$	8	40	74	112	152	213	234	248	266	278
$I_f(A)$	0	0.5	1.0	1.5	2.0	3.0	3.5	4.0	5.0	6.0

The field of the generator is shunt connected. Find

(a) the field resistance and the field current for a no-load voltage of 250 V,

(b) the value of the critical field resistance,

(c) the value of the critical speed, and

(d) the external resistance must be added in the field to reduce the terminal voltage to 220 V.

Solution The OCC is drawn in Fig. 7.16.

(a) Draw a line from the 250 V point on the OCC to origin. Reading from the figure,

$$I_f = 4.1 \text{ A}, R_f \frac{250}{4.1} = 61\ \Omega$$

(b) R_f (critical) is found by drawing a line from the origin such that is parallel to the nearly straight line part of OCC. R_f (critical) is the slope of this line which can be found by reading the co-ordinates of any point on the line. We choose the point P (150 V, 2 A). Therefore,

$$R_f(\text{critical}) = \frac{150}{2} = 75\ \Omega$$

(c) To find the critical speed for $R_f = 6\ \Omega$, we need to shift the OCC R_f(61 Ω) line is tangential to it. There is no need to draw the full characteristic. We draw a vertical line from P to locate P_1 on the R_f(61 Ω) line, point of downward shifted OCC. The speed change corresponds to voltage values of P and P_1.

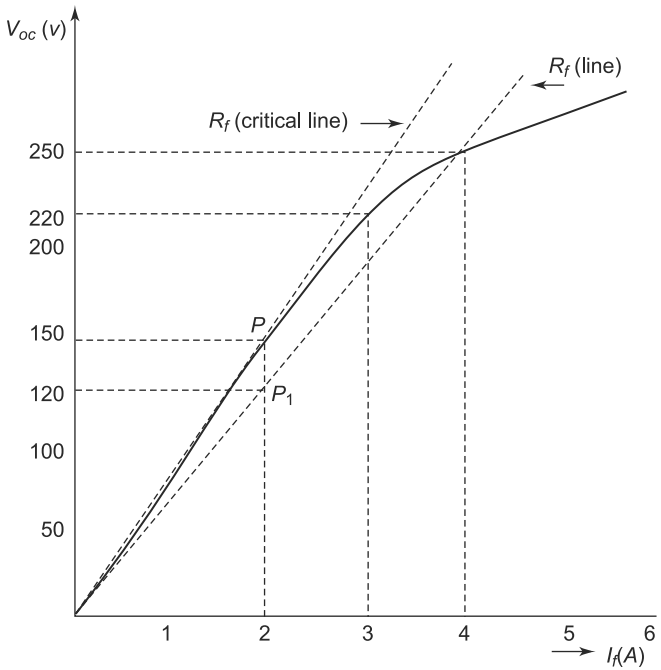


Fig. 7.16

The voltage corresponding to P_1 is 120 V
Therefore,

$$N_{\text{critical}} = 1800 \times \frac{120}{150} = 1440\,\text{rpm}$$

(d) From the figure,

$$R_f(V_0 = 220) = \frac{220}{3.2} = 68.8\ \Omega$$

External resistance to be added = 68.8 – 61 = 7.8 Ω

7.9 CHARACTERISTICS OF dc MOTORS AND SPEED CONTROL

The emf and torque equations of a dc machine are reproduced below:

$$E_a = \frac{\Phi n Z}{60}\left(\frac{P}{A}\right) = K_E \Phi n \tag{7.27}$$

$$T = \frac{1}{2\pi}\Phi I_a Z\left(\frac{P}{A}\right) = K_T \Phi I_a \tag{7.28}$$

Equation (7.27) can be written in the form

$$n = K_N \frac{E_a}{\Phi};\ K_N = \frac{1}{K_E} \tag{7.29}$$

Of course K_N and K_T are related ($K_N K_T = 60/2\ \pi$).

7.9.1 Shunt Motor

Figure 7.17 shows the connections of a dc shunt motor run from a source of voltage V. The per pole flux Φ is governed by the field current I_f by means of the regulating resistance R_r. For the armature circuit,

$$E_a = V - I_a R_a \tag{7.30}$$

Substituting in Eq. (7.29),

$$n = K_N \left(\frac{V - I_a R_a}{\Phi} \right) \tag{7.31}$$

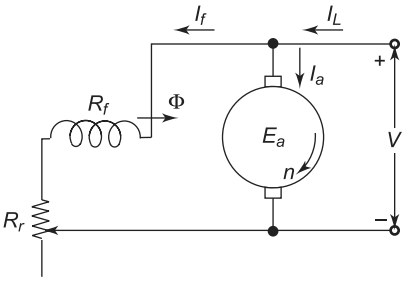


Fig. 7.17 *dc shunt motor*

Substituting I_a from the torque Eq. (7.28) in Eq. (7.31), the motor speed can be expressed as

$$n = \frac{K_N V}{\Phi} - \left(\frac{K_n R_a}{K_T \Phi^2} \right) T \tag{7.32}$$

At no load[1] ($T = 0$),

$$n = n_0 = \frac{K_N V}{\Phi} \tag{7.33}$$

Hence,

$$n = n_0 - \left(\frac{K_N R_a}{K_T \Phi^2} \right) T \tag{7.34}$$

For a given field current (Φ fixed), as per Eq. (7.34), the speed-torque characteristic of a shunt motor is linear and the speed drops from the no-load value as the load torque is increased. The speed drop is small (only a few percent) as shown in Fig. 7.18 because R_a is small (0.01 pu or less); this is the *shunt characteristic*. The torque cannot be allowed to exceed a certain limit (full load or rated value) laid down by the permissible armature current (Eq. (7.28)). The actual motor speed-torque characteristic will exhibit a slight nonlinearity (bends upwards) because of reduction in flux caused by armature reaction in presence of saturation (ignored in the above analysis).

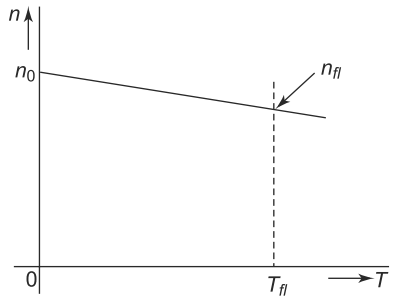


Fig. 7.18 *Speed-torque characteristic of shunt motor (for a fixed current)*

7.9.2 Speed Control

As per Eq. (7.32), the speed of a shunt motor for a given torque load can be controlled by

- control of Φ by adjusting I_f, V constant, called *field control*,
- control of V, the armature voltage, I_f constant, called *armature control*, and
- control of R_a by an adjustable resistance included in the armature circuit. This is used only for small motors as it reduces the motor efficiency because of loss in the resistance added.

7.9.3 Field Control

The armature voltage is held constant while the field current and therefore the flux/pole is controlled by the regulating resistance R_r in the field circuit, as shown in Fig. 7.17. The no-load speed increases inversely

[1] Under practical no-load condition the motor has to develop a small torque T_0 to overcome its own windage and friction torque.

with Φ (or I_f) as per Eq. (7.33). The speed-torque characteristic at each no-load speed (given field current) is linear but its slope increases as Φ is reduced (Eq. (7.32)). Three characteristics at different no-load speeds are drawn in Fig. 7.19. As R_r is fully cut out, no-load speed lower than this value is not feasible.

As the field is weakened, the maximum torque to which the motor can be loaded for rated armature current reduces proportionally (Eq. (7.28)). This torque limit is indicated in dotted line in Fig. 7.19. This is *constant kW (or hp) drive* wherein torque load must reduce as the speed is increased.

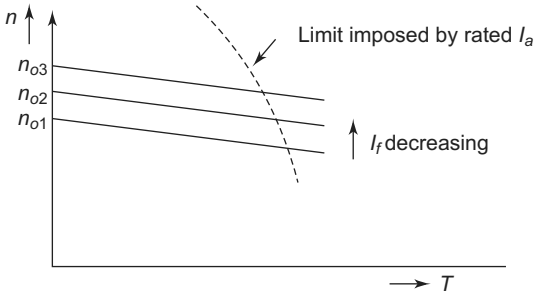


Fig. 7.19 *Field control of shunt-motor speed (armature voltage constant)*

Armature Control

The field current I_f is held constant at maximum value (V/R_f). The no-load speed varies directly as the armature voltage as per Eq. (7.33). At a given armature voltage, the speed drops slightly as the load torque is increased. The speed-torque characteristics moves up or down parallel to itself as per Eqs (7.33) and (7.34) as the armature voltage is varied, as shown in Fig. 7.20. At rated current, the torque capability is T_{fl} at any armature voltage. Thus, armature control is constant-torque drive.

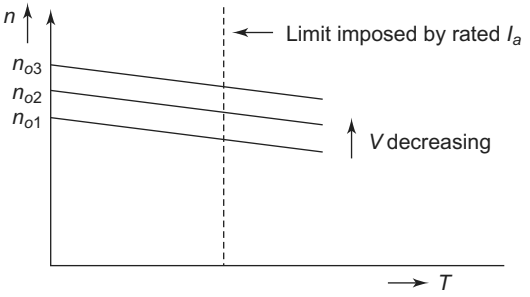


Fig. 7.20 *Armature control of shunt-motor speed (field current constant)*

Armature and Field Control

By varying armature voltage with maximum field current, the motor is increased with constant-torque capability. Having reached the rated voltage, the speed can increase further by reducing the field current but with decreasing torque capability, i.e. constant kW drive. In fact, with this arrangement the range of speed control can be made as wide as 1:6.

The armature voltage control requires a variable voltage source with full rated current capability; a high power source to match the motor rating. The field control requires an independent voltage source but with small current capability; a low power source.

Ward-Leonard Speed Control

This is the scheme, which provides the arrangement of armature and field control. An earlier used scheme is presented in Fig. 7.21. It employs an ac motor–dc motor generator set, matching the dc motor rating for feeding variable voltage current to the motor. A small dc generator called the *exciter* is coupled to the motor; generator feeds field current to the dc generator field and dc motor field. As the field requires low power, the two field currents are controlled by potentiometers. The dc generator field current provides control over armature voltage.

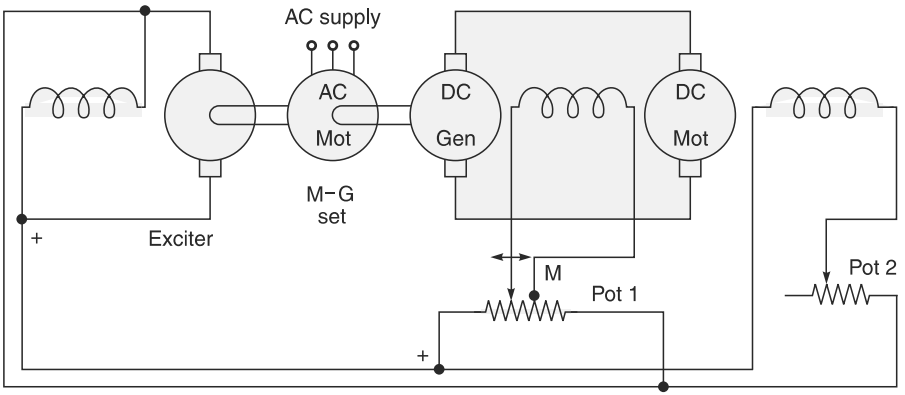


Fig. 7.21 *Ward-Leonard speed control system*

With the availability of electronic power devices, the MG set has been superseded by high power Silicon Controlled Rectifier (SCR) and the exciter by a fixed-voltage rectifier. The modern scheme is drawn in Fig. 7.22 (a). Its constant-torque and constant-kW regions are identified in Fig. 7.22(b).

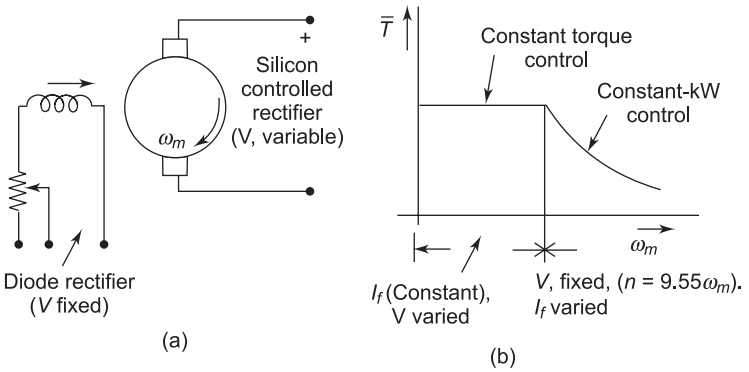


Fig. 7.22 *Ward-Leonard control of a dc shunt motor*

Example 7.5

A 4-pole, 230 V dc shunt motor has 888 wave-connected conductors. It draws a field current of 0.6 A to give a no-load flux of 5.4 mWb. The armature resistance is 0.8 Ω. Calculate the motor speed at a no-load current of 2 A. What would be the motor current (line) and speed when it develops a torque of 29.6 Nm? What is the speed regulation from no-load to this torque?

Solution Refer Fig. 7.17.

At no-load,

$$I_L = 2 \text{ A}$$

$$I_f = 0.6 \text{ A}$$

$$\therefore \quad I_a = 2 - 0.6 = 1.4 \text{ A}$$

$$E_a = 230 - 1.4 \times 0.8 = 229 \text{ V}$$

But $$E_a = \frac{\Phi n Z}{60}\left(\frac{P}{A}\right)$$

or $$n = n_0 = 1430 \text{ rpm}$$

At load,

Torque developed

$$T = 29.6 \text{ Nm}$$

$$T = \frac{1}{2\pi}\Phi I_a Z\left(\frac{P}{A}\right)$$

Substituting values,

$$29.6 = \frac{1}{2\pi} \times 5.4 \times 10^{-3} \times I_a \times 888 \times \left(\frac{4}{2}\right)$$

or $$I_a = 19.4 \text{ A}$$

$$I_L = 19.4 + 0.6 = 20 \text{ A}$$

$$E_a = 230 - 0.8 \times 19.4 = 214.5 \text{ V}$$

Substituting values,

$$214.5 = \frac{5.4 \times 10^{-3} \times n \times 888}{60} \times \left(\frac{4}{2}\right)$$

or $n = 1340$ rpm

$$\text{Speed regulation} = \frac{1430 - 1340}{1430} \times 100 = 6.3\%$$

Example 7.6

A 230 V dc shunt motor has an armature resistance of 0.1 Ω, and a shunt field resistance of 275 Ω. It runs at speed of 1000 rpm when drawing an armature current of 75 A. Calculate the additional resistance to be inserted in the field circuit to raise the motor speed to 1200 rpm at an armature current of 125 A. Assume linear magnetisation characteristic.

Solution

At $$n_1 = 1000 \text{ rpm}$$

$$E_{a1} = 230 - 75 \times 0.1 = 222.5 \text{ V}$$

$$I_f = \frac{230}{275} \quad 0.837 \text{ A}$$

Since the magnetisation characteristic is linear, Eq. (7.27) can be written as

$$E_a = K'_E I_f n \qquad \text{(i)}$$

Substituting values,

$$222.5 = K'_E \times 0.837 \times 1000 \quad \text{(ii)}$$

At $n_2 = 1200$ rpm

$$E_{a2} = 230 - 125 \times 0.1 = 217.5 \text{ V}$$

Substituting in Eq. (i),

$$217.5 = K'_E \times I_{f2} \times 1200 \quad \text{(iii)}$$

Dividing Eq. (iii) by Eq. (ii),

$$\frac{1200\, I_{f2}}{0.837 \times 1000} = \frac{271.5}{222.5}$$

or $I_{f2} = 0.681$ A

$$R_{f2} = \frac{230}{0.681} = 338\ \Omega$$

$$R_f, \text{ ext} = 338 - 275 = 63\ \Omega$$

Example 7.7

A 115 V dc-shunt motor, draws an armature current of 25 A when running at 1450 rpm at full-load torque. Motor armature circuit resistance is 0.3 Ω.

Calculate the resistance to be added in series with motor armature to reduce the speed to 1200 rpm at 3/4th full-load torque. Calculate the armature circuit efficiency also.

What would be the motor speed as 1/2 full load-torque when the resistance as calculated above is included in the armature circuit?

Solution *At full-load torque*, speed $n_1 = 1450$ rpm

$$I_{a1} = 25 \text{ A}$$

$$E_{a1} = 115 - 25 \times 0.3 = 107.5 \text{ V}$$

$$E_a = K_E \Phi n = K'_E n; \Phi = \text{constant, field is not changed} \quad \text{(i)}$$

$$T = K_T \Phi I = K'_T I_a \quad \text{(ii)}$$

or $$107.5 = K'_E \times 1450 \quad \text{(iii)}$$

$$T = K'_T \times 25 \quad \text{(iv)}$$

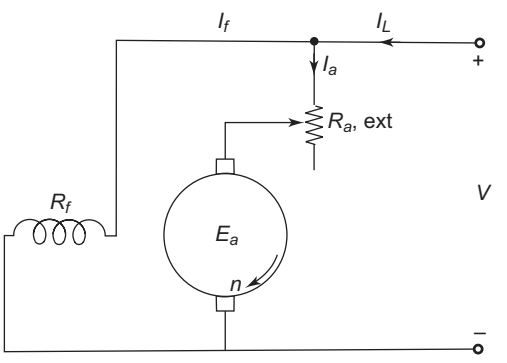


Fig. 7.23

At 3/4th full load, $n_2 = 1200$ rpm (external resistance added in armature circuit (Fig. 7.23),

$$E_{a2} = K'_E \times 1200 \quad \text{(v)}$$

From Eqs (iii) and (v),

$$E_{a2} = 107.5 \times \frac{1200}{1450} = 89 \text{ V}$$

Also $$\frac{3}{4} T = K'_T I_{a2} \quad \text{(vi)}$$

From Eqs (iv) and (vi),

$$I_{a2} = \frac{3}{4} \times 25 = 18.75 \text{ A}$$

From KVL equation of the armature circuit

$$89 = 115 - 18.75(0.3 + R_{a,\text{ext}})$$

or $$R_{a,\text{ext}} = 1.09\ \Omega$$

Armature circuit efficiency, $\eta_a = \dfrac{E_a I_a}{V I_a}$

$$= \frac{89}{115} \times 100 = 82.5\%$$

Thus, 17.5% of the power fed to the armature circuit is dissipated in the external resistance (1.09 Ω) and the armature resistance (0.3 Ω).

If instead, armature circuit is fed from a rectifier with voltage

$$V = 89 + 18.75 \times 0.3 = 94.63 \text{ V}$$

Then armature efficiency would be

$$\eta_a = \frac{89}{94.63} \times 100 = 94\%$$

The method of adding series resistance is only employed for very small (fractional kW) motors. It can be used for larger motors to reduce speed for short time periods only.

Example 7.8

An 8 kW, 230 V dc-shunt motor has an armature resistance of 0.5 Ω. It runs at a speed of 1200 rpm on no-load. At what speed would the motor run when delivering a gross mechanical power of 8 kW (i.e. inclusive of rotational loss)? Also, calculate the armature current and the torque developed. Assume that the field current is maintained constant.

At what speed would the motor run when coupled to a centrifugal pump which requires a torque of

$T_p = 0.6 \times 10^{-4}\, n^2$ Nm (n = speed in rpm),

inclusive of torque of rotational losses of the motor?

***Note*:** At no-load, the armature current would be so small that the armature voltage drop can be ignored.

Solution *At no-load*,

$$E_a \approx V = 230 \text{ V}$$

Since field current is to be maintained constant,

$$230 = K\Phi n = K'_E \times 1200$$

or $$K'_E = 0.1917 \qquad \text{(i)}$$

At load

$$E_a I_a = 8000 \text{ W} \qquad \text{(ii)}$$

Also, $$I_a = \left(\frac{230 - E_a}{0.5}\right) \qquad \text{(iii)}$$

Substituting Eq. (iii) in Eq. (ii),

$$E_a(230 - E_a) = 4000$$

or $$E^2_a - 230\,E_a + 4000 = 0 \quad \text{(iv)}$$

Solving

$$E_a = 211 \text{ V} \quad \text{or} \quad 19 \text{ V}$$

We reject $E_a = 19$ V as it would mean top large I_a $(230 - 19)/0.5 = 422$ A) well beyond the rated current of the motor (= 8000/230 = 34.8 A).

Now $$211 = K'_E \times n$$

or $$n = \frac{211}{0.1917} = 1100 \text{ rpm}$$

Also $$T = \frac{8000}{\left(\frac{2\pi \times 1100}{60}\right)} = 69.4 \text{ Nm}$$

$$I_a = \frac{230 - 211}{0.5} = 38 \text{ A}$$

But $$T = K' I_a$$

or $$69.4 = K'_T \times 38$$

or $$K'_T = \frac{69.6}{38} = 1.826 \quad \text{(vii)}$$

Pump Load

$$T = 1.826 \times \left(\frac{230 - 0.1917n}{0.5}\right)$$

or $$T = 840 - 0.7\,n \quad \text{(viii)}$$

Pump load torque

$$T_p = 0.6 \times 10^{-4}\, n^2 \quad \text{(ix)}$$

At steady speed,

$$T = T_p$$

or $$840 - 0.7n = 0.6 \times 10^{-4}\, n^2$$

$$0.6 \times 10^{-4}\, n^2 + 0.7\,n - 840 = 0 \quad \text{(x)}$$

Solving

$$n = 1097 \text{ rpm}$$

Example 7.9

A separately excited dc motor is operating at an armature voltage of 300 V. Its no-load speed is 1200 rpm. When fully loaded, it delivers a motor torque of 350 Nm and its speed drops to 1100 rpm. What is the full-load current and power? What is the armature resistance of the motor?

The motor is now fed with armature voltage of 600 V, while its excitation is held fixed as before. It is once again fully loaded. Find the motor torque, power and speed.

Solution *At no-load*

At no-load, the armature draws a very small current to develop mechanical to supply only its rotational loss. Therefore, armature voltage drop $I_{ao}\,R_a$ is of negligible order. Thus,

$$E_a \approx V = 300 \text{ V}$$

and $$300 = (K_a \Phi)\frac{2\pi\, 1200}{60};\ \text{Eq. (7.6)}$$

or $K_a\Phi = 2.39$ (remains constant as excitation does not change)

Motor loaded to 350 Nm

$$350 = (Ka\ \Phi)I_a;\ \text{Eq (7.13)}$$

or $$I_a = \frac{350}{2.39} = 146.4 \text{ A (full load)}$$

$$E_a = 300 \times \frac{1100}{1200} = 275 \text{ V}$$

Mechanical power developed

$$= E_a I_a = 275 \times 146.7$$
$$= 40.3 \text{ kW}$$

$$R_a = \frac{300 - 275}{146.4} = 0.171\ \Omega$$

Armature voltage of 600 V

At full load[2] $I_a = 146.4$ A

$T = 350$ Nm (field excitation has not changed)

$$E_a = 600 - 146.4 \times 0.171 = 575 \text{ V}$$

$$575 = 2.39 \times \left(\frac{2\pi \times n}{600}\right)$$

or $n = 2297$ rpm

$$\text{Power} = E_a I_a = 575 \times 146.4$$
$$= 84.2 \text{ kW}$$

Observe that while motor speed has more than doubled, torque has remained the same and power has more than doubled.

Example 7.10

For the motor of Example 7.9, the armature voltage is held fixed at 300 V while its current is reduced to one half. Calculate the full-load torque, power and speed.

Solution As the field excitation is reduced to one half,

$$K_a\Phi = \frac{2.39}{2} = 1.195$$

But $I_a = 146.4$ A (full load)

$$E_a = 300 - 146.4 \times 0.171 = 275 \text{ V (as before)}$$

$$275 = 1.195 \times \frac{2\pi \times n}{60}$$

or $n = 2200$ rpm

[2] The motor could be loaded to somewhat higher current because of enhanced cooling at higher speed.

Power developed $= E_a I_a = 275 \times 146.7$
$= 40.3$ kW

Torque $T = K_a \Phi I_a$
$= 1.195 \times 146.4 = 175$ Nm

Observe that while motor speed has doubled, torque is reduced to one half but power is the same.

7.9.4 Series Motor

In this kind of motor, the field is series excited by the armature current as shown in Fig. 7.24. From speed Eq. (7.29),

$$n = K_N \left[\frac{V - I_a(R_a + R_{se})}{\Phi} \right] \tag{7.35}$$

Assuming linear magnetisaton,

$$\Phi = K_{se} I_a \tag{7.36}$$

From Eq. (7.28),

$$T = K_T K_{se} I_a^2 \tag{7.37}$$

Substituting for I_a from Eq. (7.37) in Eq. (7.35),

$$n = \frac{K_N}{K_{se}} \left[\frac{V\sqrt{K_T K_{se}}}{\sqrt{T}} - (R_a + R_{se}) \right] \tag{7.38}$$

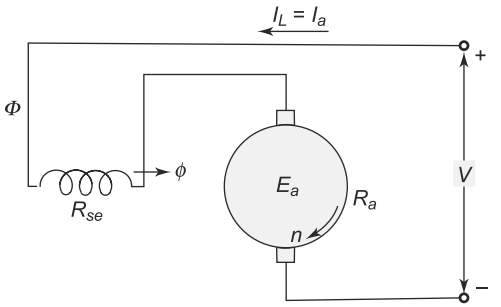


Fig. 7.24 *dc series motor*

As $(R_a + R_{sc})$ is very small and it may be ignored.
Thus,

$$n \approx \frac{K_N V}{\sqrt{T K_{se}}} \tag{7.39}$$

It is inverse hyperpole-type speed-torque characteristic as sketched in Fig. 7.25, with speed reducing as load torque increases. It is ideal for *traction-type* load. As the load torque is reduced, the motor speed rises sharply and will acquire dangerously high speed as the motor reaches no-load condition. *So the series motor must never be allowed to run at no-load even inadvertently*. This cannot happen in traction-type load as the load is always present.

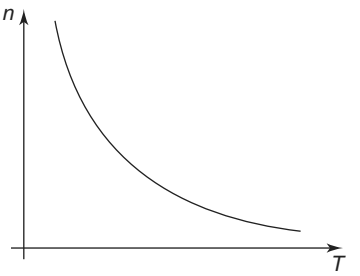


Fig. 7.25 *Speed-torque characteristic of series motor*

Speed control in dc series motors is achieved as given below:

Field Control [K_{se} Varies as in Eq. (7.38)]

This is achieved by two means:

- *Tapped-field Control:* The connection diagram is illustrated in Fig. 7.26. As the field turns are reduced by means of tap-changing gear, K_{se} [Eq. (7.36)] reduces causing the speed to go up for a given torque as shown in Fig. 7.27.
- *Series-parallel Field Control:* The field coils are divided in two equal halves and are connected in series/parallel as shown in Fig. 7.28. It is seen from this figure that the series connection corresponds to N_{se} turns (low speed) and the parallel connection is equivalent to $N_{se}/2$ turns (high speed). Only two speeds are possible in this method which is commonly employed in traction.

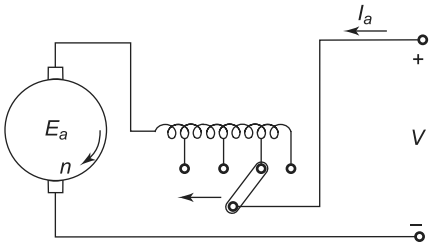


Fig. 7.26 *Tapped field control (connection diagram)*

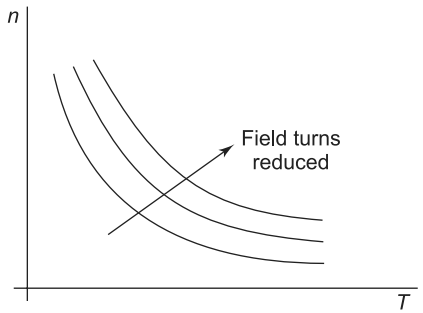


Fig. 7.27 *Tapped field speed control of dc series motor*

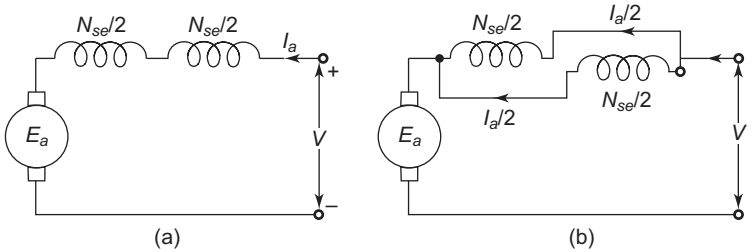


Fig. 7.28 *Series-parallel field control of dc series motor*

Armature Control

This is obtained by series/parallel connection of two identical series motors (Fig. 7.29) which are mechanically coupled. The parallel connection with voltage V across each armature gives double the speed compared to the series connection with voltage $V/2$ across each armature.

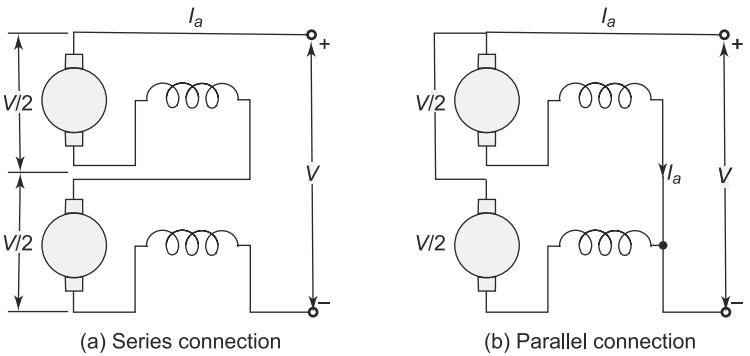


Fig. 7.29 *Series-parallel speed control of series motors; case of constant load torque is illustrated*

7.9.5 Compound Motor

It has both shunt and series fields as shown in Fig. 7.30. If the series field is connected to aid the shunt field, the motor is called *cumulative compound* and if it opposes the shunt field, it is called *differential compound*.

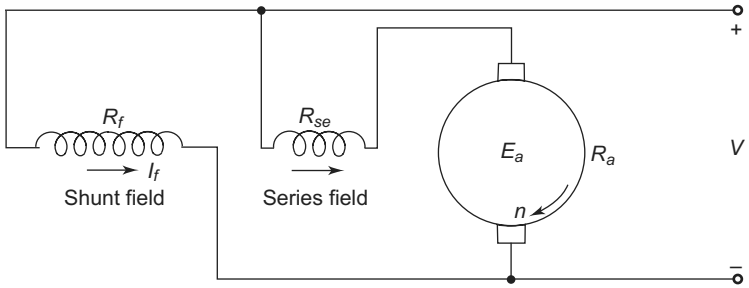


Fig. 7.30 *Compound motor*

At no-load, series field carries only a small no-load current and as a consequence, the no-load speed is determined by the shunt field (Fig. 7.31). As the load increases, the series field current (= armature current) causes the flux/pole to increase in a cumulative compound motor so that its speed drops much more sharply than in a shunt motor as shown in Fig. 7.31. On the other hand, in a differential compound motor, the opposing series field reduces the flux/pole causing the motor speed to increase as shown in Fig. 7.31. It can be arranged that full-load speed equals no-load speed (*called level compounding*): At heavy loads (overloads), the flux/pole decreases sharply and speed rises to dangerous values while the armature draws a very large current to meet the torque demand. Because of this serious drawback, a differential compound motor is not recommended for practical use.

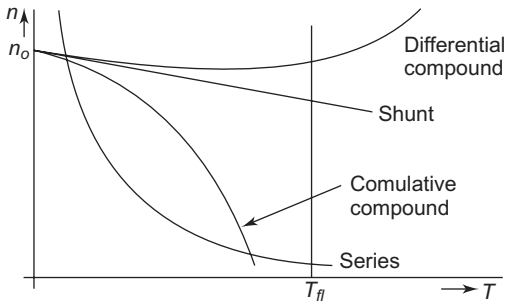


Fig. 7.31 *Speed-torque characteristics of dc motors*

A cumulative compound motor is preferred for rolling mills. Unlike a series motor, it has a finite no-load speed but speed drops sharply (similar to series motor) relieving the peak power drawn from the mains as the billet is passed through rolls.

Figure 7.31 is also illustrative of speed-torque characteristics of various types of dc motors.

Example 7.11

A dc series motor runs at 500 rpm drawing 40 A from 600 V mains. Determine the value of the resistance to be added in series with the armature for the motor to run at 450 rpm; the load torque is reduced in the square ratio of speed. Assume linear magnetisation.

Given: $(R_a + R_{se}) = 0.5\ \Omega$

Solution Without additional resistance in armature circuit ($n = 500$ rpm)

$$E_a = 600 - 40 \times 0.5 = 580 \text{ V}$$

$$580 = K_a \Phi \omega_m = K'_a I_a \omega_m \; ; \; \Phi \propto I_a \text{ in series motor} \tag{i}$$

or
$$K'_a = \frac{580}{40 \times \left(\frac{2\pi \times 500}{60} \right)} = 0.277$$

$$T = K_a \Phi I_a = K'_a I_2^2$$

$$= 0.277 \times (40)^2 = 443.2 \text{ Nm} \tag{ii}$$

With additional resistance in armature circuit (n = 450 rpm),

$$T = 443.2 \times \left(\frac{450}{500} \right)^2 = 359 \text{ Nm}$$

$$I_a = \left(\frac{359}{0.277} \right)^{1/2} = 36 \text{ A}$$

$$E_a = 0.277 \times 36 \times \left(\frac{2\pi \times 450}{60} \right) = 470 \text{ V}$$

$$R \text{ (total)} = \left(\frac{600 - 470}{36} \right) = 3.6 \; \Omega$$

$$R_{\text{ext}} = 3.6 - 0.5 = 3.1 \; \Omega$$

Example 7.12

A 220 V dc series motor has an armature resistance of 1 Ω and series field winding resistance of 0.4 Ω. On a certain load, the motor input current is 20 A. It is desired to reduce the speed of the motor by 30%. Calculate the resistance to be connected in series if the load torque varies as cube of the speed. Assume that the load torque includes the effect of mechanical loss of the motor. The magnetic circuit is unsaturated.

Solution Motor speed n_1, I_a = 20 A;

$$T = K_T \Phi I_a = K'_T I_a^2; \Phi_a \propto I_a$$

$$T_L = K_L n^3$$

$$K_L n_1^3 = K'_T I_{a1}^2 = 400 K'_T \tag{i}$$

$$K_L (0.7 n_1)^3 = I_{a2}^2 K'_T \tag{ii}$$

Dividing Eq. (ii) by (i),

$$(0.7)^3 = \frac{I_{a2}^2}{400}$$

or
$$I_{a2} = [400 \times (0.7)^3]^{1/2} = 11.7 \text{ A}$$

$$E_{a1} = 220 - 20 \; (1 + 0.4) = 192 \text{ V}$$

$$E_a = K_E \Phi n = K'_E I_a n; \Phi \propto I_a$$

$$192 = K'_E \times 20 n_1 \quad \text{(iii)}$$

$$E_{a2} = K'_E \times 11.7 \times 0.7 n_1 \quad \text{(iv)}$$

From Eqs (iii) and (iv),

$$\frac{E_{a2}}{192} = \frac{11.7 \times 0.7}{20}$$

or $E_{a2} = 78.6$ V

Additional resistance to be added in armature circuit

$$= \frac{220 - 78.6}{11.7} = -1.4 = 7.78\ \Omega$$

Example 7.13

A dc series motor runs at 1000 rpm drawing 25 A from a 250 V supply with its field halves connected in series. At what speed would it run if the field halves are reconnected in parallel? Also, calculate the armature current. Assume (a) load torque to be proportional to square of speed, and (b) voltage drop of armature resistance, and field resistance to be negligible.

Solution Assumption (a) $E_a \approx V = 250$, whatever may be the armature current.

Field halves connected in series (Fig. 7.26(a))

$$E_a = K_a \Phi \omega_m$$

$$\Phi = K_f N_{se} I_a$$

$$\therefore \quad E_a = (K_a N_f I_{se}) I_a \omega_m$$

or $$250 = (K_a N_f N_{se}) \times 25 \times \frac{2\pi \times 1000}{160}$$

or $K_a N_f N_{se} = 0.0955$

Now T(developed) $= K_a \Phi I_a^2 = (K_a K_f N_{se}) I_a^2$

$= 0.0955 \times (25)^2 = 59.7$ Nm

Field halves connected in parallel (Fig. 7.26(b)). We now have the relationship as

$$\Phi = \left(\frac{K_f N_{se}}{2}\right) I_a$$

$$E_a = \left(\frac{K_a K_f N_{se}}{2}\right) I_a \omega$$

$$T(\text{developed}) = \left(\frac{K_a K_f N_{se}}{2}\right) I_a^2$$

where I_a Φ, ω and T (developed) are new values

At new ω

But load torque $T_L = 59.7 \times \left(\frac{\omega}{\frac{2\pi \times 1000}{60}}\right) = 59.7 \times \left(\frac{\omega}{104.7}\right)^2$

Now $$250 = \frac{0.0955}{2} I_a \omega \quad \text{(i)}$$

Equating motor and load torques,

$$59.7 \times \left(\frac{\omega}{104.7}\right)^2 = \left(\frac{0.0955}{2}\right) I^2 a \quad \text{(ii)}$$

or $$\omega = \left[\frac{0.0955 \times (104.7)^2}{59.7 \times 2}\right]^{1/2} I_a$$

$$= 2.96\, I_a$$

Substituting in Eq. (i),

$$250 = \frac{0.0955}{2} \times 2.96 \times I_a^2$$

or $$I_a = 42 \text{ A}$$

$$\omega = 2.96 \times 42 = 124.5 \text{ rad/s}$$

or $$n = \frac{124.5 \times 60}{2\pi} = 1189 \text{ rpm}$$

7.10 dc MOTOR STARTING

At the time of starting the motor, back emf being zero, the motor draws an armature current of

$$I_a(\text{start}) = \frac{V}{R_a} \text{ or } \frac{V}{R_a + R_{se}} \text{ (series motor)} \quad (7.40)$$

Since the motor armature resistance may be as low as 0.01 pu (for large motors), it may draw 100 times its rated current at start. Such large currents in the motor can have serious consequences as follows:

- Heavy sparking and commutator damage,
- Sudden large starting torque will give a severe jolt to the motor shaft, and
- Such large current (even through for a short time) is not permitted to be drawn from the source of supply whose voltage would otherwise dip sharply.

To limit the starting current to 1.5–2 times the rated current (this is necessary for quick acceleration), an external resistance has to be included in the armature circuit as shown in Fig. 7.32 for a shunt motor. This resistance is cut out in suitable time and resistance steps as the motor accelerates. These steps are so devised that peak current at each cut out remains limited to the prescribed value. To obtain high starting torque, full field current must be permitted to flow (no external resistance in field circuit) when the motor is started. Direct start, when permissible, does offer the advantage of quick acceleration and low ohmic loss per start—saving in energy and reduced temperature rise for frequent-starting situations.

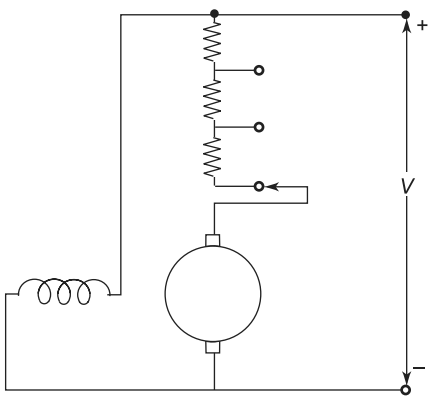


Fig. 7.32

7.11 EFFICIENCY OF dc MOTORS

Figure 7.33 shows the flow of power in a dc motor. The various losses are as follows:

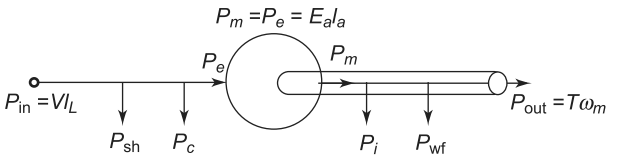


Fig. 7.33 *Power flow in a dc motor*

Constant Loss

P_i = core loss (including stray load core loss)
P_{wf} = windage and friction loss (at specified speed)
P_{sh} = shunt field copper loss (in a shunt machine)
$P_k = P_i + P_{wf} + P_{sh}$ = total constant loss

Variable Loss

$$P_C = I^2_a R_a$$

= Copper loss (inclusive of copper loss in series winding in a series motor and also inclusive of stray-load copper loss)

Total motor loss,

$$P_L = P_k + P_c$$

$$P_m = P_e = E_a I_a$$

The motor efficiency is given by

$$\eta = \frac{\text{Input} - \text{Losses}}{\text{Input}}$$

$$= \frac{VI_L - P_k - I^2_a R_a}{VI_L} \tag{7.41}$$

Under load, $I_L \approx I_a$; I_f is small in a shunt motor.
Then

$$\eta = 1 - \frac{1}{V}\left(\frac{P_k}{I_a} + I_a R_a\right) \tag{7.42}$$

The maximum motor efficiency occurs at

$$\frac{P_k}{I_a} = I_a R_a \tag{7.43}$$

or $$I^2_a R_a = P_k$$

or Variable loss = constant loss

which is the same condition as was shown in a transformer.

Example 7.14

A 50 kW, 230 V dc slums motor takes a current of 14.5 A when running light at 1640 rpm. The armature and field resistance are 0.15 Ω, and 120 Ω respectively. Estimate the motor efficiency when the motor is drawing 215 A. What would be the maximum efficiency of the motor and the load current at which it would occur?

Solution Refer Fig. 7.15.

$$I_f = \frac{230}{120} = 1.92 \text{ A}$$

$$P_{\text{sh}} = \frac{(230)^2}{120} = 441 \text{ W}$$

At no-load

$$P_{\text{in}} = 14.5 \times 230 = 3335 \text{ W}$$

$$I_a = 14.5 - 1.92 = 12.6 \text{ A}$$

$$I_a^2 R_a = (12.6)^2 \times 0.15 = 24 \text{ W} \quad \text{(negligible)}$$

$$P_k = P_i + P_{\text{wf}} + P_{\text{sh}} = 3335 - 24 \approx 3311 \text{ W}$$

On load

$$I_a = 215 - 1.92 = 213 \text{ A}$$

$$I_a^2 R_a = (213)^2 \times 0.15 = 6805 \text{ W}$$

$$P_L = 6805 + 3311 = 7.116 \text{ kW}$$

$$P_{\text{in}} = 230 \times 215 = 49.45 \text{ kW}$$

$$\eta = \frac{49.45 - 10.116}{49.45} = 79.54\%$$

For maximum efficiency,

$$0.15 I_a^2 = 3311$$

or

$$I_a = 148.6 \text{ A}$$

$$I_l = 148.6 + 1.92 \approx 150 \text{ A}$$

$$P_L = 2 \times 3311 = 6622 \text{ W}$$

$$P_{\text{in}} = 230 \times 150 = 34.5 \text{ kW}$$

$$\eta = \frac{34.5 - 6.62}{34.5} = 80.8\%$$

Three-point Starter

The connection diagram of a three-point shunt motor starter is shown in Fig. 7.34. The starter terminals to be connected to the motor are *A* (armature), *F* (field) and *L* (line). The starting resistance *n* steps between conducting raised studs. As the starting handle is rotated about its fulcrum, it is one stud to the next, one resistance step is cut out, and it gets added to the field circuit. There is a short time wait at each stud for the motor to build up speed. This arrangement ensures a high average starting torque.

At start, the handle is brought to stud one. The line voltage gets applied to the armature with full starting resistances in series with armature and to the field with NVC in series. Thus, the motor starts with maximum pick-up speed; the handle is moved from the stud to the 'ON' position shown in Fig. 7.34. The starting resistance has been fully cut out and is now included in the field circuit; being small it makes little difference in the field current. The resistance of NVC is small and forms part of the field resistance. The voltage across the armature is the line voltage. The handle is held in this position by the electromagnet excited current flowing through NVC.

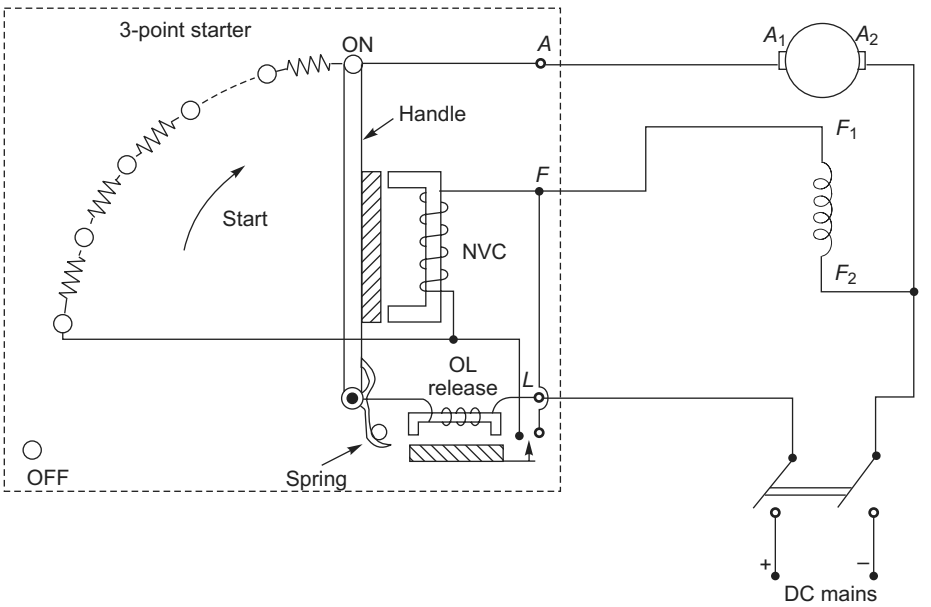


Fig. 7.34 *The dc shunt motor three-point starter (manual)*

Two protections are incorporated in the starter.

❑ **NVC (No Volt Coil)** In case of failure of field current (due to accidental or otherwise open circuiting), this coil releases the handle (held electromagnetically), which goes back to the OFF portion under the spring action.

❑ **OL (Overload) Release** The contact of their relay at armature current above a certain value (Overload short circuit) closes the NVC ends, again bringing the handle to OFF position.

7.12 CHARACTERISTICS OF dc GENERATORS

With the advent of silicon-controlled rectifiers, the importance of the dc machine as a generator has considerably reduced as SCRs can be employed to draw ac power from standard ac supply and convert it to dc. Also, the dc voltage can also be varied with ease. For the sake of completeness the characteristics of dc generators will be briefly discussed here.

The load characteristic of a dc generator at a particular speed is the relationship between its terminal voltage and load current (line current) and is also termed the *external characteristic*. The *internal characteristic* is the plot between the generated emf and load current.

7.12.1 Separately Excited dc Generator

Figure 7.35 is that of a separately excited dc generator. The operation considered here assumes that the armature is driven at constant speed (by means of prime mover) and the field excitation (I_f) is adjusted to give rated voltage at no-load and is then held constant at this value throughout the operation considered. The armature circuit is governed by the equation

$$V = E_a - I_a R_a;\ I_a = I_L \tag{7.44}$$

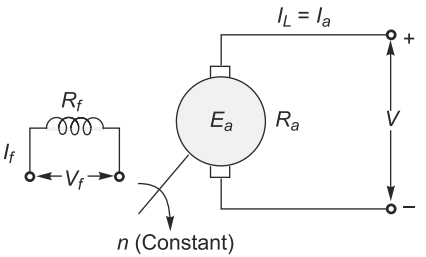


Fig. 7.35 *Separately excited dc generator*

In spite of fixed excitation, E_a drops off with load owing to the demagnetising effect of the armature reaction. As the voltage drop is caused by magnetic saturation effect, it increases with load nonlinearity. The *internal characteristic* (E_a–I_L) is also shown in Fig. 7.36. The external characteristic differs from the internal by the armature voltage drop I_aR_a which is also shown in Fig. 7.36.

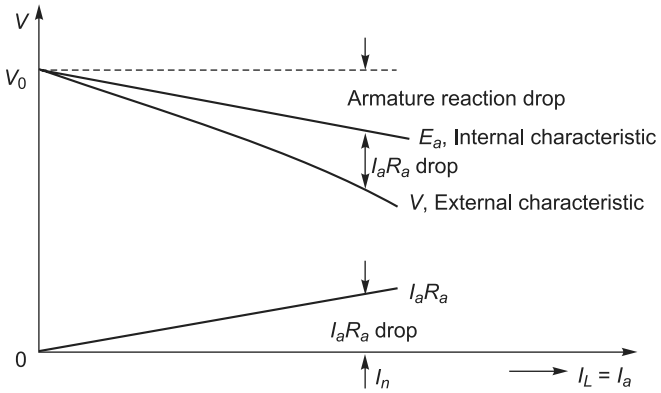


Fig. 7.36 *Characteristics of a separately excited generator*

7.12.2 Voltage Regulation

The voltage regulation of a generator (independent of the kind of excitation employed) is defined as

$$\%\ \text{regulation} = \frac{V_0 - (V_{\text{fl}} = V_{\text{rated}})}{V_{\text{rated}}} \tag{7.45}$$

where V_{fl} = full-load voltage = V_{rated}
V_0 = no-load voltage corresponding to rated voltage at full-load excitation remaining unchanged[3]

7.12.3 Shunt Generator

Short Circuit

A dc shunt generator is a self-excited generator. Figure 7.37 shows a shunt-connected generator. With field resistance adjusted to a certain value by means of the regulating resistance, the desired no-load voltage

[3] In case a shunt field winding is provided, it would mean that the total resistance in a field circuit remains unchanged in the operation.

can be obtained. The external characteristic of the generator can then be obtained by a load test with total field resistance remaining fixed in the process. The terminal voltage drops off much more rapidly with load in a shunt generator than in a separately excited generator because of fall in field current with terminal voltage. The *external characteristic* is a double-valued curve with a certain I_L (max) as shown in solid line in Fig. 7.38. As indicated in Fig. 7.38, the useful parts of the external characteristic is much before the turning point. Internal characteristic is obtained from the external characteristic by adding I_aR_a. At any point P (V_1, I_{L1}) we find

$$I_{a1} = I_{L1} + (V_1/R_f)$$

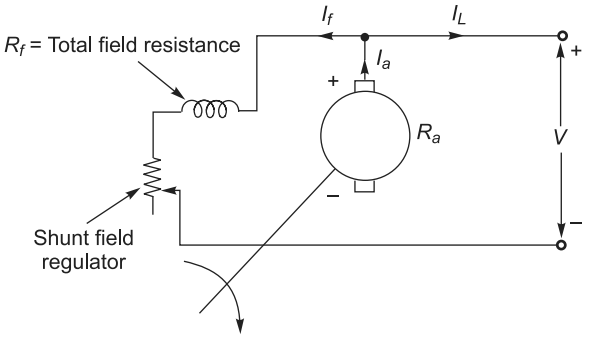


Fig. 7.37 *dc shunt generator on load*

This locates the corresponding point on the internal characteristic shown by dotted curve in Fig. 7.38.

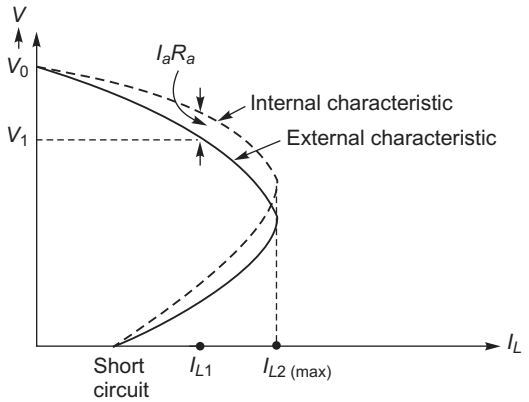


Fig. 7.38 *External characteristic of dc shunt generator*

7.12.4 Compound Generator

The causes of voltage drop in the terminal voltage from no-load to full-load in a shunt generator can be partially/fully/over compensated by use of an aiding series field (cumulative compound), which can be connected in a long or short-shunt (long-shunt shown in Fig. 7.39). The aiding ampere-turns of the series field automatically increase with the load, compensating the armature voltage drop. In a level-compound generator, full-load voltage equals no-load voltage. Steady-state volt-ampere (*V-I*) characteristics of a compound generator are shown in Fig. 7.40. Differential compounding is not used in practice as the terminal voltage falls off steeply with load. Long or short-shunt connection of series winding makes only a marginal

difference in the *V-I* characteristic of a compound generator. Compounding level can be adjusted by a diverter in parallel to the series field.

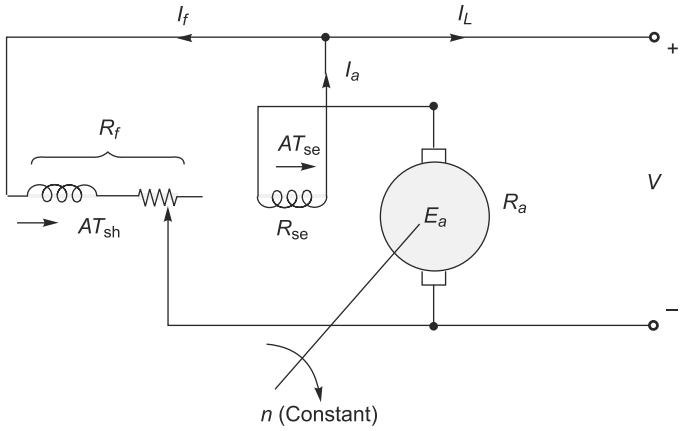


Fig. 7.39 *Compound generator (long-shunt)*

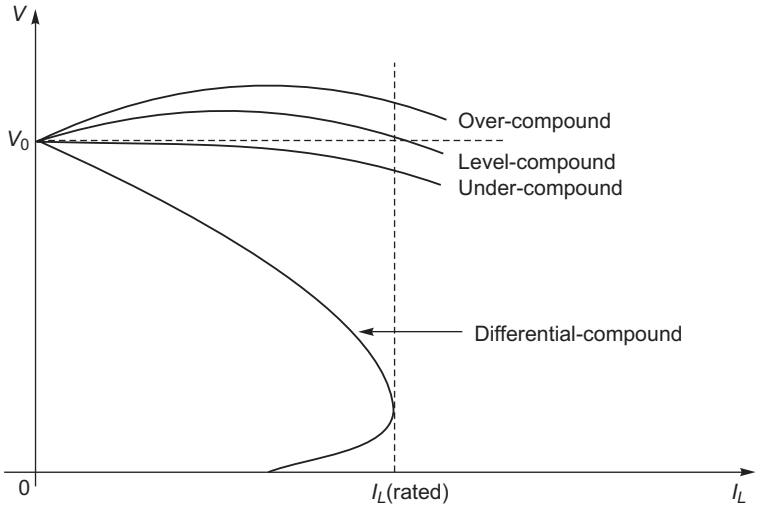


Fig. 7.40 *External characteristics of a compound generator*

7.13 dc MOTOR APPLICATIONS

A dc *motor* in spite of its high cost as compared to an induction motor is still competitive in applications requiring control speed as its speed can be varied over a wide range by (i) field control, (ii) armature control, or (iii) a combination of the two.

The dc motors have high starting torque compared to induction motor; hence, there is faster load deceleration.

Shunt Motor

Medium starting torque; speed regulation 5–15%.
Application: centrifugal pumps, conveyors, machine tools, printing presses, etc.

Series Motor

High torque at low speed and low torque at high speed; high starting torque (as much as 5 T (*fl*)); good speed control possible.
Application: traction, hoists, crane, battery-powered vehicles, etc.

Compound Motors

Differentially compound motor is ideally suited for pulsating loads (needing flywheel action).
Application: Rolling mill, etc

Example 7.15

A dc series motor operates at 800 rpm with a line current of 120 A from a 250 V mains. Determine the motor speed at a current of 60 A at 250 V assuming that the flux/pole at 60 A is 70% of its value at 120 A.

Given: R_a = 0.15 Ω, R_{se} = 0.1 Ω

Solution

$$R_a + R_{se} = 0.15 + 0.1 = 0.25\ \Omega$$

250 V, 120 A, 800 rpm operation

$$E_{a1} = 250 - 120 \times 0.25 = 220\ \text{V}$$

$$E_{a1} \propto \phi_1 \times n$$

or
$$220 \propto 800\ \phi_1 \quad \text{(i)}$$

250 V, 60 A, n_2 operation

$$E_{a2} = 250 - 60 \times 0.25 = 235\ \text{V}$$

$$\phi_2 = 0.7\ \phi_1$$

$\therefore$
$$235 \propto n_2 \times 0.7\ \phi_1 \quad \text{(ii)}$$

Dividing Eq. (ii) by Eq. (i), we get

$$0.7n_2/800 = 235/220$$

or
$$n_2 = 1221\ \text{rpm}$$

Example 7.16

A 220 V dc series motor yielded the following operational data:

Speed (rpm)	640	475	400
Current (A)	20	30	40

Find the speed at which the motor will run when connected to a 200 V mains with a series resistance of 2 Ω while drawing 35 A. Armature circuit resistance =1.2 Ω.

Solution

$$E_a = 220 - I_a(R_a + R_{sc})$$

$R_a + R_{sc} = 1.2\ \Omega$ gives

Then

$$E_a = 220 - 1.2\ I_a$$

We prepare the table as below from the given data:

Speed (n)	640	475	400	rpm
Current (I_o)	20	30	40	A
1.2 I_a	24	36	48	V
E_a	196	134	172	V

As E_a–n relationship is nonlinear, we find E_a and n at $I_a = 35$ A linear interpolation

$$E_a(35A) = 184 - (184 - 172) \times \frac{5}{2} = 178 \text{ V}$$

$$n(35\text{A}) = 475 - (475 - 400) \times \frac{5}{10} = 437.5 \text{ rpm}$$

At 200 V with added resistance of 2 Ω, 35 A

$$E_o = 200 - 35(1.2 + 2) = 88 \text{ V}$$

In a dc machine,

$$E_a = K_a \Phi\ \omega_m = K_a \Phi n,\ \Phi \propto I_a$$

As I_a is same in both cases

$$E_a \propto n$$

Therefore,

$$n\ (200\text{ V}, 35\text{A}) = 437.5 \times \frac{88}{178} = 216.3 \text{ rpm}$$

Example 7.17

A dc shunt motor rated 50 kW connected to a 250 V supply is loaded as to draw 200 A when running at a speed of 1250 rpm. Given: $R_a = 0.22\ \Omega$

(a) Determine the load torque if the rotational loss (including iron loss) is 600 W.

(b) Determine the motor efficiency if the shunt field resistance is 125 Ω.

Solution

(a)
$$E_a = 250 - 200 \times 0.22 = 206 \text{ V}$$

$$E_a I_a = P_m(\text{dev.}) = 206 \times 200 = 412 \text{ kW}$$

Rotational loss = 0.6 kW

$$P_m(\text{out}) = 41.2 - 0.6 = 40.6 \text{ kW}$$

$$\omega_m = (2\pi \times 1250)/60 = 130.9 \text{ rad/s}$$

$$T_L = \frac{40.6 \times 103}{130.9} = 310 \text{ Nm}$$

(b) Shunt field loss

$$= (250)^2/125 = 500 \text{ W}$$

$$P_e \text{ (in)} = 250 \times 200 + 500 = 50.5 \text{ kW}$$

$$\eta = [40.6/50.5] \times 100 = 80.3\%$$

Summary

➢ **Constructional features**
- Field poles on stator, always salient type with wide-pole shoe about 70% of pole pitch; field poles dc excited
- Armature in the rotor carries armature windings
- Commutator on the rotor, copper segments with mica insulation between adjoining segments.

➢ **Functions** Converts alternating armature current to dc, which is collected by brushes (carbon) suitably placed around the commutator.

➢ **Armature windings**

Lap winding

Number of parallel paths, $A = P$, poles
Number of brushes = $A = P$
Conductor current, $I_c = I_a/A$
where I_a is armature current.

Wave winding

Number of parallel paths, $A = 2$
Number of brushes = 2 needed but P used in practice
Conductor current, $I_c = I_a/2$

➢ **emf equation**

$$E_a = K_a \Phi \omega_m = \left(\frac{2\pi}{60}\right) K_a \Phi_n V$$

ω_m = rad (mech)/s, n = rpm, Φ = flux /pole

$K_a = \left(\frac{ZP}{2\pi A}\right)$, Z = number of armature conductors

For linear magnetisation, $\Phi \propto I_f$

$$E_a = K'_a I_f \omega_m, \omega_m = \left(\frac{2\pi}{60}\right) n$$

➢ **Torque equation**

$T = K_a \Phi I_a$ Nm; $K_a = \left(\frac{ZP}{2\pi A}\right)$ same as for emf

For linear magnetisation, $\Phi \propto I_f$

$$T = K'_a I_f I_a$$

➢ **Power converted**, $T \omega_m = E_a I_a$ W

➢ **Generating machine**
$V_{(terminal)} = E_a - I_a R_a$; R_a = armature resistance, very small, order 0.01 pu
$V_t < E_a$
I_a flows out of the + terminal of machine

➢ **Motoring machine**
$V_{(terminal)} = E_a + I_a R_a$
$V_t > E_a$
I_a flows into the + terminal of machine, in opposition to E_o, called *back emf*.

➢ **Machine axes**
d-axis, along the middle of field poles
q-axis, along the magnetic neutral
d and *q*-axis are at 90° (elect) to each other

➢ **Armature reaction**
AT_a at 90° (elect) to AT_f, cross magnetising
Flux density decreases at one pole end and increases at the other. In linear magnetization, no change in Φ, flux/pole. In saturation region of magnetisation, Φ reduces slightly.

➢ **Commutation**
As the armature coils move out of the influence of one pole pair to the next pole pair, the coil current must reverse, a process called commutation. Current reversal is opposed by coil reactance emf $\left(L\frac{di}{dt}\right)$.
If the current does not fully reverse, there is sparking at the brushes.
Remedy—Interpoles, narrow poles placed in the *inter-polar* region to inject speed emf to aid current reversal in the commutating coils

➢ **Excitation of the poles**
Shunt field winding—Large number of turns to carry small current (winding resistance high); voltage excited, in shunt across voltage source.
Series field winding—A few turns (small resistance), current excited in series with armature, so current flow is I_a.

➢ **Field winding excitation**
Separately excited from an independent voltage source
Shunt excited—In parallel with armature terminals
Series excited—In series with armature, current I_a
Compound excitation—Both shunt and series excitations are employed, could be *cumulative differential*
Shunt excitation can be controlled by a regulating resistance in series with shunt windings.

➢ **OCC**—open circuit characteristic. V_{oc} (= E_a) vs I_f at constant speed. The machine is run as a separately excited generator with the armature open circuited and field current varied OCC is indeed the magnetisation characteristic of the machine.

➢ **Critical field resistance (R_{fc}) for shunt generator** is the maximum field resistance above which the generator fails to excite.

➢ **Critical speed**—It is the minimum speed of a shunt generator with fixed field resistance below which the generator fails to excite.

➢ **Motor characteristics** depend upon the type of excitation. Accordingly, the motor types are shunt motor, series motor, compound motor cumulative compound and differential compound

➢ ***Shunt motor***
n-T characteristic

$n = K_N \frac{E_0}{\Phi} = K_N \frac{V - I_a R_a}{\Phi}$; no-load speed $n_0 = K_N \frac{V}{\Phi}$

At constant field current as load torque is increased, I_a increases and E_a reduces due to $I_a R_a$ drop and so the speed drops slightly from its no-load value (3-5% drop) This is the *shunt characteristic* where the speed is substantially constant.

➢ *Speed control* The speed is inversely proportional to excitation Φ (I_f) and directly proportional to $E_a \approx V_{(\text{applied voltage})}$.

➢ *Field control* I_f is reduced by a regulating resistance, the speed increases but torque reduces for rated current. This is constant kW drive.

➢ *Armature control* For fixed I_f, speed increases directly with applied armature voltage but torque in constant for rated current. This is the constant-torque drive.

➢ **Combination of armature and field control**
Keeping field current at maximum, the armature voltage is increased to raise the speed till the voltage limit is reached (*constant-T drive*). After that, the armature voltage is kept at the limit and I_f is reduced to raise the speed till the armature current limit (rated value) is reached (*constant-kW drive*). The speed range can be as wide as 1:6. This is the Ward-Leonard speed control.

➢ **Series motor**
The field winding is series connected and has very low resistance;
$I_a(R_a - R_{sc})$ drop can be ignored.
Therefore,

$$n \approx K_N \frac{V}{\Phi}, \Phi \propto I_a, T \Phi I_a^2$$

As the load torque increases, I_a increases and so Φ increases and the speed reduces.

At light load, the speed can reach dangerous value. The motor should not be switched on at no-load.

Ideal for traction type load

Speed control

Tapped field control—Field turns change

Series parallel field control—Winding is in two halves which can be connected in series or parallels. Parallel connection is equivalent to half the total number of winding turns, two speed operation.

Armature control—Two identical motors are mechanically coupled. The armatures can be connected in parallel (full voltage across each armature) or series (full voltage across each armature), two-speed operation.

Diverter control—A resistor is connected across the series field winding to reduce the winding current.

➢ **Compound motor**
Series field is provided along with the shunt field. It is cumulative compound if series field and the shunt field, and it is differential compound if it opposes the shunt field.

Cumulative compound No-load speed is controlled by the shunt field; at heavy load the speed drops shortly due to the series excitation.

Differential compound The series field by reducing flux keep the speed nearly constant till full load.

Beyond that at heavy overload, the series field causes the speed to increase to unacceptable levels. Not used in practice.

➢ **Motor starting**
At start ($n = 0$), there is no back emf ($E_a = 0$); the starting current on direct start is unacceptably high (may be 100 times the rated current). So resistance in series is connected, when starting the motor to limit the starting current to about twice the rated value. As the motor speeds up, the resistance is cut out in steps.

➢ **Motor efficiency**
Constant loss (P_k)—Core loss, windage and friction loss, shunt field loss (shunt motor)
Variable loss—Armature copper loss, $I_a^2 R_a$
At η_{max},
Variable loss = constant loss

$$I_a^2 R_a = P_k \text{ or } I_a = \sqrt{\frac{P_k}{R_a}}$$

➢ **Relationships to Remember (MUST)**

$$n \propto \frac{E_a}{\Phi} \quad T \propto \Phi I_a$$

If $\Phi \propto I_f$ (linear magnetisation)

$$n \propto \frac{E_a}{I_f} \quad T \propto I_f I_a, \quad T \propto I_a^2 \text{ (series motor)}$$

$$\omega_m = \left(\frac{2\pi}{60}\right) n$$

Approximation

On no-load $E_a \approx V$ (terminal)

This approximation may be used on load where less degrees of accuracy is acceptable.

Exercises

Review Questions

1. Why are the pole shoes made as large as 70% of pole pitch in a dc machine?
2. Comment on the statement "The armature conductor current is alternating but nonsinusoidal".
3. *Discuss*: The emf and torque of a dc machine depend on the flux/pole but are independent of the flux density distribution under the pole.
4. Write the expression for the induced emf and torque of a dc machine using standard symbols. What is the machine constant? What is the value of the constant relating to ω_m and n?
5. Explain the meaning and significance of the critical field resistance of a shunt generator.
6. To how many coil ends is each commutator segment connected?
7. The two ends of coil in lap windings are connected to which commutator segment? What is the commutator pitch?
8. Why is the armature reaction in a dc machine called cross magnetising? Can this affect the flux/pole?
9. What are interpoles, their purpose, location and excitation? Explain each item.
10. Compare the number of parallel paths in the lap and wave windings.
11. State the condition, which determines if a dc machine is generating or motor.
12. Write the expression relating the electrical power converted to the mechanical form in a dc motor. How are the electrical power input and mechanical power output different from these powers?

13. What is OCC and what information does it reveal about a dc machine? At what speed is it determined? What is the air-gap line?
14. Write the basic proportionality relationships of a dc machine. What form do these take for linear magnetisation?
15. State the types of dc motors. What is the basis of the classification?
16. Using emf and torque equation, explain how a dc motor has two powerful methods of speed control through field excitation and armature voltage.
17. Sketch the speed-torque characteristic of a shunt motor at fixed field current. Explain the characteristic through relevant fundamental relationships of the machine
18. Sketch the speed-torque characteristic of a dc series motor and advance the underlying reasoning for the nature of the characteristic based on fundamental relationships of the dc machine.
19. Explain through sketch and derivations the speed-torque characteristic of a differentially compound dc motor.
20. Advance the methods of varying the shunt field and the series field excitation of a dc machine.
21. Discuss the method of speed control of a dc series motor.
22. How is a shunt motor started? Why should it not be started direct on line?
23. Why do we need a compensating winding and how is this winding excited and why?
24. Enumerate and classify the losses in a dc shunt motor.
25. How can you determine the load current of a dc shunt motor at which the motor efficiency is maximum?

Problems

1. The generator of Example 7.5 is now run at 1600 rpm.
   (a) Find the no-load voltage and field current for a field resistance of 55 Ω.
   (b) Find the value of critical field resistance and the critical speed.
   (c) A load resistance of 0.8 Ω is connected across the generator terminals with the field resistance as in part (a). Find the generator terminal voltage and the load current.

   Given: Generator armature resistance = 0.5 Ω

   Hint: Solve iteratively.
2. A shunt generator delivers 50 kW at 250 V and 400 rpm. The armature and field resistances are 0.02 Ω and 50 Ω respectively. Calculate the speed of the machine running as shunt motor and taking 50 kW input at 250 V.
3. In a 100 kW, 600 V, 1200 rpm shunt motor, the field resistance is 500 Ω and the armature and brush resistance is 0.13 Ω. The efficiency of the motor at rated output and speed is 90%. Find (a) the line current, (b) the field current (c) induced emf, (d) mechanical power developed, and (e) torque developed.
4. The resistance of the armature of a 250 V, 20 kW, 1200 rpm dc shunt motor is 0.252 Ω. When running light, the motor takes 6.32 A at rated voltage; the field current is 0.92 A, while the speed is 1280 rpm. Determine (a) the speed when the motor takes 85 A with the field current remaining constant, and (b) the speed when the current is 60 A.
5. A constant-torque load is being supplied by a 500 V dc shunt motor, having armature and field resistances of 0.8 Ω and 300 Ω respectively. The motor takes a current of 28 A from the mains when running on load at 750 rpm. Find the value of the field resistance, which should be introduced in the field circuit to increase the speed to 1000 rpm. Find also the corresponding armature and line currents drawn by the motor. Assume linear magnetisation.
6. A dc shunt motor operating at 300 V has a no-load speed of 1200 rpm. The motor is now reconnected to 600 V mains and draws an armature current of 150 A. Calculate the motor speed. Assume linear magnetisation characteristic.

   Given: R_a = 0.2 Ω.
7. A 10 kW, 230 V dc shunt motor has armature resistance of 0.1 Ω. It runs at no load at a speed of 1500 rpm. When delivering a certain load, the motor draws an armature current of 200 A. Find the speed at which the motor will run at this load and the torque developed. Assume that the armature reaction on load causes a 4% reduction in the flux/pole compared to its no-load value.

8. A 250 V dc series motor has linear OCC with a slope of 12 V/field ampere at 1200 rpm.
   Find the speed at which the motor will run when developing a torque of 40 Nm. What current will it draw from the mains?
   Given: $R_a + R_{sc} = 0.6\ \Omega$
9. The armature and field resistances of a 25 kW, 250 V series motor are 0.12 Ω and 0.1 Ω respectively. The motor takes 85 A at a speed of 600 rpm. Find the motor speed when the motor takes (a) 100 A, and (b) 40 A. (c) What will be current taken by the motor when it runs at 800 rpm? Assume straight-line magnetisation characteristic.
10. The armature and field resistances of a 60 kW, 600 V series railway motor are 0.215 Ω and 0.08 Ω respectively. At rated voltage and at a current of 80 A, the speed is 750 rpm. Find the speed and torque developed when the current is 95 A. Assume linear magnetisation characteristic.
11. A 125 kW, 600 V dc series motor has $(R_a + R_{se}) = 0.15\ \Omega$. The full-load current at rated voltage and speed is 220 A. The magnetisation characteristic of the motor is assumed to be linear. It yielded an induced emf of 480 V at 600 rpm with a field current of 220 A.
    (a) Calculate the motor speed at full-load current and rated voltage. Also, calculate the full-load torque.
    (b) The starting current is restricted to 300 A. Calculate the external resistance to be added in the motor circuit and the starting torque.
12. In Problem 10, consider now that the motor has saturating-type magnetisation characteristic with two data points at 600 rpm given below:

emf(V)	450	518
If {A)	220	300

    Solve parts (a) and (b) once again.
13. Solve Example 7.14 assuming that the load torque remains constant as the field halves are reconnected in parallel.
14. A 500 V dc shunt motor when cold has a field resistance of 200 Ω and an armature resistance of 0.15 Ω. The motor runs at a no-load speed of 1000 rpm under cold conditions. After remaining continuously loaded at a load current of 70 A, field and armature temperatures rise to 40°C above the ambient temperature of 20°C. Calculate the motor speed under hot conditions. The temperature coefficient of copper = 1/234.5 per °C at 0°C.
15. A 220 V dc shunt motor has an armature resistance of 0.3 Ω and a field resistance of 200 Ω. The motor runs at 800 rpm with an armature current of 40 A. What resistance must be inserted in the field circuit to raise the motor speed to 1050 rpm; the load torque remaining constant? Assume linear magnetisation characteristic.
16. A dc shunt motor having an armature resistance of 0.2 ft takes 35 A from a 250 V supply and runs at 1500 rpm when driving (a) a load, the torque of which is proportional to the square of speed, and (b) a constant-torque load. Calculate in each case the resistance to be added to the armature circuit to reduce the speed to 1200 rpm. Compare the loss in the external resistance in the two cases. Assume 100% mechanical efficiency.
17. A 115 V dc shunt motor draws an armature current of 25 A when running at 1500 rpm at full load torque. Motor armature circuit resistance is 0.3 Ω.
    An additional resistance of 0.6 Ω is introduced in the armature circuit when the motor is operating at half full-load torque. Find the percentage change in the shunt field resistance, which would cause the motor to have a speed of 1400 rpm.
18. In Example 7.14, what should be the armature resistance of the motor for it to have maximum efficiency while drawing 215 A? Calculate the value of the maximum efficiency.
19. A 15 kW, 220 V, 1200 rpm, 4-pole dc shunt motor has 620 conductors connected as wave winding yielding an armature circuit resistance of 0.18 Ω. When delivering rated power at rated voltage and speed, it draws a line current of 79.8 A and a field current of 2.6 A. Calculate.
    (a) flux/pole,
    (b) developed torque,
    (c) rotational losses, and
    (d) total losses and efficiency.

Multiple-Choice Questions

1. The armature reaction mmf in a dc machine has a shape.
   (a) sinusoidal (b) trapezoidal
   (c) rectangular (d) triangular
2. A dc series motor has linear magnetisation and negligible armature resistance. The motor speed is
   (a) directly proportional to $\sqrt{T}$, T = load torque (b) inversely proportional to $\sqrt{T}$
   (c) directly proportional to T (d) inversely proportional to T
3. The power drawn by a dc shunt motor on no-load comprises
   (a) iron loss only (b) mechanical less only
   (c) iron loss and mechanical loss (d) copper loss only
4. A series motor must not be run at light/no load because
   (a) it will draw a dangerously large current
   (b) it will run at dangerously high speed
   (c) it will draw dangerously high current and run at dangerously high speed
   (d) it will stall
5. PC machine poles are constructed of thick laminations
   (a) to reduce iron loss in pole body and pale shoes
   (b) to reduce iron loss in pole body comfort and ease of construction.
   (c) to reduce pulsation loss in pole shoes and for ease of construction.
   (d) for ease of construction.
6. A differentially compound motor under high overload conditions will behave like a/an
   (a) shunt motor (b) series motor
   (c) cumulative compound motor (d) ac synchronous motor
7. A 6-pole, lap-wound, dc armature with 720 conductors draws 50A from the mains. Its armature reaction people is
   (a) 1000 AT peak, triangular wave shape (b) 500 AT peak, triangular wave shape
   (c) 1000 AT peak, sinusoidal wave shape (d) 500 AT peak, sinusoidal wave shape
8. The process of current communication in a dc machine is opposed by the
   (a) emf induced in the commutating coil because of the interpose flux
   (b) reactance emf
   (c) coil resistance
   (d) brush resistance
9. In Hopkinson's test on two identical dc shunt machines,
   (a) iron losses in both machines are equal
   (b) iron loss in the generating machine is more than that in the motoring machine
   (c) iron loss in the motoring machine is more than that in the generating machine
   (d) only starry-tool components of iron loss in both machines are equal.
10. In a separately excited dc motor, the motor back emf
    (a) reduces the effective motor time constant.
    (b) increases the effective motor time constant
    (c) does not affect the motor time constant
    (d) reduces the effective motor time constant to zero

Answers

Multiple-Choice Questions

1. (d) 2. (b) 3. (c) 4. (b) 5. (c)
6. (b) 7. (b) 8. (b) 9. (b) 10. (a)

Synchronous Machine—Generator (Alternator) and Motor

chapter 8

Goals & Objectives

- To familiarise with the general constructional features
- To know stator, rotor, field poles, armature windings, concept of electrical angle and mechanical angle
- What is synchronous speed, its determination from the frequency and number of machine poles
- The general emf formula
- To understand the rotating magnetic fields; conditions, speed and direction
- Interaction torque of rotating magnetic field, conditions for steady torque
- Synchronous machine, induction machine: their distinguishing features
- General approach to machine losses and efficiency, cooling
- Circuit model
- Determining of synchronous reactance
- Observing characteristics of synchronous machine

8.1 INTRODUCTION

Alternating emfs (ac) with three-phase connection are generated in an electric machine called alternator. It can feed ac current and power to a load. The alternator must be run by a prime mover at a speed so as to generate ac of 50 Hz (standard).

Electromechanical energy conversion takes place whenever a change in flux linkages is associated with mechanical motion. Speed voltage is generated in a coil when there is relative movement between the coil and magnetic field. Alternating emf is generated if the change in flux linkage of the coil is cyclic. The *field windings*, which are the primary source of flux in a machine, are therefore arranged to produce cyclic north-south space distribution of poles. A cylindrical structure is a natural choice for such a machine. Coils, which are seats of induced emf's, are several in number in practical machines and are suitably distributed and connected in series/parallel and in star/delta three-phase connection to give the desired voltage and to supply the rated currents; this arrangement is called the armature winding.

An alternator is a machine in which the field windings (even number of poles) are placed on the rotor and the stator carries ac armature windings as shown in Fig. 8.1. While the reverse structure is possible (field on stator and armature winding on rotor), the arrangement of Fig. 8.2 is almost universally adopted in a synchronous machine because of ease of mechanical construction and of insulating a high-voltage stationary winding. The field poles are made projecting, i.e. *salient type* (Fig. 8.1). For high-speed machines, *nonsalient* or *cylindrical* poles are preferred (Fig. 8.4). The field windings are excited through slip rings from a dc source as shown in Fig. 8.2. Generally, a small dc generator called the *excitor* is coupled to the shaft of the synchronous machine for this purpose. This type of machine must run at a definite fixed speed (called synchronous speed) corresponding to the frequency and number of poles.

An alternator can operate as a motor when fed from three-phase ac supply and mechanically loaded at the shaft; of course it can run only at synchronous speed rotated to the supplying frequency of 50 Hz.

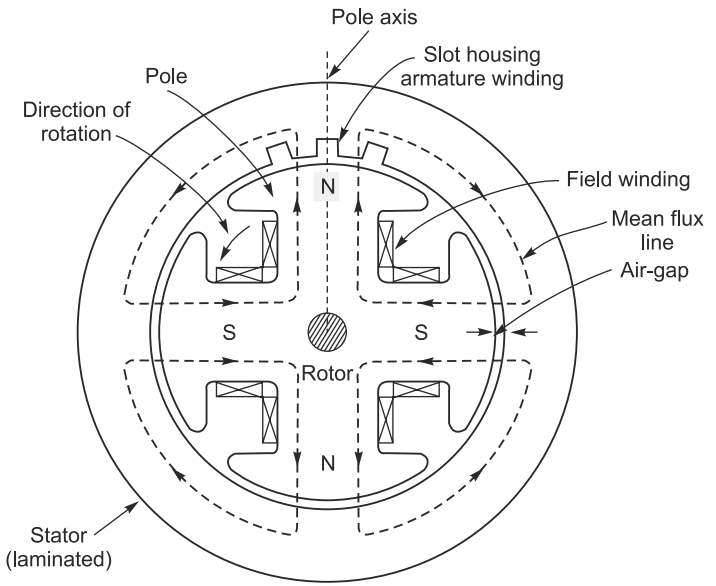


Fig. 8.1 *Salient-pole alternator (cross-sectional view); 4 poles*

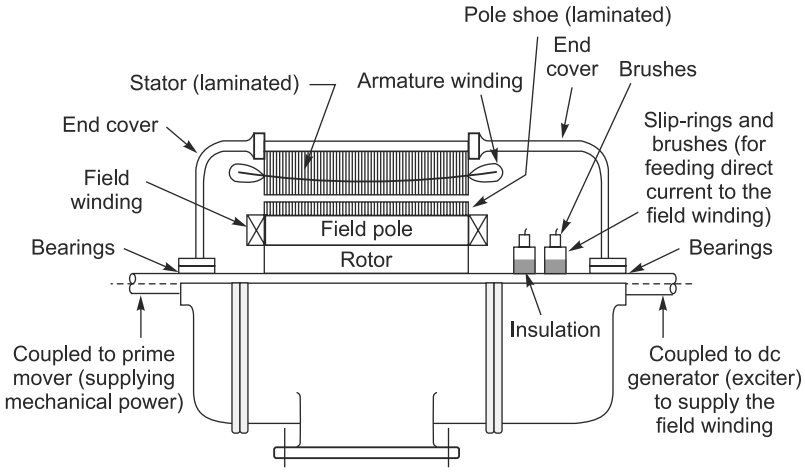


Fig. 8.2 *Alternator*

8.2 ELEMENTARY SYNCHRONOUS MACHINE

In the 4-pole structure exhibited in Fig. 8.1, the field poles have odd symmetry, viz. alternate north-south. The field coils are of *concentrated* kind. If the effect of armature slotting (a secondary affect) is ignored and the air-gap is assumed uniform over the pole faces, it is obvious that the air-gap flux density will be constant over a major part of the pole face, gradually reducing because of fringing at the pole tips and finally becoming zero in the interpolar region. The air-gap flux density wave (around the stator's inner periphery) is therefore a *flat-topped* wave as shown in Fig. 8.3(a).

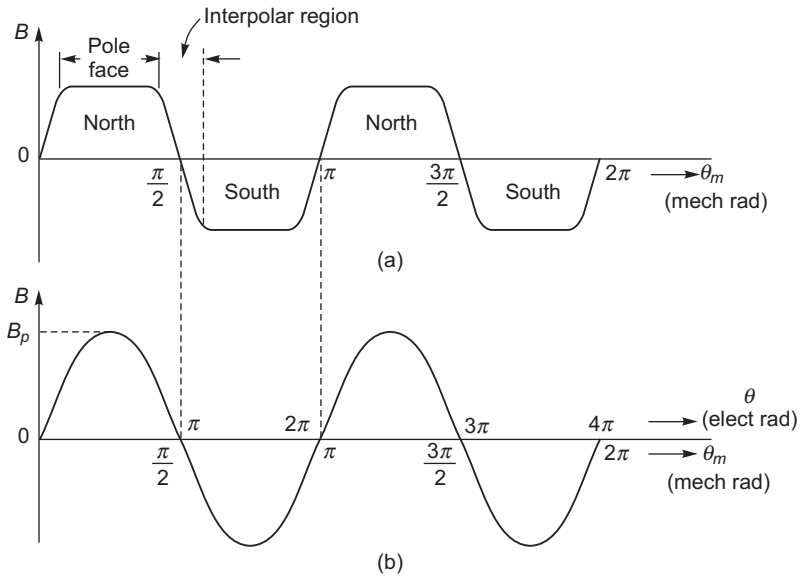


Fig. 8.3 *Flux density wave in electric machines (4-pole structure)*

This is not the right kind of flux density distribution as it is desirable to generate sinusoidal emf. The pole faces in such a machine structure (*salient-pole* kind) are therefore *chamfered* at the edges so that the air gap increases towards pole edges, causing the flux density wave to become nearly sinusoidal. It shall be assumed[1] from now on that the air gap flux density is sinusoidal as shown in Fig. 8.3(b).

The mechanical angle θ_m round the machine periphery is always 2π but it is more convenient to designate the complete angle of one cycle of the *B*-wave (north-south) as 2π, which to distinguish it is called the electrical angle θ. For a *P*-pole machine, the relationship between these two angles is expressed as

$$\frac{\theta}{\theta_m} = \frac{2\pi \times (P/2)}{2\pi} = \frac{P}{2} \tag{8.1}$$

Another method of achieving a nearly sinusoidal *B*-wave is to use a cylindrical (nonsalient) rotor structure with a uniform air gap but distributed field windings as depicted in Fig. 8.4. In this arrangement, as one moves away from the pole-axis, the flux paths link progressively smaller number of field ampere-turns and hence produces the nearly sinusoidal *B*-wave. The actual *B*-wave will have a stepped shape corresponding to the rotor slots. The high-frequency harmonics pertaining to these steps will be ignored in machine analysis here.

It is easily observed from that the *B*-wave repeats itself every one pole pair; so does the electrical conditions on the stator (this follows as a consequence). We can therefore picturise and model the machine on a one pole-pair basis in the form of the elementary machine shown in Fig. 8.5.

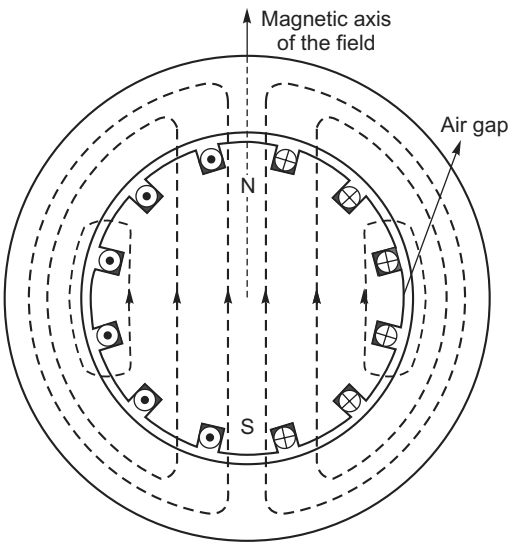


Fig. 8.4 *Nonsalient pole (cylindrical) rotor*

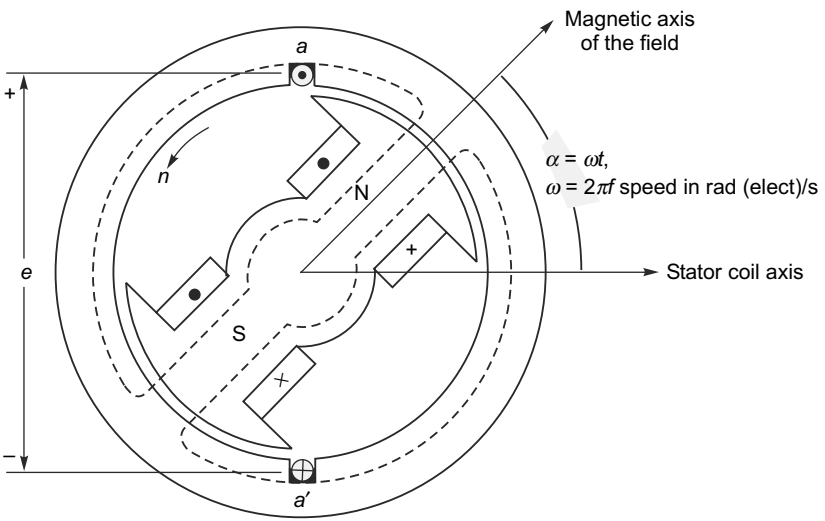


Fig. 8.5 *Elementary generator (synchronous)—salient-pole, 2-pole rotor*

[1] The harmonic emfs generated by the slightly nonsinusoidal *B*-wave are filtered out by the machine's leakage inductances and the inductive transmission lines.

Figure 8.5 shows an elementary 2-pole generator with a single armature coil. The coil may be single or multiturn and has generally a *diamond shape* as shown in Fig. 8.11. The two *coil-sides* (a, a') are located in stator slots spaced 1/2 B-wavelength or π (180°) electrical apart. Such a coil is known as *full-pitch* coil. Let the rotor rotate at a constant speed of n rpm or revolution per minute.

or
$$\omega = \left(\frac{P}{2}\right)\omega_m = \frac{\pi n P}{60} \text{ rad(elect)/s} \tag{8.2}$$

Figure 8.6(a) shows the cross-sectional developed view of the stator along with sinusoidal B-distribution (B-wave in space). This B-wave is present all along the axial length of the machine and the end effects are ignored. As the rotor rotates, the B-wave moves with it, gliding past the coil-sides. As a result, emf of the same wave shape as the B-wave, i.e. sinusoidal, is generated in each coil-side (Blv rule). At any time, the emfs induced in the coil-side a, a' are of the same magnitude but of opposite signs; therefore, around the coil these emfs add up so that the coil emf is twice the coil-side emf. This is in consequence of the fact that the two coil-sides are π radians (elect) apart which means that if one coil-side is under north pole the other is under south pole. The sinusoidal wave of the coil emf generated as a result of the rotor motion is depicted in Fig. 8.6(b).

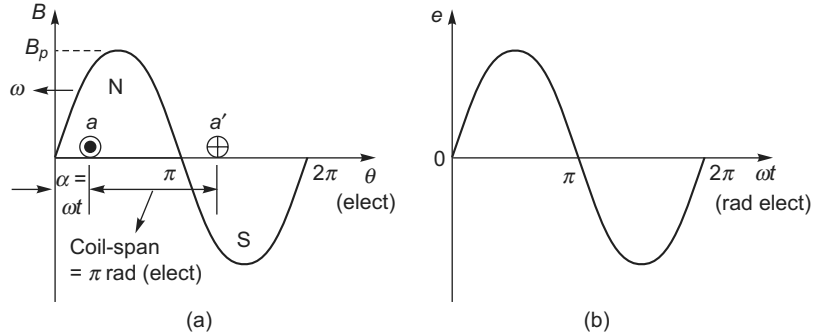


Fig. 8.6 *(a) B-wave and coil-sides at time t, (b) Coil emf*

One cycle of emf is generated when the rotor moves through the angle corresponding to one pole-pair (2π rad (elect)). Thus the frequency of emf generated is

$$f = \frac{\omega}{2\pi} = \frac{nP}{120}\text{Hz};\ \omega = \frac{\pi n P}{60} \tag{8.3}$$

It is seen from Eq. (8.3) that for a given number of poles, a certain frequency (power frequency is 50 Hz) is obtained at a definite speed called the *synchronous speed* and hence the name *synchronous generator*. For high-speed steam turbines, usually two poles at 3000 rpm are employed. High centrifugal forces at such high speeds demand cylindrical pole construction. For low-speed hydroturbines, say 16 poles, 375 rpm, salient pole is ideal construction.

8.3 THREE-PHASE GENERATOR (ALTERNATOR)

Practical synchronous generators are always of the three-phase kind in which three coils are placed in slots around the stator with a relative electrical spacing of 120° ($2\pi/3$) between the coil axes as illustrated in Fig. 8.7(a). As a consequence the emfs of the three coils (phases) differ relatively in time phase by 120°. The

three coils are usually connected in star, in a synchronous generator. It is observed from Fig. 8.7(a), that each phase occupies 60° elect/pole on the stator one after another with coil-side sequence *abc*.

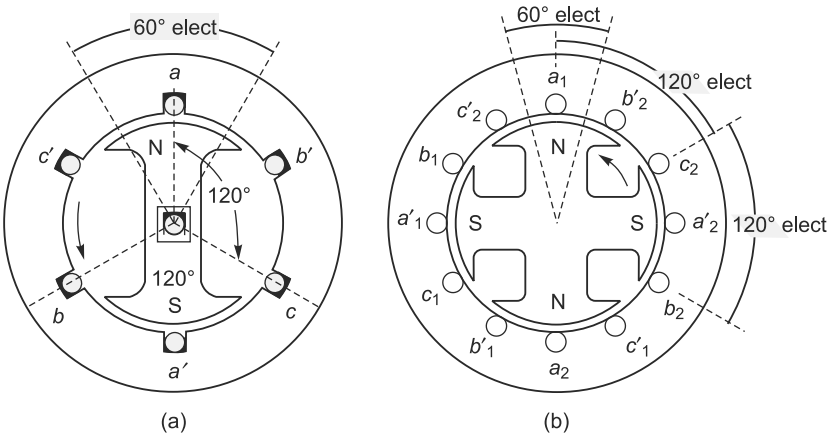


Fig. 8.7 *(a) Three-phase, 2-pole synchronous generator (b) Three-phase, 4-pole synchronous generator*

Figure 8.7(b) shows the corresponding arrangement for a 4-pole generator. Since the total electrical angle of the machine is 4π radians, each phase now has two coils with coil axis spacing of 2π. The two coils of each phase can be connected in series or parallel, as shown in Fig. 8.8(a), and (b) depending upon voltage and current requirement of the machine. Series connection means current corresponding to coil current (limited from heating point of view) and voltage twice that of coil voltage. In parallel connection, voltage is same as the coil voltage while current is twice that of the coil current. The three phases so connected are connected in star.

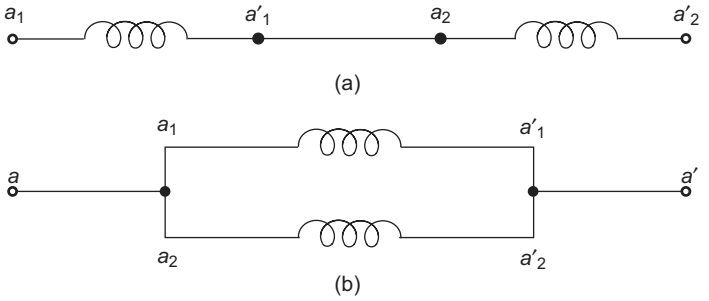


Fig. 8.8 *(a) Series connections (b) Parallel connections*

8.4 GENERATED emf OF ac WINDINGS

The *B*-wave (assumed sinusoidal) of the elementary machine depicted in Fig. 8.5 is drawn in Fig. 8.6(a). It can be expressed as

$$B = B_p \sin \theta \tag{8.4}$$

where B_p is the peak flux density and θ is the electrical angle.

The flux contained in an angle $d\theta$ is

$$d\phi = Blr\left(\frac{2}{P}\right)d\theta;\ d\theta_m = \left(\frac{2}{P}\right)d\theta$$

where l is the stator length (axial) or active conductor length and r is the mean air-gap radius of machine.

The flux linking the coil (single turn) is given by

$$\phi = \int_{\alpha}^{\alpha+\pi} lr\left(\frac{2}{P}\right)B_P \sin\theta\, d\theta = \left(\frac{4}{P}\right)B_P\, lr\cos\alpha$$

But $\alpha = \omega t$

$$\therefore \quad \phi = \left(\frac{4}{P}\right)B_P\, lr\cos\omega t \tag{8.5}$$

The flux/pole is then given by

$$\Phi = B_{\text{av}} \times 2\pi\frac{lr}{P}$$

For sinusoidal flux density distribution,

$$B_{\text{av}} = \left(\frac{2}{\pi}\right)B_P \tag{8.6}$$

$$\therefore \quad \Phi = \left(\frac{2}{\pi}B_P\right)\times 2\pi\frac{lr}{P} = \left(\frac{4}{P}\right)B_P lr$$

$$\therefore \quad \phi = \Phi\ \cos\ \omega t \tag{8.7}$$

Flux linking an N-turn coil is given by

$$\lambda = N\Phi = N\Phi\cos\ \omega t \tag{8.8}$$

Hence, the coil emf is given by

$$e = -\frac{\mathrm{d}\lambda}{\mathrm{d}t} = \omega N\Phi\sin\ \omega t \tag{8.9}$$

wherein the assumed positive direction of emf is such that if current were allowed to flow in that direction, it would cause flux to be produced in the positive direction along the coil axis. Observe that for convenience, we used $e = +(d\lambda/\mathrm{d}t)$ in the transformer and negative sign in emf was incorporated in the circuit diagram.

The rms value of the coil (phase) emf is

$$E = \sqrt{2}\pi fN\Phi = 4.44\, fN\Phi \tag{8.10}$$

which is the same result as in transformer except that Φ here means flux/pole.

It follows from Eqs (8.8) and (8.9) that the flux linkage phasor (loosely called flux phasor) leads the phase emf phasor by 90° as depicted in Fig. 8.9. Compare it with the transformer case.

The difference in the two is explained by the negative sign in $e = -d\lambda/dt$.

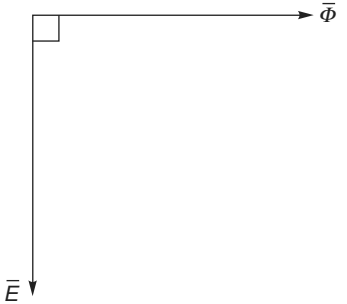


Fig. 8.9 *Flux phasor*

8.4.1 Distributed Winding

In order to fully utilise the armature periphery and further to build higher voltages (it may be as high as $11/\sqrt{3}$ kV or even $37/\sqrt{3}$ kV per phase), more than one coil/pole-pair/phase, i.e. more than one Slot/Pole/Phase (SPP), are employed in practice. Figure 8.10 shows a generator (2-pole) with SPP = 3. Such an arrangement for armature winding is called distributed winding. The total number of slots S are uniformly distributed around the armature. Then

$$\text{SPP} = m = \frac{S}{3} \tag{8.11}$$

The angle between adjacent slots is

$$\gamma = \frac{\pi P}{S} \text{ rad (elect)} \tag{8.12}$$

The emf induced in the phase coils therefore differs progressively by angle γ (elect) though the amplitude of emf is the same in each coil.

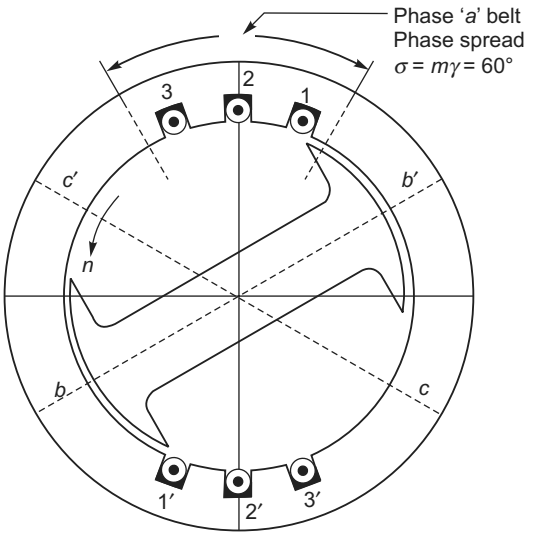


Fig. 8.10 *Synchronous generator with distributed winding*

The total emf of phase coils is therefore less than their algebraic sum of coil emfs by a factor called *breadth factor* (or distribution factor), given by

$$K_b = \frac{\sin(m\gamma/2)}{m\sin(\gamma/2)} < 1 \tag{8.13}$$

The phase emf formula then becomes

$$E_p = 4.44 k_b f N_{ph} \Phi \tag{8.14}$$

where N_{ph} = series connected turns/phase

Short-pitched Coils

Coil span less than π by β. It reduces the coil emf by the

Pitch factor

$$k_p = \cos \beta/2 \tag{8.15}$$

Hence, phase-induced emf in general is

$$E_p = 4 \cdot 44 K_b K_p f N_{ph} \Phi \tag{8.16}$$

or

$$E_p = 4 \cdot 44 K_w f N_{ph} \Phi \tag{8.17}$$

where winding factor $K_\omega = K_b t_p$

nth harmonic

$$\gamma/2 \rightarrow n\gamma/2$$

resulting in reduction of K_b and K_p. So harmonics get reduce. In fact short pithing can eliminate specific harmonic ($K_p = 0$)

8.4.2 Two-Layer Winding

It was so far assumed that only one coil-side is accommodated in each slot (single-layer winding). In modern practice, however, two coil-sides/slot are placed with one side of each coil being in top layer and the other

side in the bottom layer of a slot π radians (elect) away for full-pitch coils. The shape of such a coil is shown in Fig. 8.11. The winding layout in *developed form* is shown in Fig. 8.12 for 4 poles and SPP = 1. The top layer coil-sides are shown in solid lines and the bottom layer coil-sides are in dotted lines. The direction of the induced emf of the coil-sides in each slot are indicated in Fig. 8.12. We find from the connections indicated that coils 1 and 3 are in series and coils 2 and 4 are in series and these two sets are connected in parallel. Therefore,

$$i \text{ (phase)} = 2i_c \text{ (coil)}$$

and emf (phase) = emf of two distributed coils in series

It is possible to connect all the four coils in series, which will yield $i_p = i_c$ and double the phase emf.

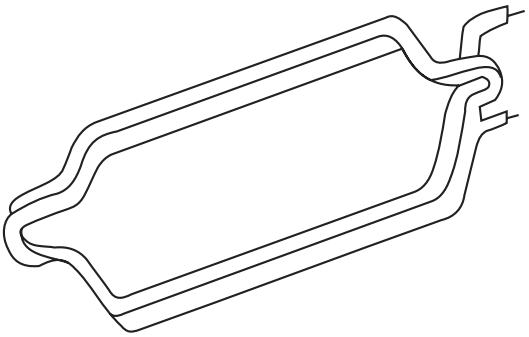


Fig. 8.11 *Coil of a double-layer winding*

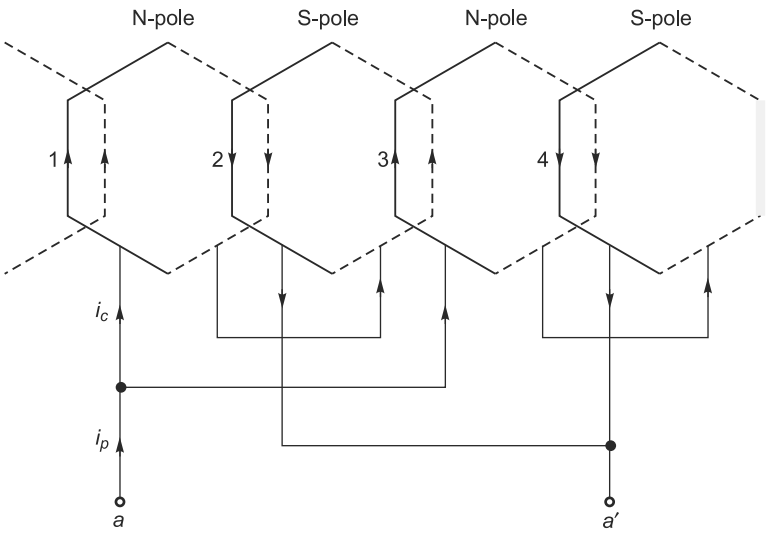


Fig. 8.12 *One phase of a double-layer winding (4 poles, SPP = 1)*

This type of winding offers the advantages that all coils are identical in shape (convenience in the manufacturing process) and that the end portions of the coils (overhang) can be neatly arranged mechanically.

Example 8.1

A 50 Hz, 6-pole synchronous generator has 36 slots. It has a two-layer winding with full-pitch coils of 10 turns each. The flux/pole is 0.016 Wb (sinusoidally distributed). Determine the induced emf (line-to-line) if the coils are connected to form a 1-phase winding, if the current-carrying capacity of conductor composing coils is 10 A.

Solution 1-phase winding:

$$m = \frac{S}{P} = \frac{36}{6} = 6$$

$$\gamma = \frac{180 \times 6}{36} = 30^\circ$$

$$K_b = \frac{\sin m\gamma/2}{m \sin \gamma/2} = \frac{\sin 6 \times 30^\circ/2}{6 \sin 30^\circ/2}$$

$$N_{\text{ph}} = 36 \times 10 = 360$$

$$E_p = 4.44\, K_b f N_{\text{ph}}\, \phi$$

8.5 ROTATING MAGNETIC FIELD

Consider now the three phases of an ac winding carrying balanced alternating currents (phase sequence abc). Then,

$$\begin{aligned} i_a &= i_m \cos \omega t \\ i_b &= I_m \cos (\omega t - 120^\circ) \\ i_c &= I_m \cos (\omega t - 240^\circ) \end{aligned} \tag{8.18}$$

Figure 8.13 shows the three-phase coils (concentrated) along with their magnetic axes, which are located 120° (elect) apart in space. The three mmfs can be expressed as

$$\begin{aligned} F_a &= F_m \cos \omega t \cos \theta \\ F_b &= F_m \cos (\omega t - 120^\circ) \cos (\theta - 120^\circ) \\ F_c &= F_m \cos (\omega t - 240^\circ) \cos (\theta - 240^\circ) \end{aligned} \tag{8.19}$$

The resulting mmf wave is then given by

$$\begin{aligned} F &= F_a + F_b + F_c \\ &= F_m[\cos \omega t \cos \theta + \cos (\omega t - 120^\circ) \cos (\theta - 120^\circ) \\ &\qquad + \cos (\omega t - 240^\circ) \cos (\theta - 240^\circ)] \end{aligned}$$

Simplifying trigonometrically,

$$F(\theta, t) = \frac{3}{2} F_m \cos(\omega t - \theta) + \frac{1}{2} F_m [\cos(\omega t + \theta)] + \cos (\omega t + \theta - 240^\circ) + \cos (\omega t + \theta - 480^\circ)$$

$$= \frac{3}{2} F_m \cos(\omega t - \theta) \tag{8.20}$$

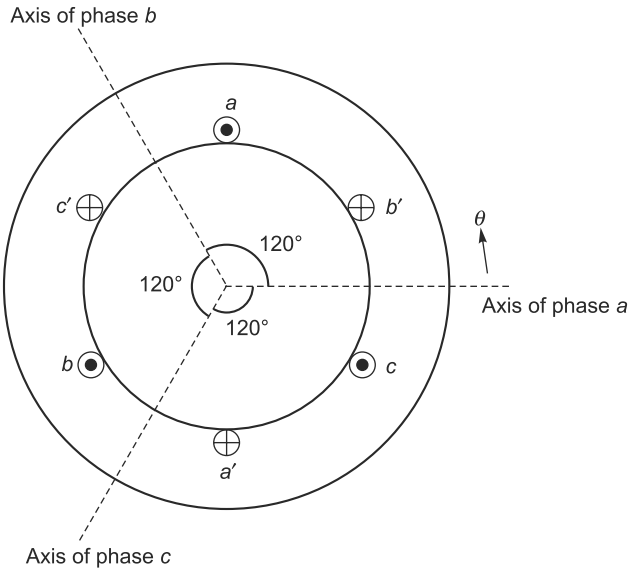


Fig. 8.13 *Relative location of the magnetic axes of the three phases*

As per Eq. (8.20), the resultant field rotates at speed $\omega = 2\pi f$ rad (elect)/s or $n = 120f/P$ rpm, *synchronous speed*, in the direction from the *leading to the lagging* phase axis; *a*-axis to be axis in Fig. 8.13. The direction of rotation can be easily reversed by changing the phase sequence of the currents (interchange two stator leads as connected to the source (three-phase)). The peak amplitude of the resultant field is

$$F_{\text{peak}} = \frac{3}{2}F_m \tag{8.21}$$

Conclusion

Whenever a three-phase winding, with 120°(elect) *spatial phase difference* between the axes of the three phases is fed, with balanced three-phase currents with a *time phase difference* of 120°(elect), the resultant mmf (and its associated *B*-wave) rotates at synchronous speed $\omega_s = 2\pi f$ radians (elect)/s (or $n_s = 120\,f/P$ rpm). The direction of rotation of the mmf wave is from the leading to the lagging phase and can be reversed by changing the phase sequence of currents.

Physical Picture

A sinusoidally distributed (in space) field can be represented by a vector oriented along its peak value, i.e. along the coil axis. The vector oscillates if the coil carries alternating current.

At $\omega t = 0$ [from Eq. (8.18)]

$$i_a = I_m, i_b = -\frac{1}{2}I_m, i_c = -\frac{1}{2}I_m$$

The corresponding three field vectors are drawn in Fig. 8.14 ($F_a = F_m$, $F_b = -1/2\ F_m$ and $F_c = -1/2\ F_m$) wherein it is shown that the resultant field has a peak value of (3/2) F_m and is directed along the axis of phase *a*.

At $\omega t = 120°$,

$$i_a = -\frac{1}{2}I_m, i_b = I_m, i_c = -\frac{1}{2}I_m$$

It immediately follows that the resultant field would now lie along the axis of phase *b* (counterclockwise rotation) and will have the same peak value ((3/2) F_m).

Similarly, at $\omega t = 240°$, the resultant field will lie along the axis of phase *c* and so on.

Figure 8.14 illustrates physically the concept of a rotating magnetic field whose speed is $\omega_S = 2\pi f$ rad (elect)/s.

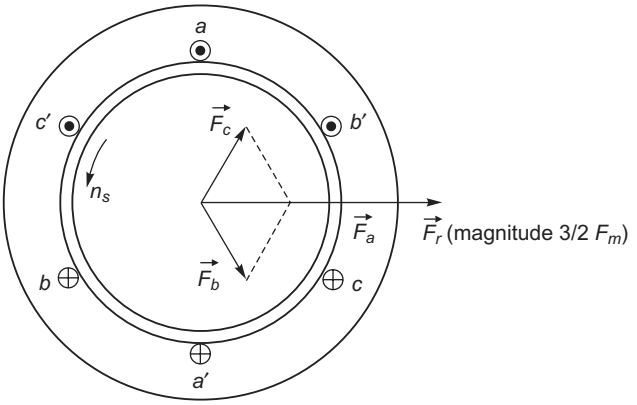


Fig. 8.14 *Resultant field at $\omega t = 0$; peak value (3/2) F_m along the axis of phase a*

Example 8.2

A three-phase, 6-pole, 50 Hz synchronous machine is carrying balanced currents. Its peak fundamental field has a value of 450 AT.

(a) Write the expression for F_{a1} in terms of electrical as well as mechanical space angles.
(b) Write the expression for the rotating stator field.
(c) What is its speed in rpm and mechanical rad/s?

Solution

(a) $F_{a1} = 450 \cos \omega t \cos \theta_c$ AT, $\omega = 2\pi f = 314$ rad/s

$= 450 \cos \omega t \cos 3\theta_m$

(b) Rotating field

$$F = \frac{3}{2} \times 450 \cos(\omega t - \theta_c) \text{ AT}$$

(c) $$n_s = \frac{120 \times 50}{6} = 1000 \text{ rpm},$$

$$\omega_m = \frac{2\pi}{60} \times 1000 = 104.7 \text{ mech rad/s}$$

8.6 TORQUE IN ROUND ROTOR MACHINE

From a field viewpoint, electromagnetic torque is the result of interaction of two magnetic fields in the air gap, one $\vec{F}_1$ created by the stator currents and the other $\vec{F}_2$ by the rotor currents. For creation of steady torque, the following two conditions must be met:

- The two fields must be stationary relative to each other.
- The two fields must have the same number of poles.

The reason for these will become obvious from the discussion that follows.

Figure 8.15(a) shows the cross-sectional view of a 2-pole round rotor machine. The axes of the stator and rotor fields are indicated therein and these have an angle A between them. It is immediately obvious that the attractive forces between the rotor north and stator south, and also that between the rotor south and stator north cause a torque to act on the rotor in the direction indicated tending to reduce λ, i.e. it tends to align the two fields. This torque will be balanced by the prime mover/load torque at a steady value of λ. There will of course be a reaction torque on the stator in the opposite direction, which will be balanced by the bolting down of the stator to the foundations. It is assumed that the two fields are stationary relative to each other, as only then is a steady torque possible. If the fields were to rotate relative to each other, the attractive forces between them will alternate by repelling forces resulting in average zero torque.

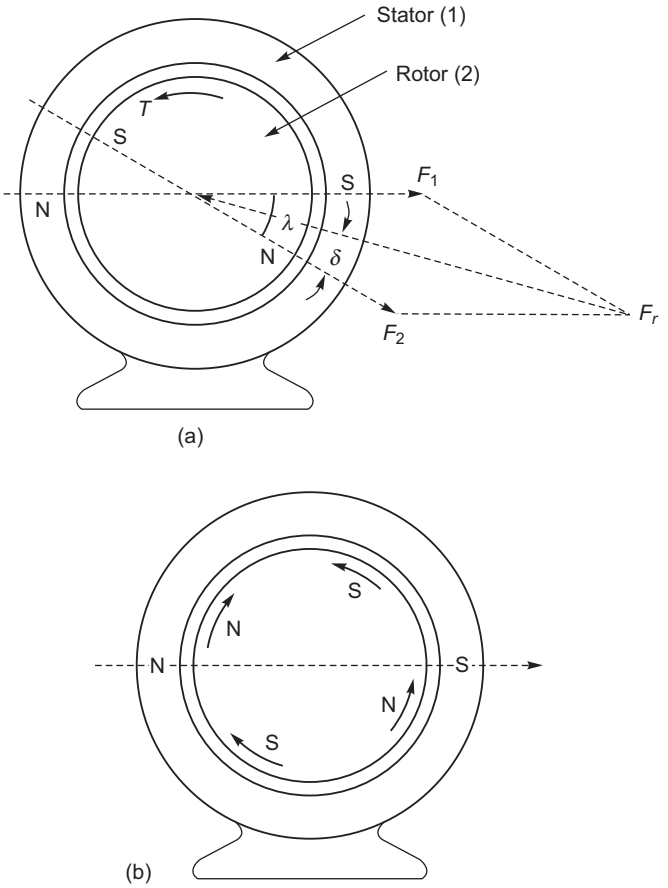


Fig. 8.15 *(a) Torque in round rotor machine (b) Case of 2-pole stator and 4-pole rotor*

Figure 8.15(b) shows a 2-pole stator and a 4-pole rotor. It is easily seen from this figure that the forces on the rotor surface alternate resulting in net zero torque and hence the condition that both the fields (stator and rotor) must have the same number of poles.

Figure 8.15(a) shows the vector representation of two sinusoidally distributed fields of peak values F_1 and F_2; F_r is the *resultant field*. Because of sinusoidal flux density distribution caused by these fields, it is intuitive to expect that the interaction torque would be proportional to the sine of λ, the angle of separation of their axes. This torque can be expressed as

$$T = K' F_1 F_2 \sin \lambda$$

or
$$T = K' F_r F_2 \sin \delta \tag{8.22}$$

where δ is the angle between the axes of F_r and F_2.

For cylindrical rotor permeance

$$\Phi_r \propto F_r$$

Also $F_2 \propto I_2$ (rotor current)

We can the write

$$T = K \Phi_r I_2 \sin \delta$$

Generating Operation

The field vector $\overline{\mathbf{F}}_1$, $\overline{\mathbf{F}}_2$, and $\overline{\mathbf{F}}_r$ are shown for a generating machine in Fig. 8.16(a). It is seen that $\overline{\mathbf{F}}_2$ load $\overline{\mathbf{F}}_r$ by angle δ. $\overline{\mathbf{F}}_2$ pulls $\overline{\mathbf{F}}_1$ in the direction of the rotor rotation at synchronous speed n_s. The interaction of the fields produce torque T in opposite direction such that $T = T_{PM}$ and the mechanical power input at rotor shift get converted to electrical power (output) at stator terminals.

Motoring Operation

As shown in Fig. 8.16(b), $\overline{\mathbf{F}}_2$ lags $\overline{\mathbf{F}}_r$, by angle δ in opposite direction of rotation. $\overline{\mathbf{F}}_1$ now pulls $\overline{\mathbf{F}}_2$ (the rotor) along with it at synchronous speed n_s. The interaction of the fields produces the electromagnetic torque $T = T_L$ (mechanical load torque) resulting in conversion of electrical power (input) to mechanical power (output).

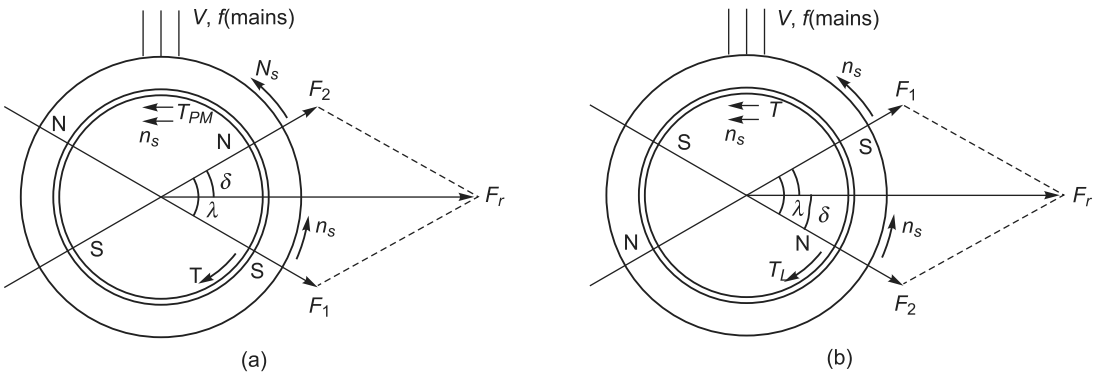


Fig. 8.16 *Torque production in synchronous machine: (a) Generating operation (b) Motoring operation*

Torque-angle (T-δ) Characteristics

For a certain stator, terminal voltage V

$$V(\text{line}) = \sqrt{3} \times 4.44 K_w f \, \Phi_r N_{\text{ph}} \text{ (series)} \tag{8.23}$$

if the stator resistance and leakage reactance (per phase) are ignored. Thus, for a given terminal voltage, Φ_r remains constant (as in a transformer). For a given field current ($I_f = I_2$), Eq. (8.22) becomes

$$T = K_T \sin \delta \tag{8.24}$$

The sinusoidal T–δ relationship of Eq. (8.24) is called *torque-angle* [or *power angle* ($P = T\omega_s$)] characteristic diagram. Maximum electromagnetic torque, called *pull-out* torque, is produced at $\delta = 90°$.

8.7 CIRCUIT MODEL (EQUIVALENT CIRCUIT)

8.7.1 Heuristic Treatment

Rather than finding the resultant field and therefrom determining the induced emf of the machine, we will proceed on the basis that the magnetic circuit is linear, because of the predominant air gap. It means that by the superposition theorem we can add the emf phasors corresponding to the individual fields to determine the resultant emf phasor. It implies that instead of the field Eq. (8.2), we use the phasor emf equation.

$$\bar{E}_r = \bar{E}_f + \bar{E}_a \tag{8.25}$$

We shall ignore at present the resistance and leakage reactance of the armature. Therefore, the terminal voltage

$$\bar{V}_t = \bar{E}_r \tag{8.26}$$

To model Eq. (8.25) as a circuit, we need to identify $\bar{E}_a$ as the voltage drop of a circuit element. We immediately notice that $\bar{E}_a \propto \bar{I}_a$ as it is caused by $\bar{F}_a$. Further, we need to determine the effect on $\bar{E}_a$, as the phase angle of $\bar{I}_a$ with respect to $\bar{E}_f$, which is varied over –90° to 0° to + 90°. We assume that $\bar{I}_a$ flows in the direction of $\bar{E}_a$ which means that the machine is *generating*. We proceed as per phase basis; phase '*a*'.

At *non-load*, $\bar{I}_a = 0$ and so $\bar{F}_a = 0$. The rotor field $\bar{F}_f$ induces emf $\bar{E}_f$, which is called the *excitation* emf.

Case 1. $\bar{I}_a$ lags $\bar{E}_f$ by 90"

It means that the current maximum occurs 90° later than the emf maximum. Therefore, when the current of phase '*a*' is maximum, its emf is zero and so $\bar{F}_f$ lies along the axis of phase '*a*' coil as shown in Fig. 8.17(a). The armature reaction field is also directed along the axis of phase '*a*' coil but in opposition to $\bar{F}_f$. Thus, the armature reaction is *demagnetising* and the emf $\bar{E}_a$ is in phase opposition to $\bar{E}_f$. Thus $V_t = E_r < E_f$.

Case 2. $\bar{I}_a$ in-phase with $\bar{E}_f$

On the arguments, as in Case 1, the three-phase currents and the corresponding locations of $\bar{F}_f$ and $\bar{F}_a$ are shown in Fig. 8.17(b). We find that $\bar{F}_a$ is *cross magnetising* and therefore, it will have only marginal effect on $\vec{F}_r$; So $V_t = E_r \approx E_f$.

Case 3. $\bar{I}_a$ leading $\bar{E}_f$ by 90°

This corresponds to the currents and pole positions as shown in Fig. 8.17(c). $\bar{F}_a$ now directly aids $\bar{F}_f$, which means it is *magnetising*. Therefore, $\bar{E}_a$ is in phase with $\bar{E}_f$ and so $V_t = E_r > E_f$ for the generating machine.

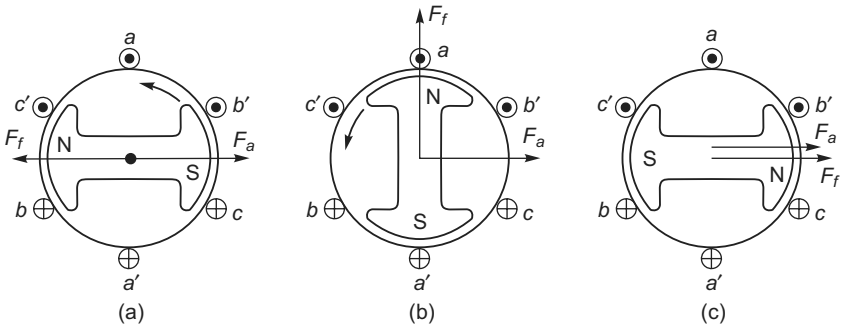


Fig. 8.17 *Air-gap field picture for various armature current phase angles*

The above illustrated effect of the armature reaction field on the resultant induced emf can be simulated by the circuit model as shown in Fig. 8.18. The series inductive reactance X_a equivalently replaces the armature reaction induced emf $\bar{E}_a$. The generating circuit equation is

$$\bar{V}_t = \bar{E}_f + \bar{E}_a = \bar{E}_f - j X_a \bar{I}_a \qquad (8.27)$$

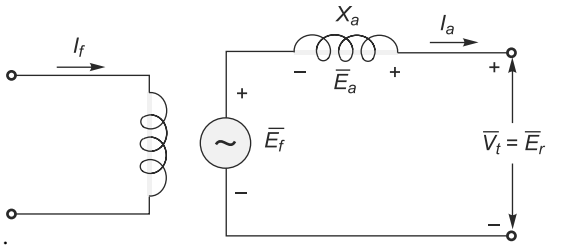


Fig. 8.18 *Circuit model of synchronous machine (generating)*

where $\bar{E}_f$ = excitation emf

$\bar{E}_a$ = armature reaction emf = $-j X_a I_a$

The corresponding phasor diagram for $\bar{I}_a$, 90° lagging, in-phase and 90° leading are drawn respectively in Figs 8.19(a), (b) and (c). These phase diagrams confirm the conclusions drawn earlier in cases 1, 2 and 3. Thus,

$$\bar{V}_t = \bar{E}_f + \bar{E}_a = \bar{E}_f - j X_a \bar{I}_a$$

$\bar{E}_f$ = excitation emf, $\bar{E}_a$ = emf induced by armature reaction field

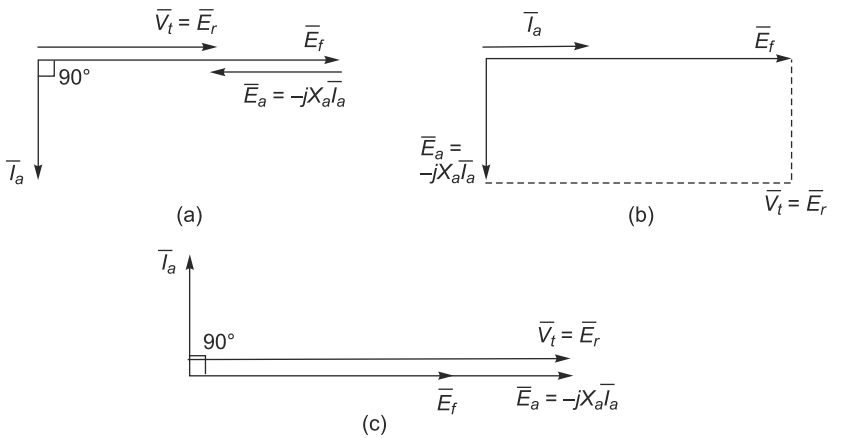


Fig. 8.19 *Phasor diagram of synchronous machine generating*

8.7.2 Circuit Model Inclusive of Armature Leakage Reactance

The circuit model of Fig. 8.20(a) or Fig. 8.18 modifies to that of Fig. 8.20(b) if the armature leakage reactance is accounted for. We define

$$X_s = X_a + X_l,\ X_l = \text{leakage reactance} \tag{8.28}$$
$$= \textit{synchronous reactance (per phase)}$$

In the simplified model of Fig. 8.20(c), the identity of E_r is not preserved as it is no longer necessary to do so. Observe that the circuit model is the same as in a transformer except that E_f is controlled by I_f.

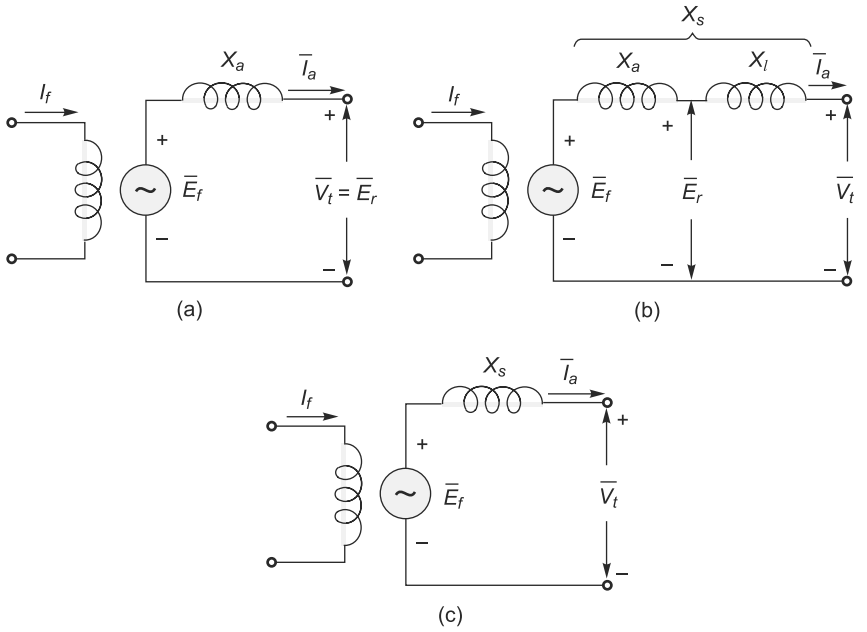


Fig. 8.20 *Synchronous machine (generating)*

In the circuit model of a synchronous machine, the machine is *generating* when the armature current $\bar{I}_a$ is in the direction of $\bar{E}_f$ and so flows out of the positive terminal of the machine as shown in Fig. 8.20(c). The machine is *motoring* when the armature current $\bar{I}_a$ flows into the positive terminal of the machine and so in opposition to $\bar{E}_f$ as shown in Fig. 8.21.

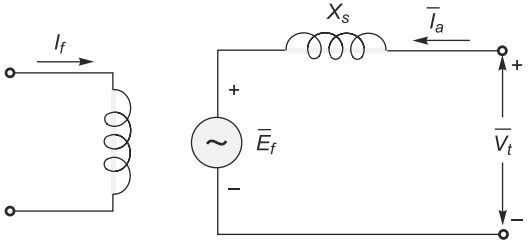


Fig. 8.21 *Synchronous machine (motoring)*

The circuit equations for the two operations of the synchronous machine are,

$$\bar{V}_t = \bar{E}_f - jX_a\bar{I}_a \text{ (generating)} \tag{8.29a}$$

$$= \bar{E}_f + jX_s\bar{I}_a \text{ (motoring)} \tag{8.29b}$$

If the machine resistance is taken into account, the total impedance per phase would be

$$Z_s = [R_a^2 + X_a^2]^{1/2} = \textit{synchronous impedance}$$

The armature resistance in a synchronous machine is usually as low as 0.01 pu and can be ignored for all performance calculations except machine efficiency. The synchronous reactance is of the order of 0.5–1.0 pu (compare with transformer leakage reactance of 0.05 pu).

8.7.3 Determination of Synchronous Reactance

As in a transformer, X_s can be determined by the OC and SC tests as in the circuit diagram of Fig. 8.22. Under OC conditions, i.e. $I_a = 0$, it follows from Eq. (8.29a) that, V_{OC} is the line-to-line open-circuit voltage. The Open-Circuit Characteristic (OCC) is the plot of V_{OC} vs. I_f, which indeed is the magnetisation characteristic of the machine and is drawn in Fig. 8.23. The linear part of the OCC is the *air-gap line*.

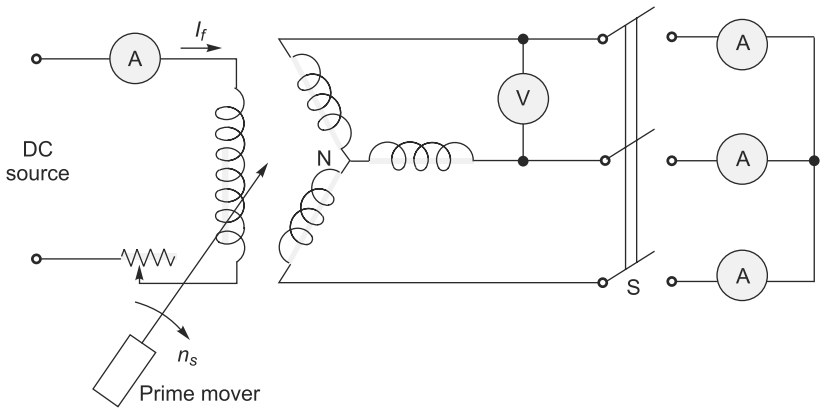


Fig. 8.22 *Circuit diagram for OC and SC tests*

The SC test is carried out with field initially open and the armature switch *S* (Fig. 8.22) closed. The field current I_f is gradually raised till the armature current reaches I_a (rated). Because of armature short circuit, this would occur at very much reduced excitation (very low I_f). The Short-Circuit Characteristic (SCC) is the plot of I_{SC} vs I_f shown in Fig. 8.23. It is linear as the magnetic circuit is unsaturated (low I_f). Therefore, only one point on the SCC needs to be determined.

The *unsaturated synchronous reactance* is then found from the air-gap line and the SCC corresponding to the same value of I_f. It follows from Fig. 8.5(c) and Eq. 8.9(a) with $V_t = 0$ that

$$X_s \text{ (unsaturated)} = \left.\frac{V_{OC}/\sqrt{3}}{I_{SC}}\right|_{\text{at same } I_f} \tag{8.30}$$

X_s as obtained from various points corresponding to the OCC reduces sharply in the saturated region (dotted curve in Fig. 8.23). Under load conditions, the machine is operated under a somewhat saturated magnetic condition when X_s will be less than that in the unsaturated region. It is therefore more realistic to use X_s (adjusted) obtained as below.

$$X_s \text{ (adjusted)} = \left.\frac{V_{OC}/\sqrt{3}}{I_{SC}}\right|_{\substack{I_f \text{ corresponding to} \\ V_t \text{ (rated) on OCC}}} \tag{8.31}$$

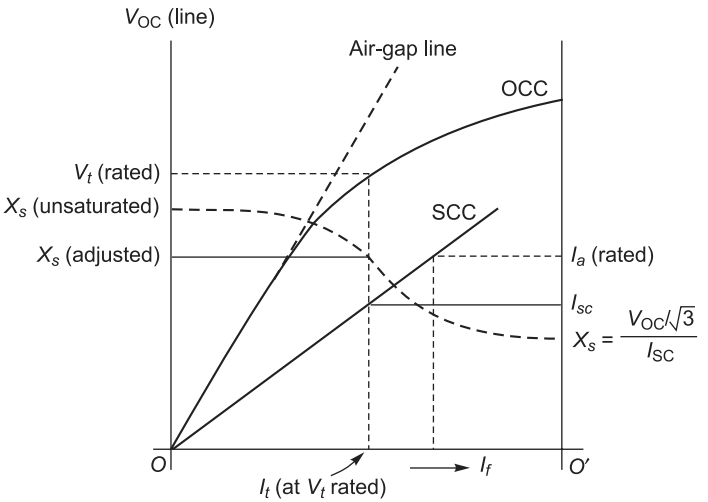


Fig. 8.23 *SCC and determination of X_s*

8.7.4 Voltage Regulation

It is the percentage change in the terminal voltage of a synchronous generator as full load at a specified power factor and rated voltage is thrown off. Thus,

$$\text{Voltage } Reg = \left.\frac{V_t(\text{no load})\big|_{I_f \text{ same as at full load}} - V_t(\text{rated})}{V_t(\text{rated})}\right|_{\text{At specified } pf} \tag{8.32}$$

Obviously,

$$V_t(\text{no load}) = E_f(\text{excitation emf})$$

It is convenient to take all voltages in line-to-line.

As in a transformer, the voltage regulation can be positive, zero or negative depending upon the load pf. Unlike a transformer, the pu synchronous reactance of a synchronous machine is far larger in the range 0.5–0.8 pu or even 1.0. Voltage calculation must therefore proceed using Eq. (8.29a) and no approximation can be used.

Example 8.3

The *OC* and *SC* test data of a 3-phase 1 MVA, 6.6 kV, star-connected synchronous generator is given below:

I_f (A)	60	70	80	90	100	110
V_{oc} (line) (V)	4693	5500	6160	6600	6967	7260
SC (A)	98					

Find

(a) unsaturated synchronous reactance,
(b) adjusted synchronous reactance,
(c) excitation voltage needed to give rated voltage at full load, 0.8 pf lagging. Use adjusted synchronous reactance.
(d) also the voltage regulation for the load specified in part (c).

Solution The *OCC* and *SCC* are plotted in Fig. 8.24.

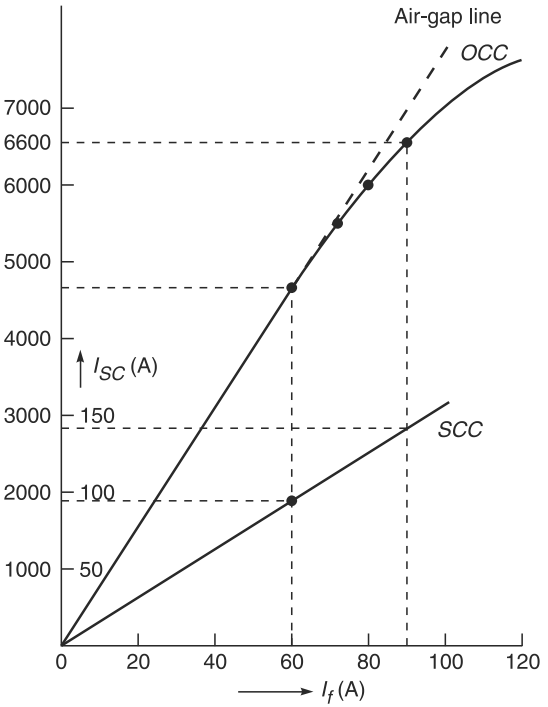


Fig. 8.24

(a) Corresponding to $I_f = 60$ A (unsaturated region)

$$X_s \text{ (unsaturated)} = \frac{4700\sqrt{3}}{98}$$
$$= 27.7\ \Omega$$

(b) Corresponding to $V_{\text{rated}} = 6600$ V

$$X_s \text{ (adjusted)} = \frac{6600\sqrt{3}}{143}$$
$$= 26.65\ \Omega$$

(c) At full load, 0.8 *pf* lagging

$$I_a = \frac{100}{\sqrt{3} \times 6.6} = 87.48 \text{ A}$$

pf angle = 39.9° lag

$$\bar{I}_a = 87.48\,(0.8 - j\,0.6) = 70 - j\,52.5$$

From Eq. (8.29a)

$$\bar{E}_f = V_t + j\,\bar{X}_s\,\bar{I}_a$$

$$\bar{E}_f = 6600\ \angle 0° + j\,26.65\,(70 - j\,52.5)\ \sqrt{3}\ ;$$

(in line values)

$$= 6600 + 2423 + j\,3225 = 9023 + j\,3225$$

$$E_f = 9582 \text{ V (excitation voltage)}$$

(d) Voltage regulation $= \dfrac{9582 - 6600}{6600} \times 100\ \times 100$

$$= 45.2\%$$

Synchronising to Mains

For synchronising to mains, the machine is run as a generator with terminals arranged to have the same phase sequence as the mains. Its speed and field current are adjusted such that

- the machine terminal voltage is nearly equal to that of the mains, and
- the machine frequency is nearly equal to that of the mains, i.e. its speed is close to synchronous.

The connection diagram is shown in Fig. 8.25. The two sets of three-phase phasors rotate with respect to each other at the difference in their frequencies as shown in Fig. 8.26. The rms voltages V_{L1}, V_{L2} and V_{L3} respectively across lamps L_1, L_2 and L_3 oscillate at the difference frequency. At the instant of synchronisation, when the two sets of phasors are co-phasal, $V_{L1} = 0$, $V_{L2} = V_{L3}$, i.e. lamp L_1 is dark and L_2, L_3 are equally bright. The machine is switched on the mains.

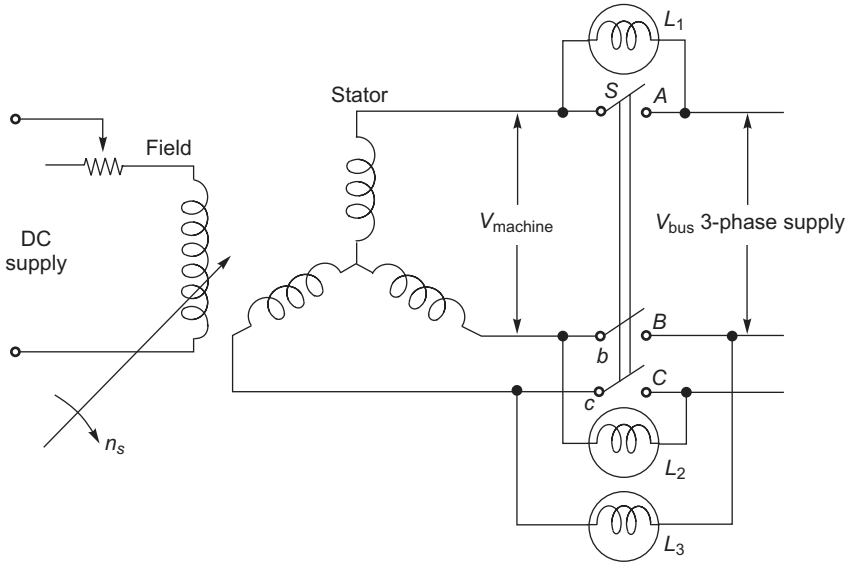


Fig. 8.25 *Synchronising to mains*

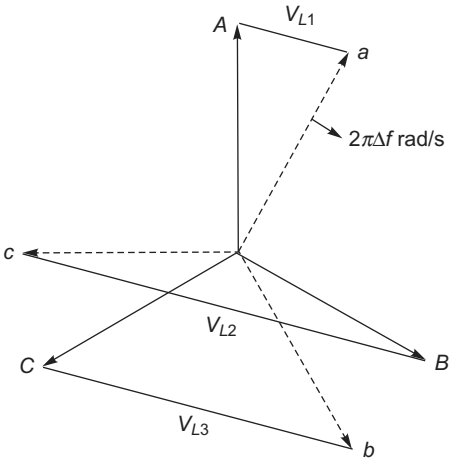


Fig. 8.26 *Determining instant of synchronisation*

Acceptable phase difference in the two phasor sets is about 5°. For larger angular difference, the machine would get a current and torque jolt and may not *synchronise* (falls out of step). Instead of lamps, an instrument called *synchroscope* is employed in generating stations. Instrumentation schemes have been devised for complete autosynchronisation.

The machine after synchronisation would act as a generator or motor depending upon the mechanical conditions at its shaft.

It is immediately obvious from the above that to start a synchronous motor, a small pilot motor (induction type) must be coupled to it to bring it to the speed for synchronisation.

Damper Winding

Springlike synchronous link along with rotor inertia results in oscillations, called *hunting*, initiated by disturbances of the electrical or mechanical sides of the machine. These oscillations are very undesirable electrically and would also fatigue the shaft. These are damped out by providing short-circuited copper bars, known as damper or *amortisseur winding*, placed in the rotor pole faces. The damper winding, because of induced currents when the rotor oscillates w.r.t. the rotating field, produces the desired damping effect (damper torque always opposes the oscillatory movement).

Induced currents in the damper winding when the stator is switched on to the supply provide the starting torque (induction principle) for a synchronous motor. The field is switched on after the rotor reaches close to synchronous speed. Such an induction start synchronous motor is known as *synduction motor*.

8.8 OPERATING CHARACTERISTICS

Power-angle Characteristic

With reference to the circuit model of Fig. 8.27.

$$\bar{E}_f = \bar{V}_t - jX_s \bar{I}_a \text{ ; generating mode} \tag{8.33a}$$

$$\bar{E}_f = \bar{V}_t + jX_s \bar{I}_a \text{ ; motoring mode} \tag{8.33b}$$

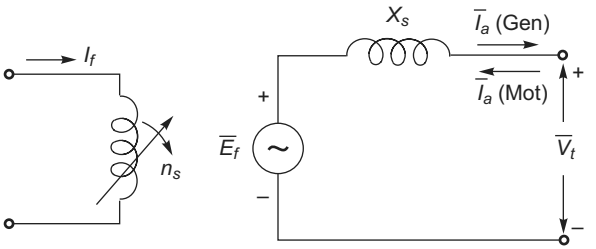


Fig. 8.27 *Synchronous machine—generating/motoring modes*

The phasor diagrams for the two modes as per Eqs (8.33a) and (8.33b) are drawn in Figs 8.28(a) and (b). It is easily seen from these figures that

$\bar{E}_f$ leads $\bar{V}_t$ by angle δ in generating mode

$\bar{E}_f$ lags $\bar{V}_t$ by angle δ in motoring mode

It easily follows from the geometry of the phasor diagrams of Figs 8.28(a) and (b) that

$$PN = I_a X_s \cos\theta = E_f \sin\delta \tag{8.34}$$

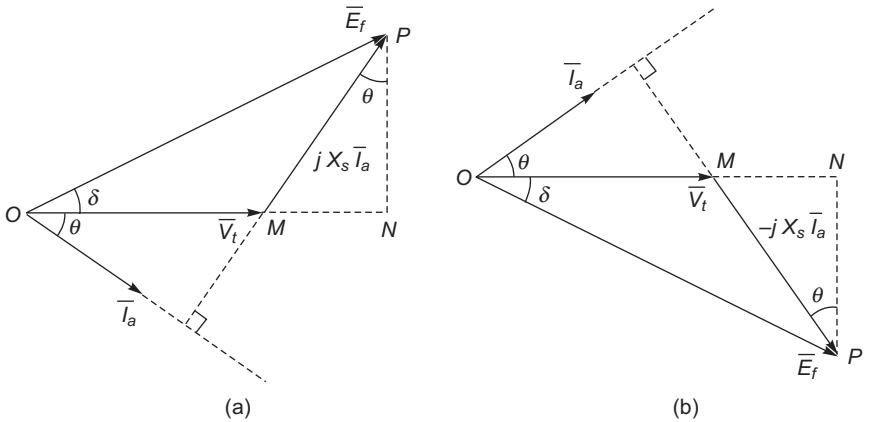


Fig. 8.28 *Synchronous machine phasor diagram; constant excitation, variable load (a) Generating mode-lagging pf, (b) Motoring mode-leading pf*

Multiplying Eq. (8.34) by V_t on both sides and manipulating

$$V_t I_a \cos\theta = \frac{V_t E_f}{X_s} \sin\delta \tag{8.35}$$

or

$$P_e = \frac{V_t E_f}{X_s} \sin\delta \tag{8.36}$$

where $P_e = V_t I_a \cos\theta$

= electrical power delivered to/drawn from mains

δ = angle by which E_f leads/lags V_t and is called the *power* (or *torque*) *angle*

This angle takes into account the leakage reactance of the machine but notice the similarity in form.

The plot of Eq. (8.36) drawn in Fig. 8.29 is known as the power-angle characteristic. The motoring region of the machine has negative δ with the machine drawing electrical power and delivering mechanical power. For a given V_t and excitation emf E_f, δ is controlled by mechanical conditions at the shaft—positive δ when shaft power is input to the machine by a prime mover and negative δ when shaft power is drawn by a mechanical load. The machine loses synchronism for values of the electrical power demanded from a generator more than $P_{e\,\max}$, or the mechanical load on a motor is more than $P_{e\,\max}$. In case of motors, loss of synchronism is referred to as being "pulled out" of synchronism. For a machine operating at a value of δ even smaller than 90°, transient disturbances can cause it to lose synchronism. Steady value of δ is rarely allowed to exceed 30°.

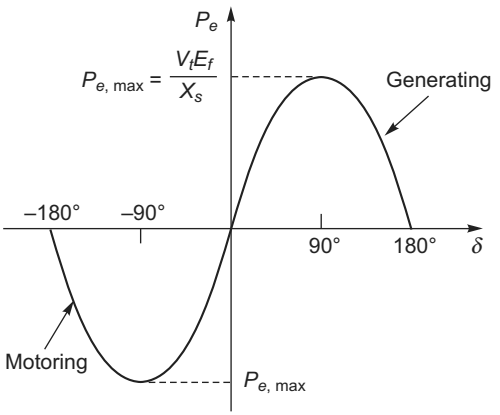


Fig. 8.29 *Power-angle characteristic*

Operation at Constant Load Variable Excitation

For this type of operation, from Eqs (8.36) and (8.35),

$$E_f \sin\delta = \frac{P_e X_s}{V_s} = \text{constant} \tag{8.37a}$$

and

$$I_a \cos\theta = \frac{P_e}{V_t} = \text{constant} \tag{8.37b}$$

The motoring-mode phasor diagram is drawn in Fig. 8.30 for unity power factor. The corresponding excitation is called *normal*. The loci of E_f and I_a are shown dotted in this figure. The cases of over-excitation and under-excitation are illustrated in Fig. 8.31 from which it can be concluded that an over-excited motor draws leading current (acts like a capacitive load) but an under-excited motor draws lagging current (acts like an inductive load).

The case of variable generating machine excitation is just the reverse. Both these cases are summarised below:

- ❑ **Over-excitation** Leading *pf* in motoring mode; lagging *pf* in generating mode
- ❑ **Under-excitation** Lagging *pf* in motoring mode; leading *pf* in generating mode

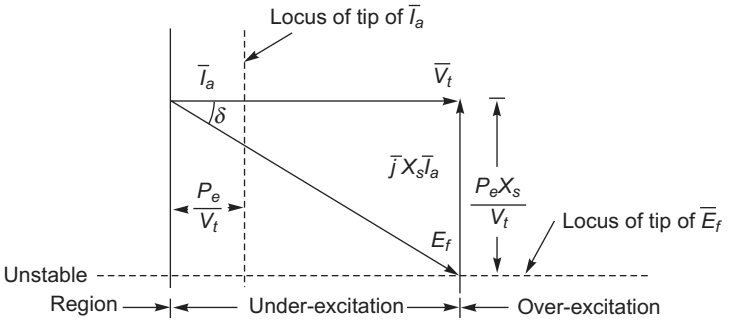


Fig. 8.30 *Motoring machine—normal excitation*

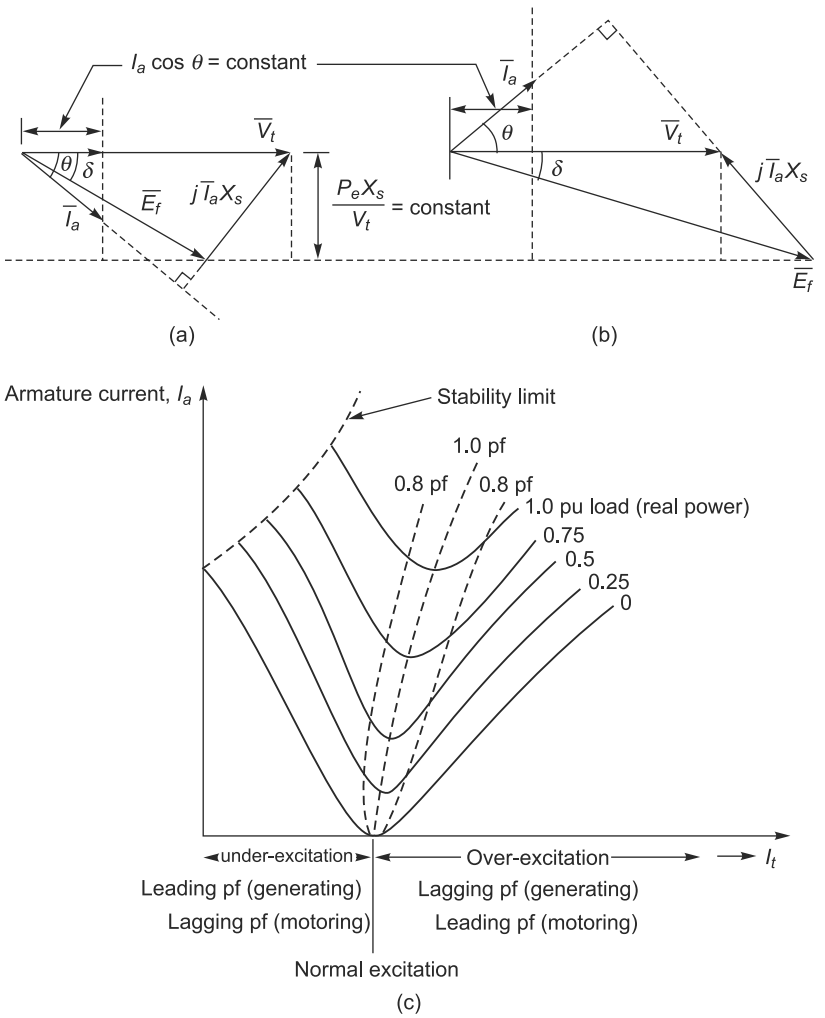


Fig. 8.31 *(a) Under-excitation (lagging current); motoring (b) Over-excitation (leading current); motoring machine (c) V-curves of synchronous machine (constant load (real power)), variable excitation*

An unloaded synchronous motor may be used as a variable condenser or inductor by varying its excitation.

The plots of the variation of armature current of a synchronous machine for constant real power load but with variable excitation are shown in Fig. 8.31(c). These are known as *V-curves*.

Example 8.4

A three-phase synchronous motor is synchronised to the mains at a terminal voltage of 12.5 kV. It has a synchronous reactance of 8.0 Ω.

Assuming the motor to be unloaded and neglecting rotational loss, draw the phasor diagram and compute the current, active and reactive power drawn from the mains, and power factor in the following two cases:

(a) The field current is raised to increase the machine excitation by 20% (over-excitation).

(b) The field current is reduced to decrease the machine excitation by 20% (under-excitation).

Note: It is to be understood that at the time of synchronisation, the machine excitation voltage is the same as the terminal voltage as the machine is just ***floating*** on the bus bars.

Solution Since motoring operation is considered, the direction of positive current is into the machine. Since the motor is on no load (also no rotational loss), power angle stays at zero; $\delta = 0$ and E_f and V_t are always in phase.

$$V_t = \frac{12.5}{\sqrt{3}} = 7.217 \text{ kV/phase}$$

At no load, $E_f = V_t = 7.217$ kV

(a) $E_f = 7.217 \times 1.2 = 8.66$ kV/phase, $V_t = 7.217$ kV (mains)

The phasor diagram is drawn in Fig. 8.32(a). Observe that $\bar{I}_a$ must lead by 90°.

Now

$$I_a = \frac{8.66 - 7.217}{8} = 0.1804 \text{ kA}$$

Phase angle $\theta = 90°$ lead

pf = 0 lead

$P_e = 0$

$$Q_e = -\sqrt{3} \times 12.5 \times 0.1804$$

$$= -3.906 \text{ kA}$$

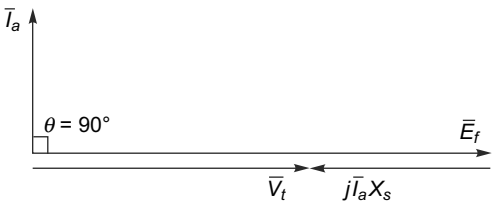


Fig. 8.32(a)

(b) $V_t = 7.217$ kV/phase

$E_f = 7.217 \times 0.8 = 5.774$ kV/phase

The phasor diagram is drawn in Fig. 8.32(b).

Observe that $\bar{I}_a$ must lag by 90°. Now,

$$I_a = \frac{7.217 - 5.774}{8} = 0.1804 \text{ kV}$$

$\theta = 90°$ lag

$p_f = 0$ lag

$P_e = 0$

$$Q_e = +\sqrt{3} \times 12.5 \times 0.1804$$

$$= +3.906 \text{ MVAR}$$

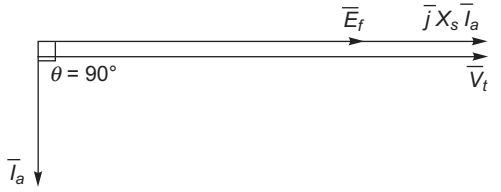


Fig. 8.32(b)

Remark: When over-excited, the motor draws –3.906 MVAR (or delivers + 3.906 MVAR to the mains) while when under-excited, it draws + 3.906 MVA (or delivers –3.906 MVA to the mains).

Example 8.5

The motor of Example 8.4 is run as a generator (it is now coupled to a prime mover) and it delivers 10 MW to the bus bars while it is over excited by 20%. Find the current, *pf* and MVAR delivered.

Solution Since the generator is delivering active power to the bus bars (10 MW), the steam the valve of the turbine must have been opened. Now,

$$P_e = 3\left(\frac{V_t E_f}{X_s}\right) \sin \delta$$

$$10 = 3 \times \left(\frac{7.217 \times 8.66}{8}\right) \sin \delta$$

or $$\delta = 25.3°$$

$$\bar{I}_a = \frac{\bar{E}_t - \bar{V}_t}{jX_s} ; \ \bar{E}_f \text{ lead } \bar{V}_t \text{ by } 253.3°$$

$$= \frac{8.66 \angle 25.3° - 7.217 \angle 0°}{j8}$$

$$= 0.4626 - j\, 0.0765 \text{ kA}$$

$$\bar{I}_a = 0.4689 \angle -9.4°$$

$$I_a = 0.4689 \text{ kA; pf} = 0.987 \text{ lag}$$

$$Q_e = +\sqrt{3} \times 12.5 \times 0.0765$$

$$= +1.656 \text{ MVAR}$$

Example 8.6

A 1000 kW, star-connected, 3.3 kV, 24-pole, 50 Hz synchronous motor has a synchronous reactance of 3.24 Ω; the resistance being negligible.

The motor is fed from infinite bus bars at 3.3 kV. It is drawing rated power at 0.9 pf leading from the bus bars. Calculate the maximum power and torque the motor can deliver while its excitation is maintained constant. Draw the phasor diagram under this condition. Find also the current, pf and reactive power drawn.

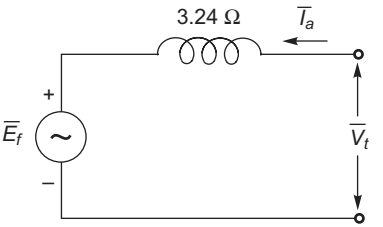


Fig. 8.33

Solution With reference to Fig. 8.33.

$$P_e \text{ (in)} = 1000 \text{ kW at 0.9 pf leading}$$

$$I_a = \frac{1000}{\sqrt{3} \times 3.33 \times 0.9} = 194.4 \text{ A}$$

$$\theta = \cos^{-1} 0.9 = 25.8°$$

or $$\bar{I}_a = 194.4 \angle 25.8°$$

$$V_t = \frac{3300}{\sqrt{3}} = 1905 \text{ V}$$

Now, $$\bar{E}_f = 1905 \angle 0° - j194.4 \angle 25.8° \times 3.24$$

$$= 2178.5 - j\, 566.9$$

$$E_f = 2252 \text{ V}$$

Under the condition, when the motor is drawing maximum power from the mains, $\bar{V}_t$, leads $\bar{E}_f$ by 90°. The phasor diagram is drawn in Fig. 8.34.

$$P_{e,\max} = 3 \times \frac{1905 \times 2252}{3024} = 3972 \text{ kW}$$

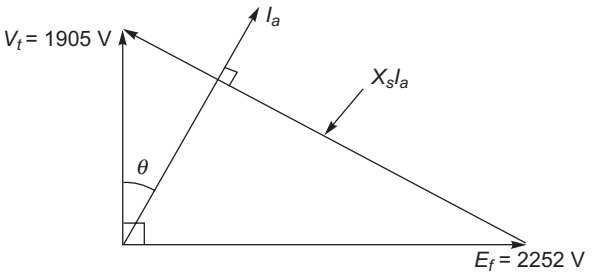


Fig. 8.34

From the phasor diagram,

$$\bar{I}_a = \frac{V_t \angle 0° - E_f \angle -90°}{jX_s}$$

$$= \frac{1905 - 2252 \angle -90°}{j3.24}$$

$$= 695.1 - j\,588 = 910 \angle -40.2°$$

$$I_a = 910 \text{ A; pf} = 0.764 \text{ lag}$$

$$Q_e = \sqrt{3} \times 3.3 \times 588$$

$$= +3361 \text{ kVAR}$$

Example 8.7

A three-phase, 25 KVA, 400 V, 4-pole, star-connected synchronous machine has X_s = 4.5 Ω/ph, the armature resistance being negligible. The machine is synchronised to a 400 V, three-phase infinite bus. Neglect rotational loss.

(a) The machine is acting as a motor delivering 20 kW of mechanical power at 0.8 leading pf. Determine the excitation emf *E* and power angle.

(b) With the load remaining constant at 20 kW, the field current is gradually reduced. What is the minimum *E* and angle beyond which the machine will fall out of step? What is the value of the armature current and power factor under this operating condition? Also, draw the phasor diagram.

Solution Refer Fig. 8.35.

(a) $P_c = P_m = 20$ kW (no losses)

$$I_a = (20 \times 1000)/(\sqrt{3} \times 400 \times 0.8)$$

$$= 36.1 \text{ A}$$

$$\therefore \quad \bar{I}_a = 36.1 \angle 36.9° \text{ A}$$

$$\bar{V}_t = (400\sqrt{3}) \angle 0° = 231 \angle 0° \text{ V}$$

$$\bar{E}_f = 231 - j4.5 \times 36.1 \times 36.9°$$

$$= 231 + j162.5 \angle -53.1°$$

$$= 375 \angle -28.7° \text{ V}$$

$$E_f \text{ (line)} = 375\sqrt{3} = 650 \text{ V}, \delta = -28.7°$$

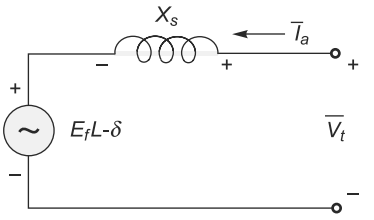


Fig. 8.35

(b) Stability limit is reached at $\delta = -90°$. Hence,

$$P = 3\left\{\frac{E_f V_t}{X_s}\right\} \sin 90° = 3\left\{\frac{E_f V_t}{X_s}\right\}$$

$$20 \times 1000 = 3\ (E_f \text{ (min) } V_t)/X_s = 3\ (E_f \text{ (min)} \times 231)/4.5$$

$$E_f \text{(min)} = 130 \text{ V} \quad \text{or} \quad 225 \text{ V(line)}, \delta = \angle -90°$$

$$\bar{I}_a = (231 + j130)/j4.5 = 28.9 - j51.3$$

$$= 58.9 \angle -60.6° \text{ A}$$

or $I_a = 58.9$ A, pf = 0.49 lagging

The phasor is drawn in Fig. 8.36.

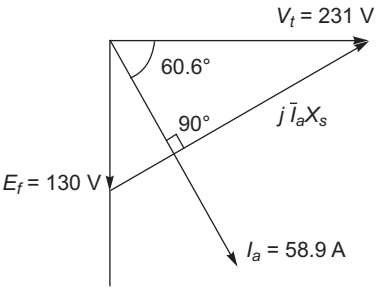


Fig. 8.36

***Remark*:** The minimum excitation limit for stability is indicated by a dotted line in the V-curves of Fig. 8.30.

Example 8.8

A three-phase hydroelectric synchronous generator is rated 110 MW, 0.8 pf lagging, 13.6 kV, Y-connected, 50 Hz, 100 rpm. Determine the

(a) number of poles,

(b) kVA rating,

(c) prime mover rating if the full-load generator efficiency is 97.1% (leave out field loss), and

(d) output torque of the prime mover.

Solution

(a) $P = (120f)/n_s = (120 \times 50)/100 = 60$

(b) $(\text{kVA})_{\text{rating}} = 110/0.8 = 137.5$

(c) $(\text{kW})_{\text{turbine}} = 110/0.971 = 113.3$

(d) $T_{\text{PM (output)}} = (113.3 \times 1000 \times 60)/(2\pi \times 100)$

$= 10.82 \times 10^3$ Nm

Example 8.9

A three-phase synchronous generator feeds into a 22 kV grid. It has a synchronous reactance of 8 Ω/phase and is delivering 12 MW and 6 MVAR into the system. Determine

(a) the phase angle of the current,

(b) the power (torque) angle, and

(c) the generated emf.

Solution

(a) $S = 12 + j\,6 = 13.42 \angle 26.6°$ kVA

Phase angle of current,

$\theta = 26.6°$ (lagging w.r.t. grid voltage)

(b) $I_a = (13.42 \times 1000)/(\sqrt{3} \times 22) = 352.2$ A

$$\bar{E}_f = (22/\sqrt{3}) \times 1000 + j8 \times 352.2 \angle -26.6°$$
$$= 13.96 + j\,2.52 = 14.18 \angle 10.2°$$

Power angle $\delta = 10.2°$ ($\bar{E}_f$ pleads $\bar{V}_t$)

(c) Generated emf = $14.18\sqrt{3} = 24.56$ kV (line)

Example 8.10

A three-phase, 10 kVA, 400V, four-pole, 50 Hz star-connected synchronous machine has negligible armature resistance and a synchronous reactance of 16 Ω/phase. The machine is operating as a generator on 400 V bus bars (assumed infinite).

(a) Determine the excitation phase emf and torque (power) angle when the machine is delivering rated kVA at 0.8 lagging pf.

(b) While supplying the same real power as in part (a), the machine excitation is increased by 20%. Find the stator current, power factor and power angle.

(c) With field current fixed as in part (a), the load (real power) on the machine is increased (by putting in more power from the prime mover) till the steady-state stability limit is reached (90°). Calculate the maximum power delivered by the machine, stator current and power factor. Draw the phasor diagram under these conditions.

Solution Refer Fig. 8.37.

(a) $\bar{I}_a = (10 \times 1000)/(\sqrt{3} \times 400) = 14.43$ A

$\theta = \cos^{-1} 0.8 = 36.9°$ lag

$\bar{I}_a = 14.43 \angle -36.9°$

$\bar{V}_t = (400/\sqrt{3}) \angle 0° = 231 \angle 0°$ V

$$\bar{E}_f = \bar{V}_t + jX_s \bar{I}_a$$
$$= 231 + j\,16 \times 14.43 \angle -36.9°$$
$$= 231 + 231 \angle 53.1°$$
$$= 413 \angle 26.4° \text{ V}$$

$E_f = 413$ V; E_f (line)

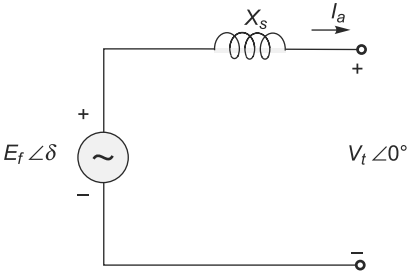


Fig. 8.37

$\delta = 26.5°$ (E_f pleads V_t)

(b) Excitation increased by 20% or $E_f = 1.2 \times 413 = 496$ V
P_e [same as in part (a)] $= 10 \times 0.8 = 8$ kW

$$\left(\frac{E_f V_t}{x_s}\right) \sin \delta = P_e$$

or $$\left(\frac{496 \times 231}{16}\right) \sin \delta = (8 \times 1000/3) \text{ (per phase)}$$

or $$\delta = 21.8°$$

$$\bar{E}_f = 496 \angle 21.8°, \bar{V}_t = 231 \angle 0°$$

$$\bar{I}_a = (\bar{E}_f - \bar{V}_t)/(jX_s) = \frac{496 \angle 8° - 231 \angle 0°}{j16}$$

$$= 31 \angle -68° \text{A}$$

$$I_a = 31 \text{ A, pf} = \cos 68° = 0.37 \text{ lagging}$$

$$\delta = 21.8°$$

(c) At steady-state power limit, $\delta = 90°$

$$P_{e,\max} = 3(\text{phase}) = \frac{413 \times 231}{16} \sin(\delta = 90°)$$

$$= 17.9 \text{ kW}$$

$$\bar{E}_f = 413 \angle 90° \text{; no change in field current}$$

$$\bar{I}_a = \frac{413 \angle 90° - 231 \angle 0°}{j16} = -\frac{231 - j413}{j16}$$

$$= 25.8 + j14.44 = 29.6 \angle 29.2° \text{ A}$$

$$\bar{I}_a = 29.6 \text{ A, pf} = \cos 29.2° = 0.873 \text{ leading}$$

The phasor diagram is drawn in Fig. 8.38.

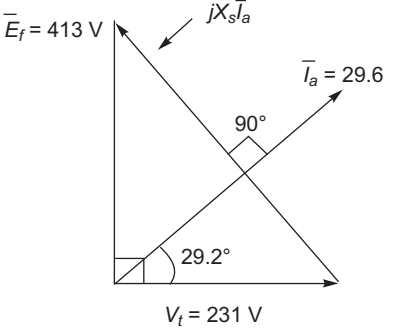


Fig. 8.38

Example 8.11

The synchronous machine of Fig. 8.24 is acting as a motor.

(a) The mechanical load on the shaft is 8 kW and the rotational losses (mechanical and iron losses) equal 0.5 kW. The machine is excited to have an excitation emf of 750 V (line). Calculate the armature current, power factor and power angle. Also, calculate the developed and shaft (load) torques. Ignore stator copper loss.

(b) The motor is on no-load and its losses can be ignored. Calculate the armature current and its power factor at an excitation emf of (i) 600 V, and (ii) 300 V. Also, calculate the kVAR drawn in each case.

(c) The motor is no-load (losses to be ignored). What should be its excitation for it to draw a leading kVAR of 6? Draw the phasor diagram.

Solution

(a) Gross mechanical load = 8 + 0.5 = 8.5 kW

P_e (in) = 8.5 kW (copper loss ignored)

$$Pe = \left(\frac{E_f V_t}{x_s}\right) \sin \delta$$

V_r = 231 V, Ef = $750/\sqrt{3}$ = 433 V

$(8.5 \times 1000)/3 = [(433 \times 231)/16] \sin \delta$

or $\delta = 27°$, ($\overline{E}_f$ lags $\overline{V}_t$)

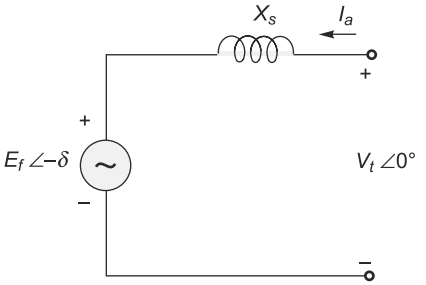


Fig. 8.39

$$\overline{I}_a = (\overline{V}_t - \overline{E}_f)/jx_s$$

$$\overline{I}_a = \left(\frac{230 \angle 0° - 433 \angle -27°}{j16}\right)$$

$= 12.3 + j8.25 = 15.66 \angle 38.2°$

$\overline{I}_a$ = 15.4 A, pf = cos 38.2° = 0.786 leading

$n_s = (120 \times 50)/4$ = 1500 rpm or 157.1 rad/s

T(dev) = 8500/157.1 = 54.1 Nm

T(shaft) = 8000/157.1 = 50.9 Nm

(b) (i) $E_f = 600/\sqrt{3} = 346$ V

On no-load with no losses, power drawn from mains is zero and so δ = 0°. Then $\overline{E}_f$ = 346 ∠ 0° V and $\overline{V}_t = 231 \angle 0°$ V (i.e. these are in phase). Now,

$\overline{I}_a = (231 - 346)/j16 = j7.19$ A = 7.19 Z∠ 90°A

$\overline{I}_a$ = 7.19 A, pf = 0, leading

kVAR (drawn) = $\sqrt{3} \times 400 \times 7.19$ = 4.98 (leading)

The motor acts like a capacitor with a per phase capacitance of

$\overline{I}_a = 2\pi f C V_L$

∴ $C = (7.19/231)/ (2\pi \times 50) = 99$ μF

(ii) $\overline{E}_f = (300/\sqrt{3}) \angle 0° = 173.2 \angle 0°$ V, $\overline{V}_t = 231 \angle 0°$

$\overline{I}_a = (231 - 173.2)/j16 = -j3.6$ A = $3.6 \angle -90°$ A

I_a = 3.6 A, pf = 0 (lagging)

kVAR (drawn) = $\sqrt{3} \times 400 \times 3.6$ = 2.49 (lagging)

The motor acts like an inductor with a per phase inductance of

$V_t = 2\pi f L I_a$

$$L = (231/3.6)/(2\pi \times 50) = 204 \text{ mH}$$

(c) kVAR (drawn) = 6, leading

$$6000 = \sqrt{3} \times 400 \times I_a$$

or $$\bar{I}_a = 8.66\,A \text{, zero leading pf}$$

$$I_a = (230 - E_f)\,/j16 = j8.66$$

or $$E_f = 368.6 \text{ V or } 640 \text{ V (line)}$$

The phasor diagram is drawn in Fig. 8.40.

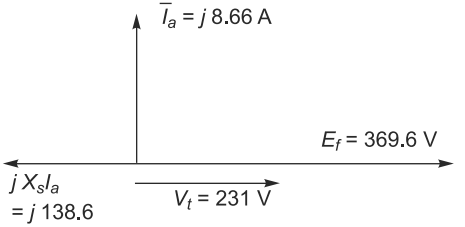


Fig. 8.40

Example 8.12

A 1000 kV A, 6.6 kV, three-phase star-connected synchronous generator has a synchronous reactance of 25 Ω, per phase. It supplies full-load current at 0.8 lagging power factor at rated terminal voltage. Compute the terminal voltage for the same excitation when the generator supplies full-load current at 0.8 leading power factor.

Solution

$$I_a(\text{rated}) = \frac{1000}{\sqrt{3} \times 66} = 87.5 \text{ A}$$

$$V_t \text{ (phase)} = \frac{6600}{\sqrt{3}} = 3810 \text{ V}$$

Operation at full-load 0.8 pf lag, rated voltage:

$$\bar{E}_f = \bar{V}_t + j X_s \bar{I}_a$$

$$= 3810 \angle 0° + j25 \times 87.5(0.8 - j0.6)$$

$$5123 + \text{j}1750 = 5413 \angle 18.8°$$

$$E_f = 5414 \text{ V}$$

Operation at full-load 0.8 pf lead, rated voltage, no change in excitation:

$$E_f = 5413 \text{ V}, I_a = 87.5 \text{ A}$$

I_a leads V_t by angle $\cos^{-1} 0.8 = 36.9°$

$$V_t \angle 0° = \bar{E}_f - j X_s \bar{I}_a$$

V_t and angle of E_f are unknown. It is easier to proceed from the phasor diagram drawn in Fig. 8.41.

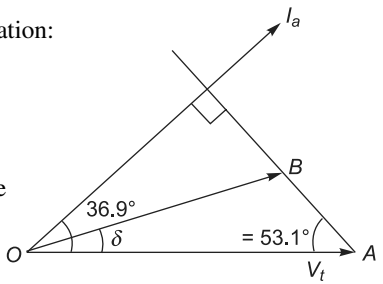


Fig. 8.41

For Δ OAB,

$$OB = E_f = 5413 \text{ V}$$

$$AB = X_s I_a = 87.5 \times 25 = 2187.5 \text{ V}$$

$$\frac{5414}{\sin 53.1°} = \frac{2187.5}{\sin \delta}$$

or $$\sin \delta = 0.323,\ \delta = 18.8°$$

$$\angle OBA = 180° - 53.1° - 18.8° = 108.1°$$

$$\frac{V_t}{\sin 108.1°} = \frac{218.5}{0.323}$$

Or $V_t = 6437$ V (phase) or

8.15 kV(line)

Observation $V_t > E_f$ because of leading current

Example 8.13

A 40 kV, 600 V, three-phase, star-connected synchronous machine has a synchronous reactance of 8 Ω and negligible resistance. When excited to a 'per phase' emf of 600 V and synchronised to 600 V main, it carries an armature current of 40 A. Find its power input/output and power factor when operating as (a) a generator, and (b) motor. Also, draw the phasor diagrams for both operations.

Solution The circuit diagram as per phase basis is drawn in Fig. 8.42(a). Terminal voltage, $V_t = 600/\sqrt{3} = 346$ V (phase)

Excitation emf, $E_f = 600$ V (phase)

(a) *When operating as a generator*

$\bar{E}_f$ leads $\bar{V}_t$ by angle δ

$$\bar{V}_t = 346 \angle 0°, \bar{E}_f = 600 \angle \delta$$

Armature current

$$I_a = \left| \frac{600 \angle \delta - 346}{j8} \right| = 40 \text{ A} \quad \text{(i)}$$

or $$\left| \frac{\cos\delta + j\sin\delta - 346/600}{j} \right| = \frac{8 \times 40}{600}$$

or $$|\sin\delta - j(\cos\delta - 0.577)| = 0.533$$

or $$\sin^2\delta + (\cos\delta - 0.577)^2 = (0.533)^2 = 0.284$$

$$1 - 2 \times 0.577 \cos\delta + 0.333 = 0.284$$

From which we get

$\cos\delta = 0.91$, $\delta = 24.6°$

$$\angle \bar{I}_a = \theta = -\tan^{-1}\left[\frac{\cos\delta - 0.577}{\sin\delta}\right] = -38.6°$$

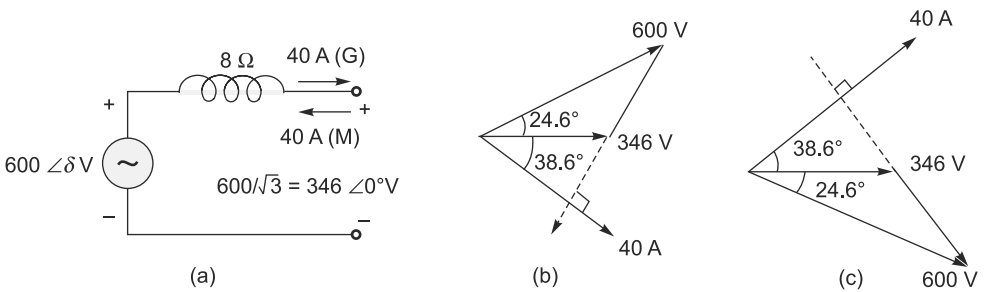


Fig. 8.42

$$\text{pf} = \cos 38.6 = 0.78 \text{ lag}$$

$$P \text{ (out)} = \sqrt{3} \times 600 \times 0.78 \times 10^{-3} = 32.5 \text{ kW}$$

The phasor diagram is drawn in Fig. 8.42(b).

(b) *When operating as a motor*

Same V_t, E_f and I_a (in)

$$I_a = \left[\frac{346 \angle 0 - E_f \angle -\delta}{j8}\right] = 40 \quad \text{(ii)}$$

This is the same equation as Eq. (i) except for a minus sign within the absolute values, which makes no difference. So

$$\delta = 24.6°, \ \theta = +38.6° \text{ (reversal in sign)}$$

$$\text{pf} = \cos 38.6° = 0.78 \text{ lead}$$

$$P \text{ (in)} = 32.5 \text{ kW}$$

The phasor diagram is drawn in Fig. 8.42(c).

Example 8.14

A synchronous motor is drawing 50 A from a 400 V, three-phase supply at unity pf with a field current of 0.9 A. The synchronous reactance is 1.3 Ω.

(a) Find the power angle δ.

(b) Assuming no change in mechanical load, find the value of the field current, which would result in a power factor of 0.8 leading. The magnetising characteristic may be taken as linear.

Solution

$$V_t = \frac{400}{\sqrt{3}} = 231 \text{ V reference phasor}$$

$$I_a = 50 \text{ A pf unity}, \ \theta = 0°$$

$\bar{I}_a$ is in phase with $\bar{V}_t$

(a) Excitation emf

$$\bar{E}_f = 231 - j\,1.3 \times 50 = 231 - j65$$

$$= 240 \angle -15.7°$$

$\bar{E}_f$ lags $\bar{V}_t$ by $\delta = 15.7°$ (motoring action)

(b) Assuming no loss

$$P \text{ (mech)} = P \text{ (elect)} = \sqrt{3} \times 400 \times 50 \times 10^{-3} = 34.64 \text{ kW}$$

As there is no change in mechanical power output, so

$$P \text{ (elect)} = 34.64 \times 10^3 = \sqrt{3} \times 400 \, I_a \times 0.8; \ pf = 0.3 \text{ leading } \phi = +36.9°$$

$$I_a = 62.5$$

$$\bar{I}_a = 62.5 \angle 36.9°$$

Now,

$$\bar{E}_f = 231 - j1.3 \times 62.5 \angle 36.9°$$

$$= 231 - 1.3 \times 62.5 \angle 126.9°$$

$$= 231 - (-48.8 + j\,65)$$

$$= 278.8 - j\,65 = 28.3 \angle -13°$$

It increases proportionally. Thus

$$\text{If} = 0.9 \times \frac{287.3}{240} = 1.08 \text{ A}$$

Example 8.15

A 1 MVA, 3 kV, three-phase, 1.2-pole, star-connected synchronous motor is connected to an infinite bus. The motor reactance of 0.8 pu. All losses are to be ignored. This is operating at 0.85 leading pf and is delivering 750 kW of mechanical power.

(a) Determine the value of E_f.

(b) With the value of E_f as found in part (a) remaining fixed, determine the maximum power and torque the motor can deliver.

(c) While delivering the load of 750 kW, the excitation emf E_f is reduced by reducing the field current. Determine the minimum value of E_f when the motor will fall out of step. What is the corresponding armature current and the pf? Draw the phasor diagram.

Solution

$$X_s(\text{pu}) = 0.8 \times \frac{X_s(\Omega) \times (\text{MVA})_B}{(\text{kV})_B^2} = \frac{X_s(\Omega) \times 1}{(3)2}$$

or $$X_s = 0.8 \times 9 = 7.2\ \Omega$$

(a) Refer to adjoining figure,

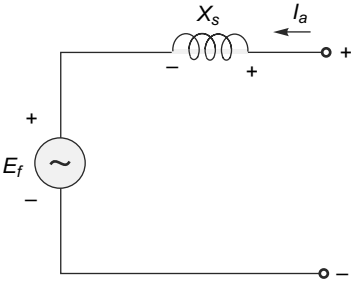


Fig. 8.43

$$\bar{V}_t = \frac{3}{\sqrt{3}} = \sqrt{3} \times \angle 0° \text{ kV} = 1732 \angle 0° \text{ V}$$

$$P_e = P_m = 750 \text{ kW, no loss assumed}$$

$$\text{pf} = 0.85,\ \phi = 31.8° \text{ lag}$$

$$I_a = \frac{750}{0.08\sqrt{3} \times 3} = 180 \text{ A}, \bar{I}_a = 180.4 \angle -318°$$

From the figure,

$$\bar{E}_f = \bar{V}_t - j X_s \bar{I}_a$$

$$= 1723 - j\,7.2 \times 180.4 \angle -31.8°$$

$$= 1048 - j\,1104$$

$$\bar{E}_f = 1522 \angle -46.5° \text{ (phase)}$$

$$E_f = 2636 \text{ V (line)}$$

$$P(\text{max}) = \frac{3 V_t E_f}{X_s} = \frac{3 \times 1732 \times 1522 \times 10^{-3}}{7.2}$$

$$= 1098 \text{ kW}$$

$$n_s = \frac{120 \times 50}{12} = 500 \text{ rpm or } 52.36 \text{ rad (mech)/s}$$

$$T(\max) = \frac{1098 \times 10^3}{52.36} = 20015 \text{ Nm}$$

(c) For fixed power, E_f is minimum when $\delta = 90°$.

$$\frac{750}{3} \times 10^3 = \frac{1732 \times E_f}{7.2}$$

or $E_f(\min) = 1039$ V (phase)

$= 1.8$ kV (line)

From the figure,

$$\bar{I}_a = \frac{1732 - (-j1039)}{j7.2} = \frac{1039 - j1732}{7.2}$$

$$= (144.3 - j240.5) = 280.5 \angle -59° \text{ A}$$

pf = cos 59° = 0.515 lag

Phasor diagram:

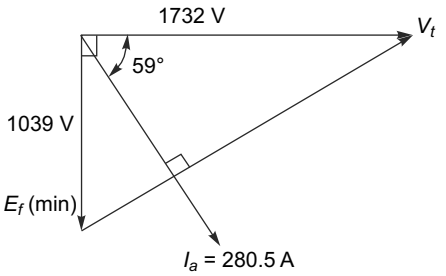


Fig. 8.44

Summary

➢ **Constructional features of electric machines**

Rotating electric machines have two flux-carrying parts, which are made of laminated silicon steel. These two are the following:

Stator—A stationary annular cylinder.

Rotor—Rotates within the stator supported by a shaft, ball bearings and end rings bolted to the stator. There is a narrow *air-gap* between the stator and rotor.

Windings—There are two windings made of copper. These are placed in stator and rotor slots or in one of these wound on projecting poles. In *synchronous machines*, the main field is created by the field poles (even in number) and dc excited. The other winding which interchanges electric power with the external circuit and so carries the *load current* is called the *armature winding* and in the *seat of induced* emf.

In a synchronous machine, the field poles on the rotor and armature winding on the stator, is the preferred construction universally adopted. Excitation current is provided to the field poles through slip ring brush arrangement.

➢ **Field pole types**
Salient or projecting poles, nonsalient or cylindrical poles.

➢ **Induced ac emf** in rotating machines. It is the speed emf. The relative motion between *B*-wave and coils, which causes change in flux linkage and emf *induction*.

➢ **Mechanical and electrical angles**

$\frac{\theta_e}{\theta_m} = \frac{2}{P}$; P = number of pole

➢ **Speed-poles-frequency**

$n = \frac{120 f}{p}$ synchronous speed in rpm

or $f = \frac{nP}{120}$ Hz

➢ **Armature Coils**
Could be single-turn or multi-turn with two-end connection.
Coil-side—Each active side of a coil

➢ **Coil span (pitch)**
- Full-pitched—angle between coil sides is π rad or 180° electrical
- Short-pitched—angle between coil sides is less than π in terms of number of slots

➢ Two-layer windings—two coil sides per slot

➢ Induced emf of a single *N* turn full-pitch coil

$E\ (rms) = \sqrt{2}\,\pi\, f\, N\, \Phi = 4.44\, f\, N\, \Phi$

Φ = *flux/pole*

Induced emf phasor lags the flux phasor by 90°

➢ **Distributed winding**—More than one coil/phase

Slots/pole/phase, $SPP = m = \frac{S}{qp}$; S = slots, q = number of phases, generally three

Slot angle, $\gamma = \frac{\pi P}{S}$ rad (elec.)

Phase spread, $\sigma = m\gamma$

➢ **Breadth factor, K_b**
Because of distributed winding, the phase emf is less than the algebraic sum of series turns/phase by the breadth factor

$K_b = \frac{\sin m\gamma/2}{m \sin \gamma/2} < 1$

K_b (harmonics) < K_b (fundamental)

Therefore, distributed winding incidentally reduces the harmonic content of emf induced.

➢ **Short-pitched (corded) coils**

The emf of a short-pitched coil is less than that for a full-pitched coil by the pitch factor

$K_P = \cos\frac{\beta}{2} < 1$; β = short-pitching angle in radians elect.

➢ Chording of coil saves in overhang copper by proper choice of β any particular harmonic can be eliminated.

➢ **Winding factor**

$K_w = K_b K_p < 1$

➢ **General formula for induced emf/phase**

$E_p = \sqrt{2}\,\pi\, K_w\, f\, N_{ph}\,(series)\,\Phi V$

➢ **MMF of ac winding**

A single coil produces rectangular mmf wave (with north and south poles, strength ($Ni/2$)

Fundamental wwf wave

$F_{a1} = \frac{4}{\pi}(Ni/2)\cos\theta$, θ = space angle elect.

For sinusoidal current ($i_a = \sqrt{2}\, I\cos\omega t$)

$F_{a1} = \sqrt{2}\, K'I\cos\omega t\cos\theta$

$= F_m \cos\,\omega t\,\cos\,\theta$

It is a standing pulsating wave.

For a distributed winding,

$$F_{a1} = \frac{4\sqrt{2}}{\pi} K_w \left(\frac{N_{ph}(series)}{P}\right) I\cos\,\omega t\,\theta$$

$= F_m \cos\,\omega t\,\cos\,\theta$

➢ **Rotating magnetic field**

A three-phase winding with their axis located at 120° elect, *phase difference* from each other are fed with three-phase balanced currents with a *time difference of 120° elect*, from each other, the resultant mmf wave and its associated B-wave rotates at synchronous speed $\omega_s = 2\pi f$ rad (elect)/s (or n_s = 120 rpm). The direction of rotation of mmf wave from the leading phase current to the lagging phase current. The number of poles of the mmf wave is same as that for which the winding is wound.

➢ **Torque in round rotor machine**

Necessary conditions for production of steady torque by two interacting magnetic fields:

1. The two fields must be relatively stationary.
2. The two field must have the same number of poles.

Torque expression

F_1, F_2 are peak values of sinusoidally distributed fields rotating at synchronous speed and F_r, the resultant field.

Torque, $T = K\, F_1\, F_2 \sin\lambda$; λ = angle between F_1 and F_2

$= KF_rF_2 \sin\delta$; δ = angle between F_r and F_2

It is F_r that produces the *air-gap flux*, Φ_r/ pole

➢ **Synchronous machine**
Generating—F_2 leads F_r by angle δ. Electromagnetic torque $T = T_{PM}$ in same direction speed synchronous.

Motoring—F_2 lags F_r by angle δ. Electromagnetic torque $T = T_L$ (load torque) in same direction speed synchronous.

Nonself-starting—Terminal voltage (equal to induced emf)

V(line) = $\sqrt{3} \times 4.44\ K_w f N_{ph}$ (series)

For fixed terminal voltage, Φ_r is constant; same as in a transformer. Therefore,

$T = K_T \sin \delta$

Pullout torque, $T_{max} = K_T$, $\delta = 90^\circ$

Higher torque load causes *loss of synchronism* or the machine *pullout*.

➢ Synchronous speed, $n_s = \dfrac{120 f}{P}$ rpm, $\omega_s = \dfrac{4\pi f}{P}$ rad (mech)/s; in general $n_s = \dfrac{60}{2\pi}\omega$

➢ Excitation emf (E_f) is the emf induced in the armature winding due to field current (I_f) only. At no-load, $E_f = V_t$ (terminal voltage)

➢ Synchronous generator ($\bar{I}_a$ in the direction of $\bar{E}_f$)

(i) When I_a lags E_f by 90°, the *armature reaction field* $\bar{F}_a$ is demagnetising. It is in direct opposition to the rotor field $\bar{F}_f$.

(ii) I_a in phase with E_f, $\bar{F}_a$ is cross-magnetising, at 90° to $\bar{F}_f$.

(iii) I_a leads E_f by 90°, $\bar{F}_a$ is magnetising in the same direction as $\bar{F}_f$.

In a synchronous motor, the direction of $\bar{I}_a$ reverses and so do the conclusions (i) and (ii) above interchange magnetising and de-magenetising.

➢ The armature reaction effects can be simulated by an armature reactance X_a in series with $\bar{I}_f$. Further, X_a when combined with armature, leakage reactance is called the *synchronous reactance* $X_s = X_a + X_l$) of the machine. Its value is of the order of 0.5 to 1 pu; far larger than in a transformer.

➢ *OCC*—Open Circuit-Characteristic–plot of V_{oc} (line) vs I_f. It is the magnetisatic characteristic of the machine. A line from the origin tangential to the linear part of *OCC* is called the *air-gap line*.

➢ *SCC*—Short-Circuit Characteristic–plot of short-circuit current I_{SC} vs I_f; it is linear as I_f is very small.

➢ Determination of synchronous reactance X_s from *OCC* and *SCC*

X_s (unsaturated) = $\left| \dfrac{V_{OC}/\sqrt{3}}{I_{sc}} \right|$ at any point on air gap line

X_s (adjusted) = $\left| \dfrac{V_{OC}/\sqrt{3}}{I_{sc}} \right|$ I_f corresponding to V_f (rated) on *OCC*

➢ Voltage regulation = $\left| \dfrac{V_t(\text{no load})\big|_{I_f \text{ same as at full load}} - V_t(\text{rated})}{V_t(\text{rated})} \right|$ specified pf

- ➢ Circuit model (equivalent circuit) of the synchronous machine—armature resistance negligible
- ➢ **Governing equations**

  Generating

  $$\bar{V}_t = \bar{E}_f - jX_s I_a$$

  $\bar{E}_f$ lead $\bar{V}_t$ by angle δ

  Motoring

  $$\bar{V}_t = \bar{E}_f - jX_s I_a$$

  $\bar{E}_f$ lag $\bar{V}_t$ by angle δ

- ➢ Starting—synchronous motor is non self-starting, started by an auxiliary motor (induction motor) and then synchronised to mains.

  Before loading, it is *floating* on the mains; drawing or delivering almost zero current.

- ➢ **Operating characteristic**

  $$P_e = \frac{V_t E_f}{X_s} \sin \delta$$; power-angle characteristic

  where $P_e = V_t I_a \cos \theta$; $\cos \theta = pf$

  $$P_e(\text{max}) = \frac{V_t E_f}{X_s}$$

  If $P_e > P_e$ (max), the machine loses synchronism or motor falls out of step.

- ➢ Fixed load variable excitation:

  I_f controls the power factor

  Normal excitation—unity power factor.
  Over-excitation—Leading pf in motoring mode; lagging pf in generating mode.
  Under-excitation—Lagging pf in motoring mode; leading pf in generating mode.

Exercises

Review Questions

1. What measures are adopted to make the *B*-wave in a synchronous machine nearly sinusoidal? Why should the *B*-wave be sinusoidal?
2. A synchronous machine has *P* poles and generates voltage of frequency *f* Hz. Write the expressions for its speed in rad (elect)/s, rad (mech)/s and rpm.
3. Explain the terms coil span, coil pitch, short-pitching and cording of coils.
4. What is SPP? Write its expressions for a stator having *S* slots and *P* poles.
5. In a distributed winding, why is the phase emf less than the algebraic sum of phase coils in series?
6. Derive the expression for the breadth factor by means of a phasor diagram.
7. Repeat Question 6 for the pitch factor.
8. What is the purpose of using short-pitched coils in ac windings?
9. Write the expression for phasor emf in a synchronous machine. Use standard symbol and explain what each symbol stands for.

10. Taking the B-wave to be sinusoidal, derive the expression for flux/pole.
11. Write the expression for flux linkages of an N-turn coil if the B-wave is sinusoidal and rotating at synchronous speed ω rad/s.
12. Draw the phasor diagram relating emf phasor to flux phasor.
13. Sketch the mmf wave of an N-turn coil carrying current i. Write the expression for its fundamental if i is sinusoidal. What kind of wave is this?
14. Write the expression for standing pulsating space wave and sketch it at $\omega t = 0, \frac{\pi}{3}, \frac{2\pi}{3}$ and π rad.
15. Relate the peak value of a rotating magnetic field and the maximum value of the fundamental of the mmf space wave of one phase.
16. State the conditions for a three-phase winding of a stator to create a rotating magnetic field and its speed and direction of rotation.
17. State the conditions for two interacting rotating fields to create steady torque.
18. Two interacting fields $\vec{F}_1$ and $\vec{F}_2$ have a resultant field $\vec{F}_r$. Write the expression for torque developed in terms of $\vec{F}_2$ and $\vec{F}_r$. Explain the significance of the angle between them.
19. Write the expression for stator line voltage of a synchronous machine and show that it determines the air-gap flux/pole of the machine.
20. What is the pull-out torque of a synchronous machine and the meaning of loss of synchronism?
21. Explain the reason why a synchronous motor is not self-starting.
22. Distinguish between time phase difference and space phase difference.
23. State the condition of maximum efficiency of an electric machine. Compare it with that of a transformer.
24. When a conducting coil is moving past a sinusoidal flux-wave, what is the relative position of the coil axis when the induced emf in it is (a) maximum, and (b) zero?
25. Draw a suitable diagram indicating armature currents directions and field poles to show that for a motoring machine drawing 90° leading current, the armature reaction is demagnetising.
26. In Question 1, if the armature current is 45° leading, show that the armature reaction is both demagnetising and cross magnetising. A synchronous generator is supplying zero power factor (a) lagging, and (b) leading current. Show that the terminal voltage V_t and the excitation emf E_f are in phase.
27. In a synchronous motor drawing leading current at pf = cos θ, draw the phasor diagram. Find therefrom the phase and magnitude relationships between V_t and E_f. Here phase relationship means lag/lead and magnitude relationship means greater than/less than.
28. Show that in a generating synchronous machine, the phase relationship (lag/lead) between V_t and E_f is independent of the power factor (lag/lead). Draw the phasor diagrams to discover your answer.
29. In a generating synchronous machine connected to infinite bus, the mechanical power input is maintained constant, while its field current is increased from a low to a high value. Draw the phasor diagram to show how the magnitude of the armature current will change. Make a sketch of I_a vs I_f.
30. A synchronous motor with terminal voltage V_t is drawing zero pf current. Write the phasor expression for the excitation emf, E_f. Is E_f more or less than V_t magnitude-wise? What is the value of the power angle?
31. Explain what is meant by the armature reactance and synchronous reactance of a synchronous machine.
32. Explain what is the air-gap line.
33. Explain why the SCC is linear.
34. Distinguish between X_s (unsaturated) and X_x (saturated). Which one should be used for higher accuracy in predicting the voltage regulation of a synchronous generator?
35. Under what conditions does the voltage regulation of a synchronous generator become negative? Draw the phasor diagram in support of your answer.
36. Explain briefly the process of synchronising a synchronous motor to the bus-bars. What conditions determine the instant of synchronisation?

37. What is meant by the statement that a synchronous machine is 'floating' on the bus-bars?
38. Elaborate the statement that an unloaded synchronous motor can be made to act as a capacitor or as an inductor.

Problems

1. Determine breadth and pitch factor for three-phase winding with 3 slots/pole/phase. The coil span is 8 slot pitches.
2. A three-phase, 20-pole synchronous generator has a star-connected winding with 180 slots and 8 conductors/slot. The flux/pole is 0.05 Wb (sinusoidally distributed) and the speed is 300 rpm. Find the frequency and the line-to-line induced emf. The total turns/phase may be assumed to be series connected. Also, assume the stator winding to be full-pitched.
3. A three-phase, 50 Hz, star-connected synchronous generator with double-layer winding runs at 750 rpm. It has 8 turns/coil and 4 slots/pole/phase with a coil pitch of 11 slots. If the flux/pole is 0.05 Wb, find the line emf induced. Assume that the total turns/phase are connected in two series circuits connected in parallel. If each turn can carry 10 A, what is the permissible phase current and the machine kVA?
4. A 50 Hz, salient-pole synchronous generator has 288 stator slots with 8 conductor/slot and the rotor is driven at 250 rpm. Full-pitch coils are used. The mean air-gap diameter is 3.2 m and the stator length is 0.8 m. The peak value of sinusoidally distributed flux density wave is 1.2 T. Permissible conductor current is 10 A.
   (a) Calculate the rms voltage that can be induced by connecting all the turns in series (single phase). Also, find the machine kVA.
   (b) Find the per phase rms voltage and machine kVA when all the turns are series connected in three-phase.
   Comment upon the results of parts (a) and (b).

   Hint: $B_{av} = \frac{2}{\pi} B_{peak}$
5. A 2-pole synchronous generator has a frequency of 50 Hz. The stator has 24 slots with 2 conductors/slot and a permissible conductor current of 8 A. Armature winding has full-pitch coils. The flux/pole is 2.2 Wb. Compute the rms value of the generator emf (line) and machine kVA capacity if the stator winding is connected as (a) a single-phase winding with all coils in series, (b) a 2-phase winding, and (c) a three-phase winding.
6. Sinusoidally distributed mmf along the air-gap of a round-rotor machine has peak value of F_r. The machine dimensions are
   P = poles, D = mean air-gap diameter
   l = axial length of stator, g = air-gap length
   The flux/pole in the air-gap set up by this mmf can be expressed as
   $$\Phi_r = P\Phi_r$$
   where P is the effective permeance pole.
   Derive the expression for P.
7. A 2-pole synchronous motor fed from 50 Hz mains is coupled to a synchronous generator. What should be the number of poles of the generator for it to generate a voltage of 400 Hz?
8. An induction motor runs at no-load and full-load speeds respectively of 990 and 950 rpm when fed from a 50 Hz, three-phase mains.
   (a) What is the number of poles of the motor?
   (b) Calculate motor slip at no load and full load. Also, calculate the frequency of rotor currents under these two conditions.
   (c) Calculate at both no-load and full load the speed of the rotor field w.r.t. the rotor surface, with the stator field and that w.r.t. to the stator.

9. A slip-ring induction motor runs at 960 rpm on full load when connected to 50 Hz main. Calculate
   (a) slip,
   (b) number of poles, and
   (c) slip and speed at full-load with the rotor resistance doubled. Assume the rotor leakage reactance to be negligible at slip frequency.
10. Draw the phasor diagram for a motoring synchronous machine.
    (*Hint:* With reference to Fig. 8.1 $\mathbf{F}_a$ would be in phase with $-\mathbf{I}_a$ (motor)).
11. Redraw Figs 8.12 and 8.13 for a generating synchronous machine.
12. A 62 kVA, 400 V, 50 Hz, three-phase generator has the magnetisation characteristic data as given below:

V_{OC}(line$V$)	160	320	400	454	520	580	612
$I_f(A)$	2	4	5	6	7.5	10	12

    It has a synchronous reactance of 1.08 Ω/phase while the armature resistance is negligible.
    The load in the generator is raised from no-load to 125% full load, pf 0.8 lagging, with its terminal voltage held constant at rated value. Determine the range through which the field current will have to be adjusted in this operation.
13. A 400 V, three-phase, star-connected synchronous motor has a synchronous reactance of 6.1 Ω/phase. For an armature current of 25 A, find the excitation emf for the pf to be (a) unity, and (b) 0.8 leading. Calculate also the active and reactive power input in each case.
14. A three-phase synchronous generator operates into a grid of 11 kV. The synchronous reactance of the generator is 4.2 Ω/phase. The generator is excited to have an emf equal in magnitude to the bus voltage. The machine is delivering 15 MW into the grid. Find
    (a) the power angle δ,
    (b) the line current and pf, and
    (c) the reactive power delivered to the bus.
15. A star-connected, three-phase, 4-pole, 50 Hz, 12.5 kV, synchronous motor has an armature resistance of 2 Ω/phase and a synchronous reactance of 48 Ω per phase. It is drawing electric power of 1050 kW from the supply. The field current is adjusted so that the motor draws a leading current of 60 A.
    (a) At what pf is the motor operating?
    (b) Calculate its excitation emf,
    (c) mechanical torque developed, and
    (d) the armature current and power factor if the load on the motor is thrown off with excitation remaining unchanged. Ignore armature resistance in this case.
16. A three-phase, 4-pole, 50 Hz, star-connected synchronous motor has a synchronous reactance of 120 Ω/phase. The excitation is such as to give an open-circuit voltage of 13.2 kV. The motor is connected to 8.5 kV, 50 Hz supply. What maximum load can the motor supply before losing synchronism? What is the corresponding motor torque, line current and power factor?
17. A 22 kV, three-phase, star-connected turbogenerator with a synchronous reactance of 1.5 Ω/phase is delivering 200 MW to the grid at 22 kV, unity pf. With the turbine power kept constant, the machine excitation is increased by 15%. Assuming linear magnetisation characteristic, calculate the machine current and power factor. At the new excitation, the turbine power is now increased gradually to 250 MW. Calculate once again the machine current and power factor.
18. A 3.3 kV, star-connected synchronous motor has a synchronous reactance of 5.5 Ω. It operates at rated terminal voltage and draws 750 kW from the supply at 0.8 leading pf. Calculate its pf when the motor shaft load is 1000 kW with the same excitation.
19. A 1000 kVA, three-phase, 22 kV, star-connected synchronous motor has a synchronous reactance of 250 Ω/phase.
    (a) Calculate the excitation emf and pf at rated current (leading), if power angle is 15°.
    (b) What is the minimum excitation emf for the motor to deliver 800 kW without losing synchronism?

What is the corresponding line current and power factor?
Assume supply voltage to be 22 kV.

Multiple-Choice Questions

1. Synchronous reactance X_S (unsaturated) is obtained as

V_{OC} = open-circuit voltage (line)
I_{SC} = short-circuit current (line)
I_f = field current

(a) $\left.\dfrac{V_{OC}}{I_{SC}}\right|_{I_f}$ (rated)

(b) $\left|\dfrac{V_{OC}}{I_{SC}}\right|$ any 1f

(c) $\left|\dfrac{V_{OC}/\sqrt{3}}{I_{SC}}\right|$ I_f = current; in linear region of OCC

(d) $\left|\dfrac{V_{OC}/\sqrt{3}}{I_{SC}}\right|$ I_f = constant; in non-linear region of OCC

2. Short-circuit ratio of a synchronous machine is defined as the ratio of field current required to produce rated voltage on
   (a) full-load and field current required to produce rated current on SC
   (b) OC and field current required to produce rated armature current required.
   (c) SC and field current required to produce rated current on SC
   (d) full-load and field current required to produce rated voltage on SC
3. The armature reaction of a synchronous generator under short-circuit condition is
   (a) magnetising (b) cross magnetising
   (c) demagnetising (d) both demagnetising and cross magnetising
4. Synchronous motor speed is controlled by varying
   (a) the field current (b) the supply voltage
   (c) the supply frequency (d) both supply frequency and voltage
5. A synchronous generator is rated 10 MVA, 11 KV, 0.85 ps, 50 Hz. What is the significance of 0.85 ps?
   (a) Load of pf lower than 0.85 cannot be supplied (b) The prime mover power rating is 8.5 MW
   (c) Load of pf higher than 0.85 cannot be supplied (d) It is not of any significance.
6. A synchronous motor with S * synchronous reactance (negligible resistance) drawn a leading current of 10 A at 400 V. The induced emf is:

   (a) $400 + 1\sqrt{3} \times 50$ (b) $400 - 1\sqrt{3} \times 50$ (c) $400 - \sqrt{3} \times 50$ (d) $400 + \sqrt{3} \times 50$

7. The armature current upon symmetrical three-phase short-circuit of a synchronous machine (armature resistance negligible),
   (a) constitutes q-axis current only
   (b) constitutes d-axis current only
   (c) has both d-axis and q-axis components
   (d) short-circuit current cannot be divided into d and q-axis components

8. In a salient-pole synchronous machine,
   X_d = d-axis synchronous reactance
   X_q = q-axis synchronous reactance
   (a) $X_q > X_d$ (b) $X_q = X_d$ (c) $X_q < X_d$ (d) $X_q = 0$
9. Short-circuit ratio of a synchronous machine yields
   (a) $\dfrac{1}{X_S\,(\text{unsaturated})(PU)}$ (b) $\dfrac{1}{X_S\,(\text{unsaturated})}$
   (c) $\dfrac{1}{X_S\,(\text{adjusted})(\text{PU})}$ (d) $\dfrac{1}{X_S\,(\text{adjusted})}$
10. A synchronous generator is feeding power to infinite bus bars at unity power factor. Its excitation is now increased. It will feed
   (a) the same power but at a leading power factor
   (b) the same power but at a lagging power factor
   (c) more power at unity power factor
   (d) less power at unity power factor

Answers

Multiple-Choice Questions

1. (c) 2. (b) 3. (c) 4. (d) 5. (b)
6. (d) 7. (b) 8. (c) 9. (c) 10. (b)

Induction Motor

chapter 9

Goals & Objectives

- Induction motor, the asynchronous machine, types and constructional features
- Understanding the basic relationships—resultant air-gap flux, the exciting current
- Standstill rotor emf, effective turn ratio, standstill rotor emf, the rotor circuit slip dependent
- Stepwise development of the circuit model (equivalent circuit), concept of load resistance
- Concept of power across air gap, mechanical power developed
- Torque-slip characteristic, modes of operation—motor, generator, brake
- The starting problems, methods of starting squirrel-cage and slip-ring motors
- Problems encountered in speed control, comparison with dc motor

9.1 INTRODUCTION

The induction machine is an important class of electric machines, which finds wide applicability as a motor in industry and in its single-phase form in several domestic applications. More than 85% of industrial motors in use today are in fact induction motors. It is substantially a constant-speed motor with a shunt characteristic; a few percent speed drop from no load to full load. It is a singly fed motor (stator-fed), unlike the synchronous motor which requires ac supply on the stator side and dc excitation on the rotor. The torque developed in this motor has its origin in current induction in the rotor, which is only possible at nonsynchronous speed; hence, the name asynchronous machine. Torque in a synchronous machine, on the other hand, is developed only at synchronous speed when the 'locking' of the two fields takes place. Therefore, the induction motor is not *plagued* by the stability problem inherent in the synchronous motor. Since it is a singly fed machine, it draws its excitation current[1] from the mains to set up the rotating field in the air gap which is essential for its operation. As a consequence, it inherently has a power factor less than unity, which usually must be corrected by means of shunt capacitors at motor terminals. There is no simple and inexpensive method of controlling the induction motor speed as is possible in a dc shunt motor and thus it finds stiff competition from the dc shunt motor in such applications.

Here we shall give more constructional details and arrive at the circuit model of the machine.

9.2 CONSTRUCTION

Stator

It is properly wound for three phases connected in star/delta. In some motors, all the six leads are brought out for changing the connection from star at the time of starting to delta during running. The pictorial view of a stator is shown in Fig. 9.1.

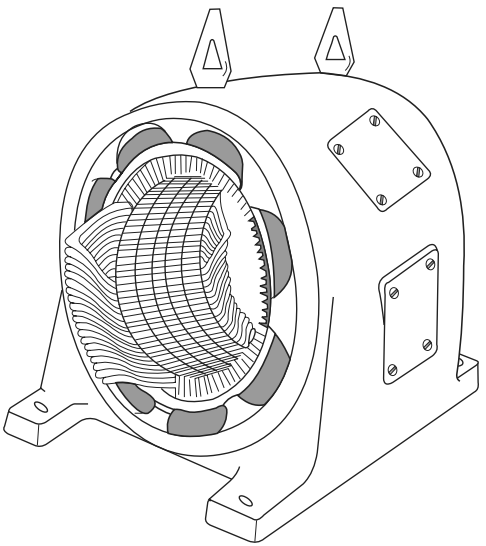


Fig. 9.1 *Induction motor stator shown partially would double-layer winding*

[1] Because of air gap the excitation current is far larger in an induction motor than in a transformer for the same VA rating.

Rotor

In one type of motor, the rotor is properly wound for three phases with three connecting leads brought out through slip rings as shown in Fig. 9.2(a). The slip rings are tapped by brushes. External resistances are connected in the rotor circuit at the time of starting but the slip rings are shorted out during running. Such a motor is called *wound-rotor* or *slip-ring motor*.

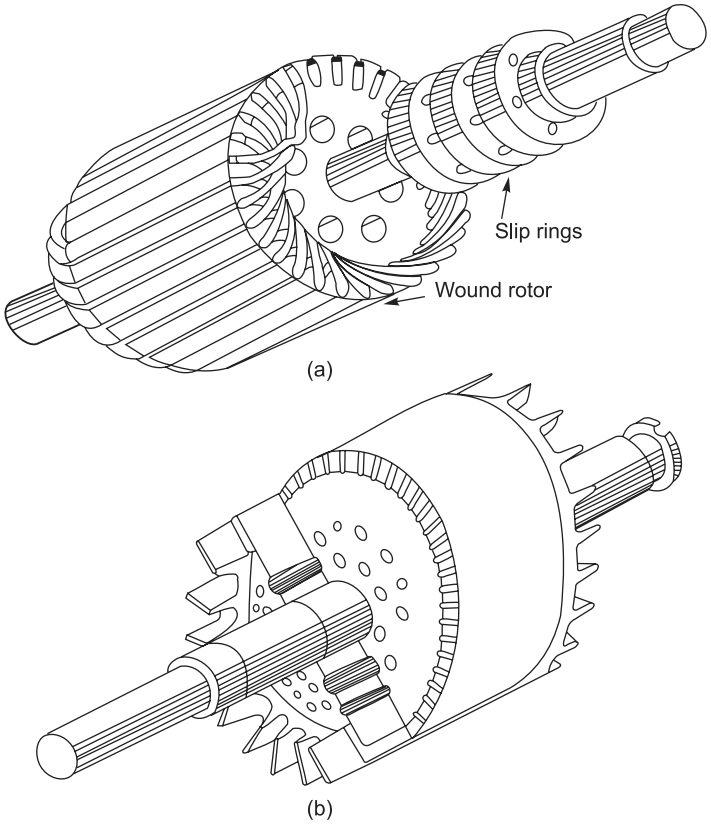


Fig. 9.2 *(a) Wound rotor for induction motor (b) Squirrel-cage rotor with cast aluminium bars and end rings*

Figure 9.2(b) is that of a *squirrel-cage* rotor where conducting bars are placed in slots and are permanently shorted at each end. *Electrically, it is equivalent to a three-phase winding, which is shorted permanently such that no external resistance can be included in it.*

Working Principle

The stator of an induction motor is wound three-phase with space-phase difference 120° elect for each pole pair. When connected to three-phase supply (V, f), it draws three-phase currents with a time-phase difference of 120° elect. This results in rotating field (same number of poles as that of winding) which is the air gap running at synchronous speed

$$n_s = \frac{120\,f}{P}$$

The rotating field induces currents in the conductors of a stationary motor. These current interacting with the field produce of torque in the same direction as the stator field causing the rotor to run, which mean the motor is self-starting. The rotor runs up to a speed spread of

$$n < n_s$$

where the electromagnetic torque T balances the load torque. The induction motor cannot reach the speed 'n_s' as the relative speed between stator field and rotor conductor will be zero. It results, in zero induced current in rotor and torque developed is zero.

Speed of stator field w.r.t. rotor conductors = $(n_s - n)$ in the forward direction (that of n_s)

Frequency of rotor currents,

$$f_2 = \frac{(n_s - n)P}{120} = \left(\frac{(n_s - n)}{n_s}\right)\left(\frac{n_s P}{120}\right) = sf \text{ (also called } \textit{slip frequency}) \tag{9.1}$$

where $s = \dfrac{n_s - n}{n_s} = \left\{1 - \dfrac{n}{n_s}\right\}$ = *slip* of rotor (per unit speed at which, the rotor falls behind the stator field) (9.2)

Obviously, $s = 1$ for $n = 0$, i.e. for the stationary rotor and $s = 0$ for $n = n_s$, i.e. for the motor running at the synchronous speed.

The rotor currents at frequency f_2 cause a rotating field $\mathbf{F}_2$ that runs w.r.t. the rotor surface at speed $(n_s - n)$ in the forward direction, while the rotor itself runs at speed n. Hence, the speed of $\mathbf{F}_2$ with the stator is always

$$(n_s - n) + n = n_s$$

and it therefore produces a torque by interaction with $\mathbf{F}_1$.

Resultant field $\mathbf{F}_r$ and air-gap flux Φ_r per pole must be nearly constant, so that stator-induced emf balances the applied voltage as stator resistance and leakage reactance are very small. Hence, the torque developed is proportional to rotor current. Also, with constant Φ_r the rotor induced emf is proportional to slip.

Induction Motor Connection Diagram

The stator, rotor and the connection diagram of a wound-rotor induction motor are drawn in Fig. 9.3(a) and (b). The stator is delta connected, the wound-rotor is star connected, and the terminals are brought out through slip rings and shorted externally. This type of motor is also known as *slip-ring* induction motor.

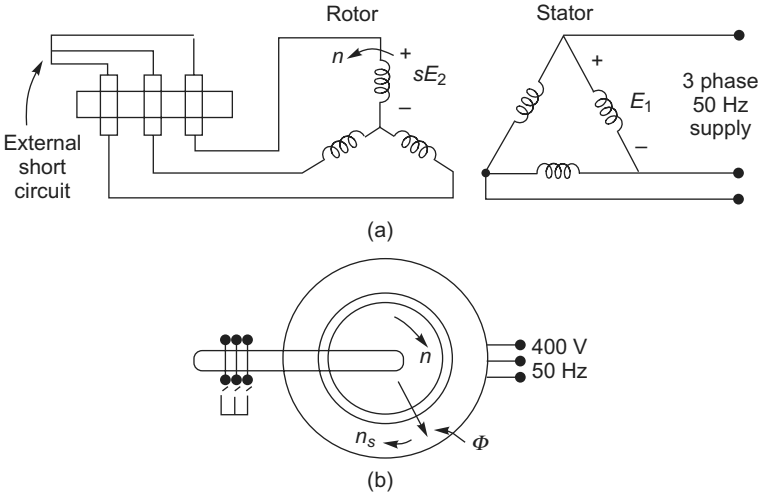


Fig. 9.3 *Stator, rotor and connection diagram of induction motor-wound rotor type*

In the connection diagram of Fig. 9.3(a), E_1 and E_2 are the stator and rotor-induced emfs. The effective turn ratio is

$$\frac{E_1}{E_2} = \frac{K_{w1} f_1 N_1}{K_{w2} f_2 N_2} \tag{9.3}$$

Torque-Slip Characteristic

Since the machine produces torque at any rotor speed, it is known as an *asynchronous machine*. An important performance measure in a motor is the variation of its speed as the shaft torque (load torque) is increased. The torque-slip (speed) characteristic of induction motor is sketched in Fig. 9.4 from which the following observations are made.

- At *low slip*[2], $T \propto s$ (linear)
- At *high slip*, $T \propto 1/s$ (rectangular hyperbola)
- The motor has a maximum torque called *breakdown* torque (T_{BD}) and cannot run at a load torque more than T_{BD}.
- The motor has a definite starting torque (corresponding to $s = 1$) which is much less than T_{BD}.
- It can be shown that if the stator voltage is changed, the torque would vary directly as the square of voltage.

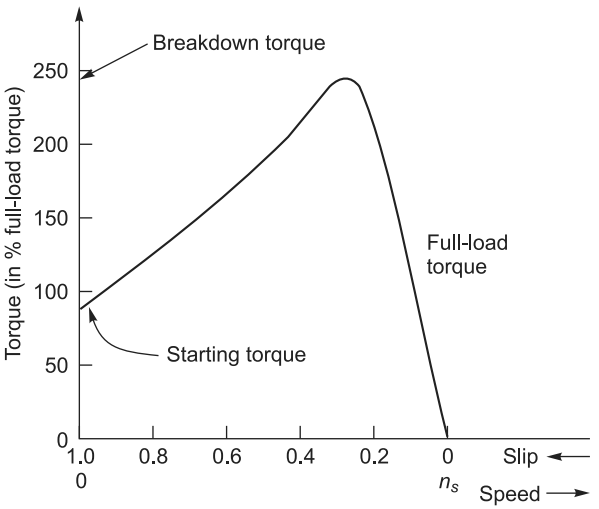


Fig. 9.4 *Torque-slip characteristic of induction motor*

Example 9.1

A 6-pole synchronous generator driven at 1000 rpm feeds a 4-pole induction motor, which is loaded to run at a slip of 4%. What is the motor speed?

Solution Frequency of the synchronous generator,

$$f = \frac{6 \times 1000}{120} = 50 \text{ Hz}$$

Synchronous speed of the induction motor,

$$n_s = \frac{120 \times 50}{4} = 1500 \text{ rpm}$$

Motor slip $s = 0.04$

Motor speed $n = (1 - s)n_s$ Eq. (9.38)

$= 0.96 \times 1500 = 1440$ rpm

[2] Rotor frequency $f_2 = sf$ is very small at low slip ($s = 0.04, f_2 = 2$ Hz). The rotor circuit reactance can therefore be neglected so that rotor circuit is basically resistive. Rotor current is therefore proportional to rotor induced emf, which itself is proportional to slip. Hence $T \propto s$, $\delta \approx 90°$).

Example 9.2

A 4-pole, 50 Hz wound-rotor motor when supplied at rated voltage and frequency with slip-rings[3] open-circuited develops a voltage of 80 V between any two rings. With the same stator excitation, the rotor is now driven by external means at (a) 1500 rpm in opposite direction to the direction of rotation of the stator-caused field, and (b) 1000 rpm in the same direction. Find the slip-ring voltage and its frequency in each of these two cases.

Solution

$$n_s = \frac{120 \times 50}{4} = 1500 \text{ rpm}$$

With slip rings open, the rotor remains stationary as it does not carry any currents and no torque is developed ($s = 1$). The corresponding voltage (standstill) is $V_2 = 80$ V and the frequency is $f = 50$ Hz.

(a) $n_1 = -1500$ rpm

$$s_1 = \frac{1500 - (-1500)}{1500} = 2$$

$$f_2 = s_1 f = 100 \text{ Hz}$$

With given stator excitation, Φ_r in air gap is fixed. The rotor voltage is proportional to the rotor frequency or the slip. Thus, slip-ring voltage is $2 \times 80 = 160$ V.

(b) $n_2 = 1000$ rpm

$$s_2 = \frac{1500 - 1000}{1500} = \frac{1}{3}$$

$$f_2 = s_2 f = \frac{50}{3} = 16\frac{2}{3} \text{ Hz}$$

$$\text{Slip-ring voltage} = s_2 V_2 = \frac{1}{3} \times 80 = 26\frac{2}{3} \text{ V}$$

❑ **Rating**

kW, Voltage, Speed (at full-load)
Frequency 50 Hz, (need not be specified)
kW is the rated output power called shaft power

9.3 CIRCUIT MODEL (EQUIVALENT CIRCUIT)

An induction motor is a generalised transformer in which, rotor emf and frequency both depend upon the rotor speed and in the process, conversion of energy takes place. This is explained below step-by-step followed by the circuit model.

The resultant field in the air gap must produce a flux Φ_r/pole, which induces a counter emf in the stator winding to balance the applied voltage (per phase) minus the voltage drop in the stator impedance (resistance and leakage reactance). If this drop is neglected,

[3] In a wound-rotor induction motor, three connections from the winding are brought out through slip-rings. Under running condition the slip rings are shorted. At the time of starting the motor external resistances are included in the rotor circuit through the slip-rings. A wound-rotor motor is therefore also known as a *slip-ring* induction motor.

$$V_1 \approx E_1 = \pi\sqrt{2}\, K_{w1}\, N_{\text{ph1}}(\text{series})\, f\, \Phi_r \tag{9.4}$$

where V_1 = applied voltage/phase
K_{w1} = stator winding factor
N_{ph1} (series) = stator series turns/phase
f = stator frequency

1. The stators must draw a 90° lagging magnetising current component I_m to produce Φ_r. It will also be associated with a core loss component I_i. The net exciting current is

$$\bar{I}_0 = \bar{I}_m + \bar{I}_i \tag{9.5}$$

Magnitude-wise, $I_m >> I_i$. The phasor diagram of the exciting current is drawn in Fig. 9.5, where θ_0 is only slightly less than 90°.

Because of air gap in magnetic circuit of the induction motor (compared with transformer which has no air gap being a static device), the net exciting current may be as large as 40% (magnitude-wise) of the full-load stator current.

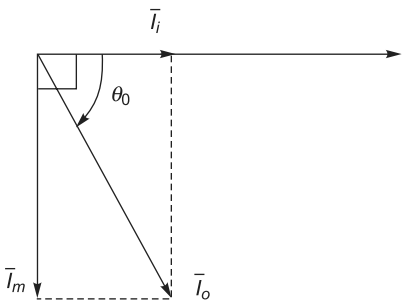


Fig. 9.5 *Phasor diagram*

2. Rotor induced emf at *standstill* (stator excited rotor blocked from rotation) is

$$E_2 = \pi\sqrt{2}\, K_{w2}\, N_{ph2}(\text{series})\, f\, \Phi_2 \tag{9.6}$$

Thus,

$$\frac{E_1}{E_2} = \frac{K_{w1}\, N_{ph1}}{K_{w2}\, N_{ph1}}$$

$$= a \text{ (effective turn ratio)} \tag{9.7}$$

- Rotor frequency at any speed n (slip s) is

$$f_2 = sf \tag{9.8}$$

and the corresponding induced emf is sE_2. (9.9)

- Though the rotor carries currents of frequency sf, because of rotor speed, these interact magnetically with the stator field at speed n_s or to the stator these appear as currents of frequency f, the stator frequency.
- The stator apart from I_0, the exciting current, draws a current component $\bar{I}'_2$ to balance the ampere turns of the rotor current $\bar{I}_2$. Thus,

$$\frac{\bar{I}'_2}{\bar{I}_2} = \frac{1}{a} \tag{9.10}$$

The net stator current is, therefore,

$$\bar{I}_1 = \bar{I}_0 + I'_2 \tag{9.11}$$

Because of large lagging exciting current [Eq. (9.5)] the stator current has a pf less than unity (0.85 or less at full load). The pf will reduce as the load on motor is decreased ($\bar{I}'_2$ reduces while $\bar{I}_0$ remains unchanged in Eq. (9.11)). Hence, an induction motor should not be operated at light load for long periods of time.

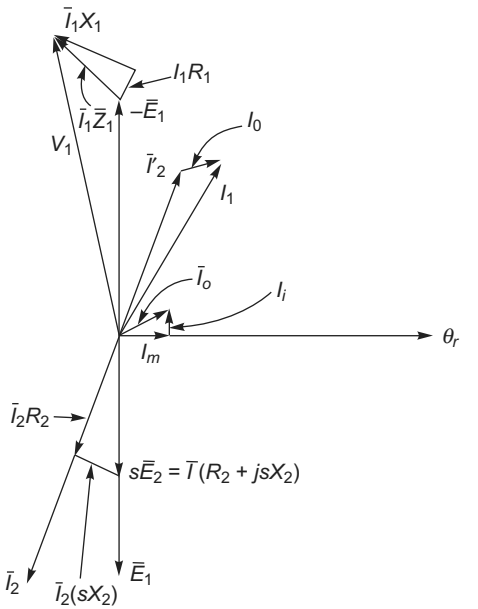


Fig. 9.6 *Phasor diagram of induction motor at slip 's' and* $\left(e_1 = -\frac{d\lambda}{dt}\right)$

Phasor Diagram

The phasor diagram for sake of clarity in drawn as per induced imf e = $\frac{dr}{dt}$. The causes the induced emfs E_1, E_2 (stamp shill) to lag by 90° to Fr and also I_2 in phase opposition to I_2. Further the phasor diagram of Fig. 9.6 is drawn at slip 's'

Rotor Circuit Impedance

With the stator connected to the mains (V, f) and the rotor held stationary (blocked from rotation), a condition called *standstill*, the frequency of the rotor currents is *f,* the same as the stator. The rotor reactance under these conditions is X_2, the *standstill reactance*.

As the rotor runs at speed n (slip s), the frequency of rotor currents is $f_2 = sf$.

The rotor reactance at this frequency is

$$f_2\left(\frac{X_2}{f}\right) = s X_2 \tag{9.12}$$

Thus the rotor circuit impedance at slip s (speed n) is

$$R_2 + js\, X_2$$

The power crossing the air gap P_G is split into two parts—the mechanical power output P_m and electrical loss in rotor resistance $3I_2^{\,2} R_2$.

In the next step, the transformer turn ratio is changed from a:1 to 1:1 like in a static transformer. It is to be observed that this transformation is *power invariant* wherein P_G, the power crossing from the stator to the rotor and P_m, the mechanical power developed, are preserved as such.

In the rotor circuit,

$$\bar{I}'_2 = \frac{s\bar{E}_1}{R'_2 + jsX'_2} \tag{9.13}$$

Dividing both numerator and denominator by s,

$$\bar{I}'_2 = \frac{\bar{E}_1}{R'_2/s + jX'_2} \tag{9.14}$$

The trick refers the rotor circuit to the stator frequency. This transformation is not power invariant and in the process, the mechanical power developed per phase is now represented electrically as

$$\frac{P_m}{3} = \frac{I'^2_2 R'_2}{s} - I'^2_2 R'_2$$

$$= I'^2_2\left(\frac{1}{s} - 1\right)R'_2 \tag{9.15}$$

The final circuit model presented in Fig. 9.7 is approximate to the extent that the exciting shunt branch has been connected before the stator impedance. This approximation was also used in the transformer model but is a much stronger approximation in induction motor as the exciting (or no-load) current I_0, because of the air gap in the magnetic circuit, is much larger in the induction motor than it is in a transformer (2–5% of full-load current). I_0 in induction motor can be as large as 40% of the full-load current (in magnitude).

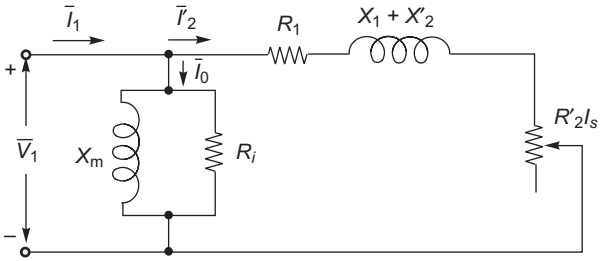


Fig. 9.7 *Development of circuit model (equivalent circuit) of induction motor*

Power Across Air Gap, Torque and Power Output

The power crossing the air gap (after accounting for core loss and stator copper loss) is

$$P_G = \frac{3I'^2_2 R'_2}{s} \tag{9.16}$$

$$= \frac{3I'^2_2 R_2}{s} \tag{9.17}$$

$\therefore$ power across air gap

$$= \frac{\text{rotor copper loss}}{\text{slip}}$$

It also follows that

$$\text{Rotor copper loss } 3I'^2_2 R'_2 = s P_G \tag{9.18}$$

Now the mechanical power output (gross) is

$$P_m = P_G - 3I'^2_2 R'_2$$

$$= 3I'^2_2 R'_2 \left(\frac{1}{s} - 1\right) \tag{9.19}$$

$$= (1 - s)P_G \tag{9.20}$$

As per Eq. (9.19), the mechanical power output is the power absorbed by the load resistance R'_2 (l/s – 1)
The rotor speed is

$$\omega = (1 - \text{s})\omega_s \text{ rad (mech)/s}$$

The electromagnetic torque developed is given by

$$T = \frac{P_m}{\omega} = \frac{3I'^2_2 R'_2 (1/s - 1)}{(1 - s)\omega_s}$$

$$= \frac{3I'^2_2 R'_2}{s\omega_s} = \frac{P_G}{\omega_s} \text{ Nm} \tag{9.21}$$

It immediately follows that

$$P_G = T\omega_s \tag{9.22}$$

i.e. power across the air gap = torque × synchronous speed. Therefore, P_G is also called torque in *synchronous watts*.

The net mechanical power output and torque are obtained by subtracting losses—windage, friction and stray-load loss.

Power Factor

The stator current (line current) is

$$\bar{I}_1 = \bar{I}_0 + \bar{I}'_2$$

The load component of the line current is given by

$$\bar{I}'_2 = \frac{V}{(R_1 + R'_2/s) + g(X_1 + X'_2)}$$

At low values of slip (2–5%) at full load, R'/s predominates and I'_2 has a small lagging angle (high pf). On the other hand, the exciting current has a large lagging phase angle (slightly less than 90°). Further, its magnitude is about 40% of the load current resulting in the pf of the line current (I_1) of the order of 0.8 to 0.85 lagging. This fact is illustrated by the adjoining phasor diagram. Refer Example 9.3.

If the motor load is lightened, $\bar{I}'_2$ reduces, while $\bar{I}_0$ remains constant. It can be easily visualised from the phasor diagram that θ will increase and the pf will reduce. Therefore, an induction motor should not be run at light load for long periods of time. In choosing an induction motor, its rating should match the load. Over-rated motors should not be used.

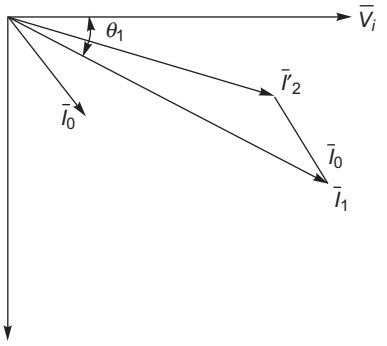


Fig. 9.8 *Phasor diagram*

Example 9.3

The efficiency of a 400 V, three-phase, 6-pole induction motor drawing a line current of 80 A at 0.75 pf at 4% slip is 85%. Calculate the shaft output and shaft torque.

Solution

$$\text{Input} = \sqrt{3} \times 400 \times 80 \times 0.75 \times 10^{-3}$$
$$= 41.57 \text{ kW}$$
$$\text{Shaft output} = 41.57 \times 0.85 = 35.33 \text{ kW}$$
$$n_s = 1000 \text{ rpm}$$
$$n = (1 - 0.04) \times 1000 = 960 \text{ rpm}$$
$$\omega = \frac{2\pi \times 960}{60} = 100.5 \text{ rad/s}$$
$$\text{Shaft t3orque} = \frac{35.33 \times 1000}{100} = 351.5 \text{ Nm}$$

Example 9.4

A 4-pole, 50 Hz, three-phase induction motor when running on full load develops a useful torque of 100 Nm while the rotor emf is observed to make 120 cycles/min. It is known that the torque lost on account of friction and core loss is 7 Nm. Calculate.

(a) shaft power output,
(b) rotor copper loss,
(c) motor input, and
(d) motor efficiency.

The total core loss is given as 700 W.

Solution

$$f_2 = sf = \frac{120}{60} = 2 \text{ Hz}$$

$$s = \frac{5}{50} = 0.04$$

$$n_s = 1500 \text{ rpm}$$

$$n = (1 - 0.04) \times 1500$$
$$= 1440 \text{ rpm}$$

$$\omega = \frac{1440 \times 2\pi}{60}$$
$$= 150.7 \text{ rad/s}$$

(a) Shaft power output = $T\omega = 100 \times 150.7 = 15.07$ kW
Mechanical power developed,

$$P_m = (100 + 7) \times 150.7 = 16.12 \text{ kW}$$

(b) From Eq. (9.19),

Rotor copper loss $3I_2^2R_2 = P_m\left(\frac{s}{1-s}\right)$

$$= 16.12 \times \frac{0.04}{(1-0.04)} = 0.67 \text{ kW}$$

(c) Motor input = 16.12 + 0.67 + 0.7 = 17.49 kW

$$\eta = \frac{15.07}{17.49} = 86.16\%$$

9.4 TORQUE-SLIP CHARACTERISTIC

For the sake of simplicity of treatment, the stator impedance will be neglected.[4] The simplified circuit for obtaining torque expression is given in Fig. 9.9. The result given below follows immediately.

$$I'_2 = \frac{V_1}{\sqrt{(R'_2/s)^2 + X'^2_2}} = \frac{V_1/a}{\sqrt{(R_2/s)^2 + X_2^2}} \quad (9.23)$$

Substituting in Eq. (9.18),

$$T = \frac{P_G}{\omega_s} = \frac{3}{\omega_s}\frac{V_1^2(R'_2/s)}{(R'_2/s)^2 + X'^2_2} = \frac{3}{\omega_s}\frac{(V_1/a)^2(R_2/s)}{(R_2/s)^2 + X_2^2} \quad (9.24)$$

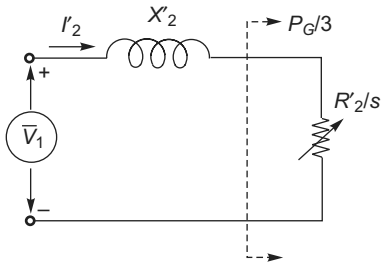


Fig. 9.9 *Circuit for obtaining torque expression*

For maximum torque, $P_G/3$ in Fig. 9.9 must be maximum, which happens when R'_2/s matches with X'_2 (maximum power transfer theorem), i.e.

$$\frac{R'_2}{s_{\max T}} = X'_2$$

[4] This assumption causes a tolerable error in the region of low slip but unacceptable error for large slips. Yet it helps to get a feel of the complete *T-s* characteristic.

or $$s_{\max T} = \frac{R'_2}{X'_2} = \frac{R_2}{X_2} = \frac{\text{rotor resistance}}{\text{standstill reactance}} \tag{9.25}$$

Substituting Eq. (9.25) in Eq. (9.24),

$$T_{\max} \text{ or } T_{\text{breakdown}} = \frac{3}{\omega_s}\left(\frac{V_1^2}{2X'_2}\right) \tag{9.26}$$

$$= \frac{3}{\omega_s}\left(\frac{(V_1/a)^2}{2X'_2}\right) \tag{9.27}$$

For load torque $T_L > T_{\max}$, the motor stalls and so it is called *breakdown torque*.

Starting current and torque are given by substituting $s = 1$ in Eqs (9.23) and (9.24). Thus,

$$I'_{2(\text{start})} = \frac{V_1}{\sqrt{R'^2_2 + X'^2_2}} = \frac{V_1/a}{\sqrt{R_2^2 + X_2^2}} \tag{9.28}$$

$$T_{\text{start}} = \frac{3}{\omega_s}\frac{V_1^2 R'_2}{(R'_2)^2 + X'^2_2} = \frac{3}{\omega_s}\frac{(V_1/a)^2 R_2}{R_2^2 + X_2^2} \tag{9.29}$$

The starting torque increases by adding resistance in the rotor circuit. At the same time, the starting current will reduce. This indeed is the advantage of the slip-ring induction motor in which a high starting torque is obtained at low starting current.

Observe that

$$T_{\text{start}}\,(\max) = T_{\text{breakdown}};\ R'_2 = X'_2 \text{ (Eq. (9.25))} \tag{9.30}$$

Ignoring R'_2/s,

$$T = \frac{3}{\omega_s}\frac{V_1^2 R'_2}{sX'^2_2} = \frac{3}{\omega_s}\frac{(V_1/a)^2 R_2}{sX_2^2} \text{ (inverse law } T\text{–}s\text{)} \tag{9.31}$$

Plot of Complete T-s Characteristic

From the above results, the complete *T-s* characteristic is plotted in Fig. 9.10. Its various operating modes are the following:

❑ **Motoring Mode** $0 \le s \le 1$; subsynchronous speed, motor runs in the direction of the rotating air gap field;

❑ **Braking Mode** $s > 1$; motor runs in opposite direction to the rotating field; and

❑ **Generating Mode** $s < 0$; motor runs at supersynchronous speed in the direction of the rotating field. Negative s implies that mechanical power output [Eq. (9.19)] is negative (input) and so the electrical power is the output. Also, from Eq. (9.16), power across the air gap changes sign. Power transfers from rotor to stator across the air gap.

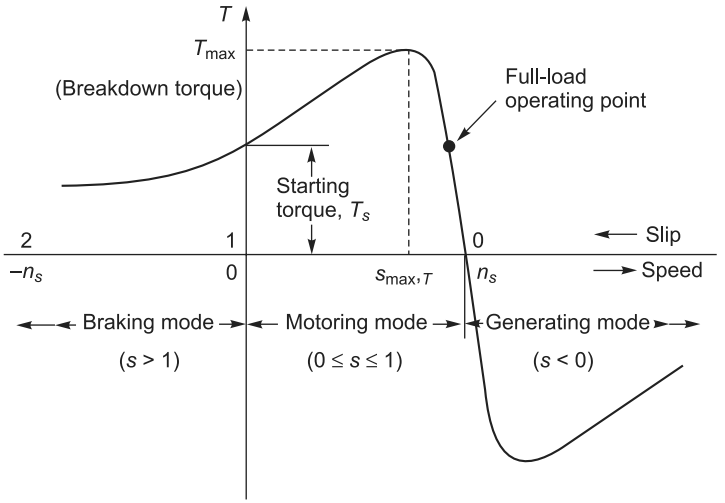


Fig. 9.10 *Torque-slip characteristic of induction motor (at fixed terminal voltage)*

External Resistance Added in Rotor Circuit

This is only possible in a slip-ring induction motor. As resistance is added in the rotor circuit, we observe that

- breakdown torque remains unchanged (Eq. (9.27));
- slip at breakdown torque increases (Eq. (9.25)); and
- T_{start} becomes maximum (equal to $T_{breakdown}$) at $R_2 = X_2$.

The torque-slip characteristics of the induction motor for increasing values of rotor resistance are plotted in Fig. 9.11.

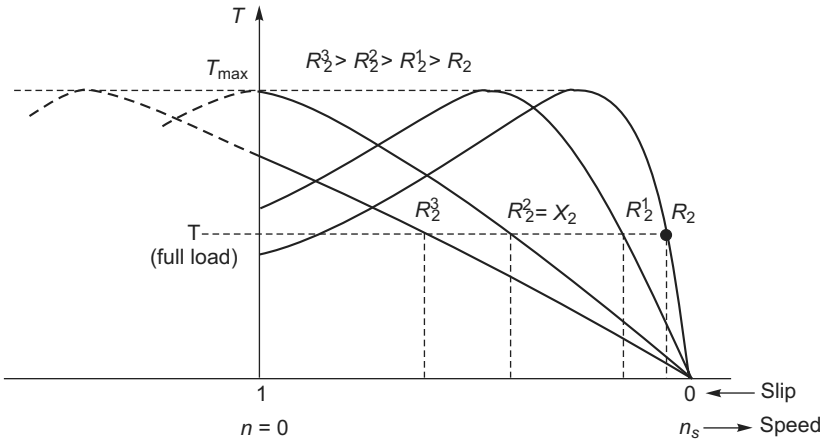


Fig. 9.11 *Torque-slip characteristics of induction motor with increasing values of rotor resistance*

Example 9.5

A 6.6 kV, 20-pole, 50 Hz, three-phase star-connected induction motor has a rotor resistance of 0.12 Ω, and a standstill reactance of 1.12 Ω. The motor has a speed of 292.5 rpm at full load. Calculate (a) slip at maximum torque, and (b) the ratio of maximum to full-load torque. Neglect stator impedance.

Solution

$$n_s = \frac{120 \times 50}{20} = 300 \text{ rpm}$$

$$s_{fl} = \frac{300 - 292.5}{300} = 0.025$$

(a) From Eq. (9.25),

$$s_{\max T} = \frac{R_2}{X_2} = \frac{0.12}{1.12} = 0.107$$

(b) From Eq. (9.24),

$$T_{\text{f1}} = \frac{3}{\omega_s} \frac{(V/a)^2 \times 0.12 / 0.025}{(0.12 / 0.025)^2 + (1.12)^2} = \frac{3}{\omega_s} \left(\frac{V}{a} \right)^2 \times 0.1976 \quad \text{(i)}$$

From Eq. (9.27),

$$T_{\max} = \frac{3}{\omega_s} \frac{0.5(V/a)^2}{1.12} = \frac{3}{\omega_s} \left(\frac{V}{a} \right)^2 \times 0.446 \quad \text{(ii)}$$

Dividing Eq. (ii) by Eq. (i),

$$\frac{T_{\max}}{T_{ft}} = \frac{0.446}{0.1976} = 2.26$$

Example 9.6

A three-phase, Y-connected, 440 V, 7.5 kW, 50 Hz, 6-pole induction motor has the following circuit parameter constants.

R_1 = 1.06 Ω $\quad$ R'_2 = 0.576 Ω

X_1 = 1.68 Ω $\quad$ X'_2 = 0.75 Ω

X_m = 44.2 Ω

The total windage, friction and core losses may be assumed to be 415 W at any load.

The motor runs at a speed of 975 rpm at rated voltage and frequency on a particular load. Calculate input torque and power, stator current, power factor and efficiency.

Solution

$$n_s = 1000 \text{ rpm}, \ \omega_s = \frac{2\pi \times 1000}{60} = 104.7 \text{ rad/s}$$

$$n = 975 \text{ rpm}$$

$$s = \frac{1000 - 975}{1000} = 0.025$$

As the iron-loss resistance R_i is not provided, it will be ignored and stator iron loss along with windage and friction loss will be subtracted from the gross mechanical power output. From Fig 9.7

$$\begin{aligned}
\bar{Z} &= (1.06 + 0.576/0.025) + j(1.68 + 0.75) \\
&= 24.1 + j2.43 = 24.22 \angle 5.8^\circ \\
\bar{I}'_2 &= \frac{440/\sqrt{3}}{24.22} \angle -5.8^\circ = 10.5 \angle -5.8^\circ \text{ A} \\
\bar{I}_0 \approx \bar{I}_m &= -j\frac{440/\sqrt{3}}{44.2} = -j5.75 \text{ A} \\
I_1 &= \bar{I}_0 + \bar{I}'_2 = 10.5 \angle -5.8^\circ - j5.75 \\
&= 12.45 \angle -33^\circ \text{ A} \\
\text{pf} &= \cos 33^\circ = 0.84 \text{ lag} \\
\text{Power input} &= \sqrt{3} \times 440 \times 12.45 \times 0.84 \\
&= 7.97 \text{ kW} \\
\text{Power output (gross)} &= 3I'^2_2 R'_2 \left(\frac{1}{s} - 1\right) \\
&= 3 \times (10.5)^2 \times 0.576 \left(\frac{1}{0.025} - 1\right) \\
&= 7.43 \text{ kW} \\
\text{Power output (net)} &= 7.43 - 0.415 \\
&= 7.015 \text{ kW} \\
\eta &= \frac{7.015}{7.97} = 88\% \\
\text{Torque (net)} &= \frac{7.015 \ \ 1000}{104.7(1 - 0.025)} \\
&= 68.72 \text{ Nm}
\end{aligned}$$

9.5 DETERMINATION OF CIRCUIT MODEL PARAMETERS

Since an induction machine is analogous to a transformer, similar non-loading tests would determine the circuit model parameters wherein the blocked rotor test now corresponds to the SC test of a transformer.

9.5.1 No Load Test

The machine is run as a motor on no load. It runs close to synchronous speed ($s \approx 0$). It cannot reach synchronous speed because of windage and friction loss. Under no-load condition, therefore, the circuit model of Fig. 9.7 simplifies as Fig. 9.12 because

$$\text{load resistance} = R'_2 \left(\frac{1}{s} - 1\right)\Big|_{s \approx 1}$$

$$\approx \infty \text{ (open circuit)}$$

The data recorded during the no-load test are:

V_0 (line) rated value

I_0 = no-load current

P_o = no-load power (3 phase)

= stator core loss plus windage and friction loss

From these values X_m and R_i can be computed as illustrated in Example 9.7.

It is to be noted the R_i now includes the effect of windage and friction loss apart from the stator iron loss.

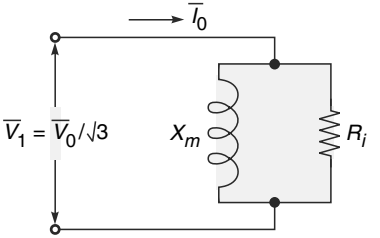


Fig. 9.12 *Circuit model at no load (equivalent star basis)*

9.5.2 Blocked-Rotor Test

The stator is supplied with reduced voltage while the rotor is blocked, i.e. not allowed to rotate (s =1). Now

$$\text{load resistance} = R'_2 \approx 0 \text{ (short circuit)}$$

because of which a much reduced voltage (about 25% of rated) has to be applied for circulating full-load current. At such low voltage, exciting current and stator core loss can be ignored, i.e. the shunt branch of the circuit model is disconnected reducing the circuit of Fig. 9.7 to that of Fig. 9.13.

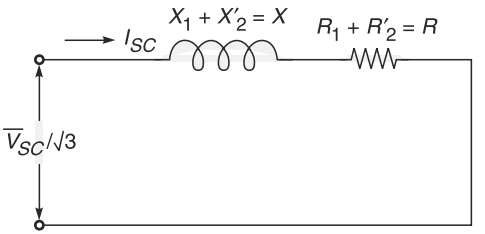


Fig. 9.13 *Circuit model for blocked-rotor test*

The data recorded during the test are:

V_{SC} (line), I_{SC} (line)

P_{SC} = full-load copper loss

From these values, we can compute

$$R = R_1 + R_2 \text{ and } X = X_1 + X_2$$

as illustrated in Example 12.8. The stator phase resistance R_1 can be measured by dc test and corrected to ac value and R_1, R'_2 separated. For separating X_1, X'_2, we can use the approximation

$$\frac{X_1}{X_2} = \frac{R_1}{R_2}$$

9.5.3 Voltage-Ratio (a) Test

It is possible to measure the voltage ratio ($E_1/E_2 = a$) only for a slip-ring motor with slip rings open-circuited (obviously rotor would be stationary).

Example 9.7

A 3-phase, 400 V, 25 kW, 50 Hz, 8-pole motor yielded the following data on testing:

No load	400 V	8.7 A	1210 Ω
Blocked rotor	200 V	47.8 A	6050 Ω

The stator phase resistance is 0.42 Ω (star basis).

(a) Estimate the parameters of the circuit model.

(b) The motor is run from 400 V, 50 Hz, 3-phase supply. Calculate

(i) Line current, power factor, torque developed and motor efficiency at 710 rpm,

(ii) Line current and torque developed at starting, and

(iii) Maximum torque and the slip at which it occurs.

Solution

(a) Motor parameters (equivalent star basis): Refer Fig. 9.7.

No Load Test Shunt branch parameters

$$\frac{P_0}{3} = \frac{(V/\sqrt{3})^2}{R_i}$$

or
$$R_i = \frac{(V/\sqrt{3})^2}{(P_0/3)} \quad \text{(i)}$$

Substituting values

$$R_i = (400/\sqrt{3})^2/(1210/3)$$
$$= 132.2\ \Omega \text{ (inclusive of windage and friction loss)}$$
$$P_0 = \sqrt{3}\ V I_o \cos\theta_0$$

or

$$pf = \cos\theta_o = 1210/(400\sqrt{3} \times 8.7) = 0.2 \text{ lag}$$
$$\theta_0 = 87.5°$$
$$R_i = (400/\sqrt{3})^2/(1210/3)$$
$$= 132.2\ \Omega \text{ (inclusive of windage and friction loss)}$$
$$\cos\theta_0 = 1210/(\sqrt{3} \times 400 \times 8.7) = 0.2;\ \theta_0 = 78.5°$$
$$X_m = R_i / \tan\theta_0 = 27\ \Omega$$

Blocked Rotor Test

$$R = R_1 + R_2' = \frac{6050}{3 \times (47.8)^2} = 0.883\ \Omega$$
$$R_2' = 0.883 - 0.42 = 0.463\ \Omega$$
$$Z = \frac{200\sqrt{3}}{47.8} = 2.146\ \Omega$$
$$X = \sqrt{Z^2 - R^2}$$

Substituting values

$$X = X_1 + X_2' = [(2.416)^2 - (0.883)^2]^{1/2}$$
$$= 2.25\ \Omega$$

(b) (i)
$$n_s = 750 \text{ rpm},\ \omega_s = 78.54 \text{ rad/s}$$
$$s = \frac{750 - 710}{750} = 0.053$$

With reference to Fig. 12.7

$$\bar{Z} = (0.42 + 0.463/0.053) + j\,2.25$$
$$= 9.16 + j\,2.25 = 9.43\ \angle 13.8°\ \Omega$$

$$I_2' = \frac{400/\sqrt{3}\ \angle 0°}{9.43\ \angle 13.8°} = 24.5\ \angle -13.8°\ \text{A}$$

$$\bar{I}_0 = 8.7\ \angle -78.5°$$

$$\bar{I}_1 = 8.7\ \angle -78.5° + 24.5\ \angle -13.8°$$

$$= 29.3\ \angle -29.4°\ \text{A}$$

$$I_1 = 29.3\ \text{A},\ pf = 0.87\ \text{lag}$$

Now $$T = \frac{3I_2'^2\ R_2'}{s\omega_s};\ \text{(Eq. (9.21))}$$

$$= \frac{3 \times (24.5)^2 \times 0.463}{0.053 \times 78.54}$$

= 200.3 Nm (net; because windage and friction loss is accounted for in the shunt branch)

Power output $= 3I'^2{}_2 R_2';\ \left(\frac{1}{s} - 1\right)$ (Eq. (9.21))

$$= 3 \times (24.5)^2 \times 0.463 \left(\frac{1}{0.053} - 1\right)$$

= 14.897 kW (net; because of the same reason as advanced for torque)

Power input $= \sqrt{3} \times 400 \times 29.3 \times 0.87$

= 17.66 kW

$$\eta = \frac{14.897}{17.66} = 84.36\%$$

(ii) $s = 1$

$$\bar{Z} = 0.883 + j\,2.25$$

$$= 2.42\ \angle 68.6°\ \Omega$$

$$I_2' = \frac{400/\sqrt{3}\ \angle 0°}{2.42 \angle 68.6°} = 95.43 \angle -68.6°\ \text{A}$$

$$\bar{I}_1 = 8.7 \angle -78.5° + 95.43 \angle -68.6°$$

$$= 103.6 \angle -69.94°\ \text{A}$$

$$T_{\text{start}} = \frac{3 \times (95.43)^2 \times 0.463}{78.54}$$

= 161.1 Nm

(iii) For maximum torque P_G should be maximum. With reference to Fig. 12.7, this condition is fulfilled when (maximum power transfer theorem)

$$[R_1^2 + (X_1 + X_2')^2]^{1/2} = \frac{R_2'}{s_{\max T}} \quad \text{(ii)}$$

or $$s_{\max T} = \frac{R_2'}{\left[R_1^2 + (X_1 + X_2')^2\right]^{1/2}} \quad \text{(iii)}$$

$$= \frac{0.463}{\left[(0.42)^2 + (0.25)^2\right]^{1/2}} = 0.2$$

Now for $s = 0.2$

$$= \left(0.42 + \frac{0463}{0.2}\right)^2 + j\,2.75\ \Omega$$

$$= 2.735 + j\,2.25 = 3.54\ \angle 39.4°$$

$$I'_2 = \frac{400/\sqrt{3}}{3.54} = 65.24\ \text{A}$$

$$T_{\max} = \frac{3 \times (65.25)^2 \times 0.463/0.2}{78.54}$$

$$= 376.3\ \text{Nm}$$

9.6 STARTING

At starting (s = 1), short-circuit conditions prevail (load resistance = 0). The motor starting current can therefore be as large as four to six times the full-load current. Yet, at the same time, the starting torque is no higher than the full-load torque $\left(T_s = \left.\frac{I_s^2 R'_2}{s\omega_s}\right|_{s=1}\right)$. While such large currents, which flow for the short starting period, cannot damage the motor, these may not be permitted to be drawn from the power network depending upon its source impedance (low-impedance source can stand large current demands without undue voltage dips, which are bothersome to other consumers). In general, however, motors above 5 kW should not be started direct-on-line (DOL) and also if permissible, these should be started on no-load (motor decoupled from load) so that these can run to speed quickly.

9.6.1 Squirrel-Cage Motors

Reduced voltage is the only possible method of starting a squirrel-cage motor as the rotor cage is permanently shorted and cannot be tampered with. The starting torque reduces as voltage square (see Eq. 9.29) and therefore only no-load starting is possible. Various methods of starting squirrel-cage motors are discussed below.

Stator Impedance Starting

Motor voltage is reduced by placing series resistance/reactance in the lines. The starting current reduces directly as the motor voltage but the torque reduces as square of voltage. This method can only be used for small fractional kW motors.

Star-Delta Starting

The motor is designed for delta running and is started in star as shown in Fig. 9.14. Let

Z_{sc} = short-circuit phase impedance (delta connection)

V = line-to-line voltage

DOL (direct on line) starting (in delta):

$$I_{s\,(\text{phase})} = \frac{V}{Z_{sc}} \tag{9.32}$$

$$I_{s\,(\text{line})} = \frac{\sqrt{3}\,V}{Z_{sc}} \tag{9.33}$$

$$T_s \propto I^2_{s\,(\text{phase})} = \frac{V^2}{Z^2_{sc}} \tag{9.34}$$

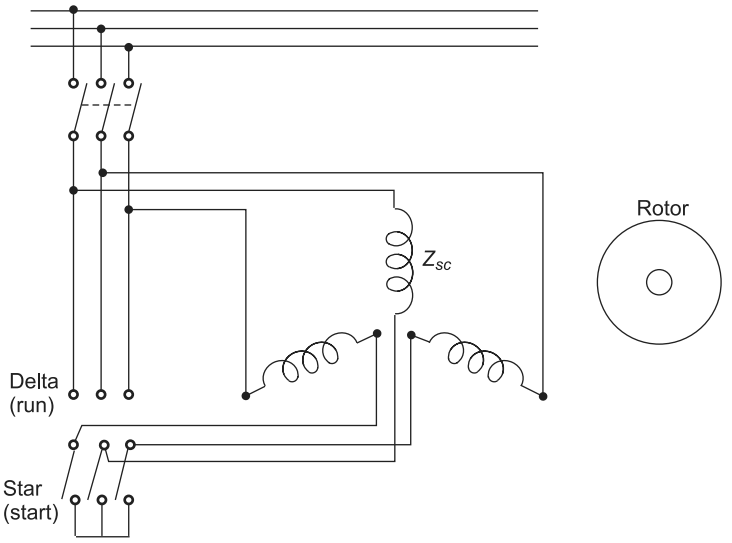


Fig. 9.14 *Star-delta starting*

Starting in star,

$$I_{s\,(\text{line})} = I_{s(\text{phase})} = \frac{V^2}{\sqrt{3}\,Z_{sc}} \tag{9.35}$$

$$T_s \propto \frac{V^2}{\sqrt{3}\,Z_{sc}^2} \tag{9.36}$$

From these results, we get

$$\frac{I_{s(\text{line})}(\Delta)}{I_{s\,(\text{line})}(\Delta)} = \frac{1}{3} \tag{9.37}$$

and

$$\frac{T_s(\Delta)}{T_s(\Delta)} = \frac{1}{3} \tag{9.38}$$

Observe that compared to DOL starting, torque reduces by the same factor (1/3) same as the line current. Because of this advantage and simplicity of the method, it is popularly used.

Autotransformer Starting

The connection diagram for this method of starting is drawn in Fig. 9.15. It is immediately observed that compared to DOL starting both torque and line current reduce by a factor of a^2 (a being the voltage ratio of autotransformer). It is also observed that star/delta starting corresponds to $a = 1/\sqrt{3}$ (fixed). The autotransformer can incidentally be used for small speed reduction, if desired. Because of the expense involved, this method is employed only for large squirrel-cage motors.

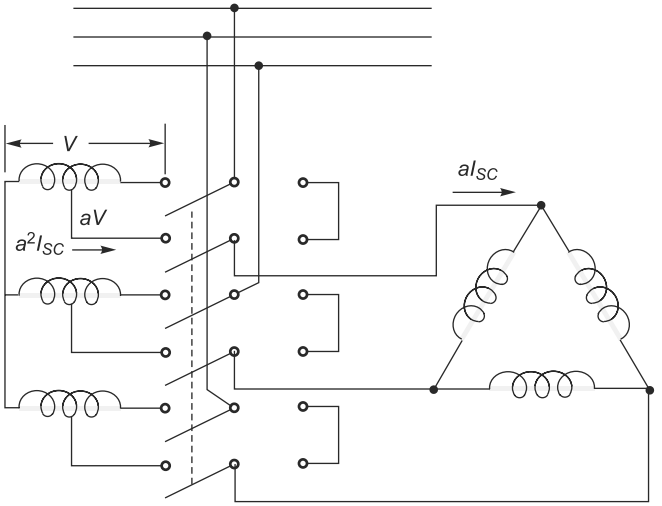


Fig. 9.15 *Autotransformer starting*

9.6.2 Slip-Ring Motors

Rotor Resistance Starting

Resistances are included in the rotor circuit via slip rings as shown in Fig. 9.16 and are cut out in steps as the motor picks up speed. While the starting current reduces, the starting torque increases (unlike in squirrel-cage motor starting); the starting torque being maximum at R_2 (total) = X_2 (see Fig. 9.11). Thus, the method is ideal for on-load starting. The slip-ring motor being more expensive than the squirrel-cage motor (because of wound rotor), it is employed only where on-load starting is a necessity. High starting torque in the medium range can be obtained by the less expensive double-cage motor (described later).

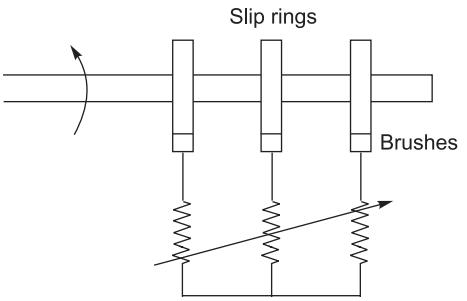


Fig. 9.16 *Rotor resistance starting*

Example 9.8

A squirrel-cage induction motor has a full-load slip of 4%. Its starting current is five times its full-load current. Calculate the starting torque in pu of the full-load torque. Neglect stator impedance and magnetising current.

Solution

$$\text{Starting torque} \quad T_s = \frac{3}{\omega_s} I_s^2 R'_2 \tag{i}$$

$$\text{Full-load torque} T_{\text{f1}} = \frac{3}{\omega_s} \frac{I_{f1}^2 R'_2}{S_{\text{f1}}} \tag{ii}$$

Dividing $$\frac{T_s}{T_{f1}} = \left(\frac{I_s}{T_{f1}}\right)^2 s_{f1}$$

$$25 \times 0.04 = 1 \text{ pu}$$

Remark: While the starting current is as high as five times full-load current, the starting torque just equals full-load torque. This corroborates the statement made earlier on starting.

Example 9.9

A three-phase squirrel-cage induction motor has a ratio of maximum torque T_m to full-load torque T_{fl} as 3.5 : 1. Determine the ratio of starting torque T_s to full-load torque for (a) direct starting, (b) star-delta starting, and (c) autotransformer starting with a tapping of 70%. The rotor resistance and standstill reactance per phase (delta) are 0.5 Ω and 5 Ω respectively. Neglect stator impedance.

Solution

$$T_m = K_T \frac{V^2}{2X_2}; \; V = \text{line voltage; Eq. (9.24)}$$

$$T_s = K_T \left(\frac{V^2 R_2}{R_2^2 + X_2^2}\right); \text{ Eq. (9.26)}$$

$$T_{f1} = \frac{T_m}{3.5} = \frac{K_T V^2}{7X_2} = \frac{K_T V^2}{35}$$

(a) Direct Start

$$\frac{T_s}{T_{f1}} = \frac{K_T V^2 R_2}{R_2^2 + X_2^2} \times \frac{35}{K_T V^2} = \frac{35 \times 0.5}{(0.5^2 + 5^2)} = 0.693$$

(b) Star-delta Starting

$$\frac{T_s}{T_{f1}} = \frac{K_T (V/\sqrt{3})^2 R_2}{R_2^2 + X_2^2} \times \frac{35}{K_T V^2} = \frac{35 \times 0.5}{3 \times (0.5^2 + 5^2)} = 0.231$$

(c) Autotransformer Starting

$$\frac{T_s}{T_{f1}} = \frac{K_T (0.7V^2) R_2}{R_2^2 + X_2^2} \times \frac{35}{K_T V^2} = 0.49 \times 0.693 = 0.4693$$

9.5.3 Speed Control

The speed of an induction motor is given by

$$n = (1 - s)\, n_s$$

$$= (1 - s)\frac{120f}{P} \tag{9.39}$$

Equation (9.39) suggests two methods of speed control, namely

- Slip control
- Frequency control

These are discussed below.

Slip Control

❑ **Voltage Control** Torque is proportional to the square of applied voltage [Eq. (9.24)]. The *T-s* characteristics for various voltages are drawn in Fig. 9.20. Also shown in this figure is a fan-type load characteristic. From the intersection points, it is easily seen that slip increases (speed drops) as the voltage is reduced. Because of the square law for fan torque, at lower voltages slip tends to increase disproportionately and the motor tends to draw a large current causing inefficient operation and motor overheating. The method is obviously unsuitable for constant-torque loads. Even for fan-type loads, it can only be used for small reduction in speed. It is used only in small motors where series resistance/reactances are employed for reducing the voltage applied to the motor.

❑ **Rotor Resistance Control** Resistance is included in the rotor circuit via slip-rings as shown in Fig. 9.16. Obviously, this type of control is only possible for a wound-rotor machine. Figure 9.18 shows the *T-s* characteristics for increasing values of rotor resistance along with the fan-type load characteristic. It is easily seen that the slip increases as the rotor resistance is increased.

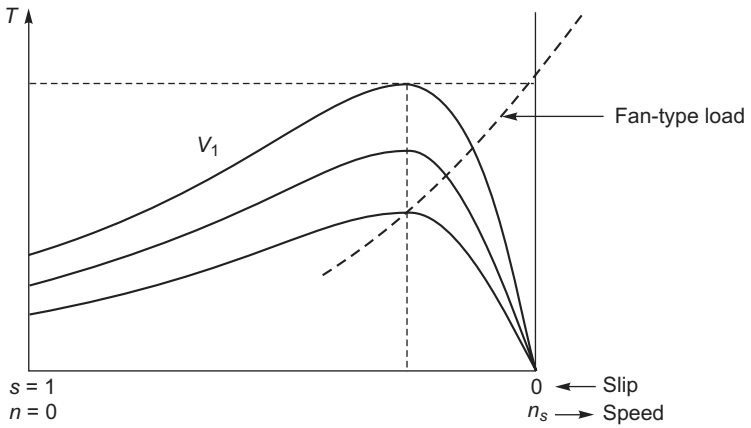


Fig. 9.17 *Speed control by voltage control*

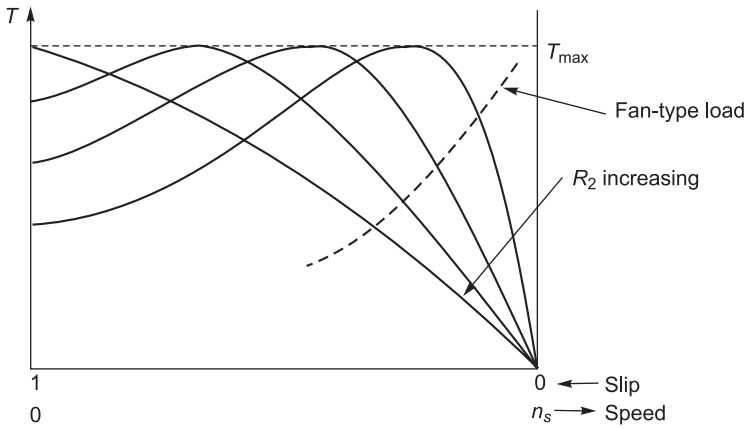


Fig. 9.18 *Rotor resistance control*

On approximate basis,

$$I_2 = \left(\frac{s}{R_2}\right)\left(\frac{V_1}{a}\right)$$

$$T = \frac{3}{\omega_s}\left(\frac{s}{R_2}\right)\left(\frac{V_1}{a}\right)^2$$

For constant load torque, as R_2 is increased, s increases proportionally and I_2 remains constant resulting in considerable increase in rotor resistance loss. At the same time, the output $T\omega$ decreases. Thus, the motor efficiency drops off sharply. The method is therefore useful only for small speed changes for short time periods in which case the starter resistance itself can be used for this purpose.

Frequency Control

In order to prevent abnormal rise in magnetising current at below normal frequency, V/f must be kept constant [Eq. (9.4)] so that air gap flux/pole remains fixed.

For constant (V/f), let us examine the effect on the breakdown torque. As per Eq. (9.26) reproduced below,

$$T_{BD} = \frac{3}{\omega_s}\frac{(V/a)^2}{2X_2}$$

$$\omega_s = \frac{120f}{P} \times \frac{2\pi}{60} = \left(\frac{4\pi}{P}\right) f$$

$$X_2 = 2\pi f L_2$$

Therefore,

$$T_{BD} = \frac{3}{\left(\frac{4\pi}{P}\right) f}\frac{(V_1/a)^2}{2(2\pi f L_2)} = K_{BD}\left(\frac{V_1}{f}\right)$$

We conclude that with constant (V/f), the breakdown torque remains constant. Variable frequency and voltage supply is obtained from a thyristor inverter, which is itself fed from an ac/dc converter as shown in Fig. 9.19. Like in a dc motor, a wide range of speed control becomes possible by this method. It is, however, expensive as a full-rated converter and inverter are needed.

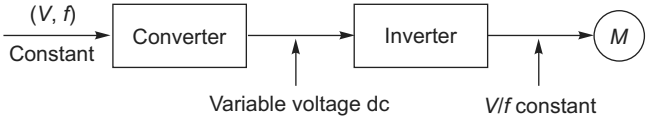


Fig. 9.19 *V/f control of induction motor*

9.7 HIGH-EFFICIENCY INDUCTION MOTORS

With the ever-increasing energy cost, the lifetime operating cost of an induction motor can be traded against a high efficiency and a high capital cost. With rising demand for high efficiency or energy-efficient induction motors, designers and manufacturers are stepping up their production of such motors.

Example 9.10

The rotor of a 6-pole, 50 Hz, slip-ring induction motor has a resistance of 0.25 Ω/phase and runs at 960 rpm. Calculate the external resistance/phase to be added to lower the speed to 800 rpm, with the load torque reducing to 3/4 of the previous value. Assume stator impedance to be negligible.

Solution For the range of slip considered,

$$R'_2/s >> X'_2 \tag{i}$$

$$T = \left(\frac{3}{\omega_s}\right)\left(\frac{sV_1}{R'_2}\right) = k\frac{s}{R'_2} \tag{ii}$$

At 960 rpm: $s = (1000 - 960)/1000 = 0.04$

At 800 rpm: $s = (1000 - 800)/1000 = 0.2$

$$T = k(0.04/0.25) \tag{iii}$$

$$(3/4)\ T = k\ [0.2/(0.25 + R_2\ (\text{ext}))] \tag{iv}$$

Dividing Eq. (iii) by Eq. (iv), we get

$$4/3 = \frac{0.25 + R_2(\text{ext})}{0.2 \times 0.25} \times 0.04/0.25$$

Solving, we get R_2 (ext) = 1.42 Ω

Example 9.11

A 6-pole, 50 Hz slip-ring induction motor has a rotor resistance of 0.25 Ω and a maximum torque of 180 Nm, while it runs at 860 rpm. Calculate (a) the torque at 4.5% slip, and (b) the resistance to be added in the rotor circuit to obtain the maximum torque at starting.

Solution

$$s_{\max T} = (100° - 860)/1000 = 0.14$$

$$R_2 = 0.14\ X_2 \text{ (for max. torque)}$$

$$\therefore \quad X_2 = 0.25/0.14 = 1.79\ \Omega$$

$$T_{\max} = \frac{3}{\omega_s}\left(\frac{0.5(V_1/a)^2}{X_2}\right) = k/X_2$$

$$180 = k/1.79 \text{ or } k = 322.2$$

(a) Now at slip $s = 0.045$

$$T = \left(\frac{3}{\omega_s}\right)\left(\frac{(V_1/a)^2}{(R_2/s)^2 + X_2^2}\right)$$

$$R'_2/s = \frac{2 \times 100.6}{(0.25/0.045)^2 + (1.79)^2} \times \frac{0.25}{0.045}$$

(b) For maximum torque at starting,

$$R_2 + R_2(\text{ext}) = X_2 = 1.79\ \Omega$$

or $$R_2\ (\text{ext}) = 1.79 - 0.25 = 1.54\ \Omega.$$

Example 9.12

A 400 V, 5 kW, 50 Hz induction motor runs at 1445 rpm at full load. The rotational losses are 285 W. If the maximum torque occurs at 900 rpm, calculate its value.

Solution Mechanical output = 5000 W

Rotational loss = 285 W

Mechanical power developed,

$$P = 5285 \text{ W}$$

$$\text{Slip } s = (1500 - 1445)/1500 = 0.0367$$

$$P_m = 3\left(\frac{1}{s} - 1\right) I'^2_2 R'_2 \tag{i}$$

Ignoring stator impedance

$$I'_2 = V/[R'_2/s + X'^2_2]^{0.5} \tag{ii}$$

Substituting I'_2 from Eq. (ii) in Eq. (i), we get

$$P_m = 3\left(\frac{1}{s} - 1\right)\frac{V_1^2 R'_2}{(R'_2/s) + X'^2_2} \tag{iii}$$

Substituting values,

$$5285 = 3\,(1/0.0367 - 1) \times \frac{(400/\sqrt{3})R'_2}{(R'_2/0.0367)^2 + X'^2_2} \tag{iv}$$

or

$$0.94\,R'^2_2 + 0.00126\,X'^2_2 = R'_2 \tag{v}$$

At maximum torque,

$$s = (1500 - 900)/1500 = 0.4$$

$$R'_2 = 0.4\,X'_2 \tag{vi}$$

Solving Eqs (v) and (vi), we get

$$X'_2 = 2.65\ \Omega,\ R'_2 = 1.06\ \Omega,$$

Now,

$$T_{\max} = \frac{3}{\omega_s}\frac{0.5V_1^2}{X'_2} \tag{vii}$$

$$\omega_s = (2\pi \times 1500)/60 = 50\,\pi \text{ rad/s}$$

$$T_{\max} = (3/50\,\pi)\left\{\frac{0.5(400/\sqrt{3})^2}{2.65}\right\}$$

$$= 192.2 \text{ Nm}$$

Example 9.13

A three-phase induction motor runs at a speed of 940 rpm at full load when supplied form a 50 Hz, three-phase mains.

(a) How many poles does the motor have?

(b) What is its percent slip at full load?
(c) What is the corresponding speed of
  (i) the rotor field w.r.t. the rotor surface?
  (ii) the rotor field w.r.t. the stator?
(d) What would be the rotor speed at twice full-load slip?

Solution

(a) $n_s = 1000$ rpm $P = (120 \times 50)/1000 = 6$
(b) s = (1000 – 940)/1000 = 6%
(c) (i) 1000 – 940 = 60 rpm
  (ii) 960 + 40 = 1000 rpm
(d) $s = 2 \times 6 = 12\%$
  $n = 1000 - (12 \times 1000)/100 = 880$ rpm

Example 9.14

In Example 9.13, what would be the slip and speed at full-load torque if the total resistance of the rotor is doubled (by addition of external resistance through slip rings)?

Solution Figure 9.20 shows the rotor circuit with added external resistance. For the same torque, the rotor current must remain the same. ($T = K_T I_2$, for fixed stator voltage). Thus,

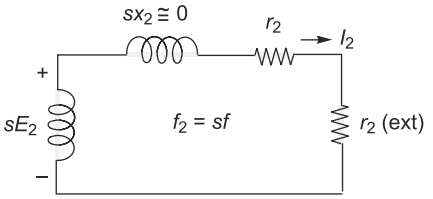


Fig. 9.20

$$\frac{sE_2}{r_2} = \frac{sE_2}{2r_2}$$

or $s' = 2s = 12\%$

$n = 1000 - (12 \times 1000)/100 = 880$ rpm

Remark: This indeed is a method of controlling the speed of a wound rotor induction motor.

Example 9.15

A three-phase, 50 Hz induction motor runs at 965 rpm.
(a) Calculate the number of motor poles.
(b) What is the slip and frequency of the rotor currents?
(c) What is the speed of the stator field with respect to rotor and with respect to rotor field?

Solution

(a) $$\frac{120f}{P} = \frac{120 \times 50}{P} \approx 965$$

or $P \approx 6.12$. So $P = 6$, $n_s = 1000$ rpm

(b) Slip, $$s = \frac{1000 - 965}{1000} = 0.035$$

Rotor frequency, $f_2 = s_{f1} = 0.035 \times 50 = 1.75$ Hz

(c) Speed of stator field relative to rotor surface = 1000 – 965
= 35 rpm (forward)

Speed of rotor field with respect to rotor surface

$$= \frac{120 \times 1.75}{6} = 35 \text{ rpm (forward)}$$

Speed of stator field with respect to rotor field
= 1000 – (965 + 35) = 0, stationary

Example 9.16

A three-phase, 50 Hz, 4-pole, 400 V wound rotor induction motor has delta-connected stator and star-connected rotor winding. Assume that effective stator to rotor turn ratio of 2:1 For a rotor, speed of 1440 rpm, calculate

(a) the slip,
(b) the rotor frequency, and
(c) the rotor induced emf line-to-line and sketch the rotor circuit.

Solution

(a)
$$n_s = \frac{120 \times 50}{4} = 1500 \text{ rpm}$$
$$n = 1440 \text{ rpm}$$
$$\text{slip} = \frac{1500 - 1440}{1500} = 0.04$$

(b) Rotor frequency, $f_2 = s_f = 0.04 \times 50 = 2$ Hz

(c) Stator induced emf = applied voltage; E_1 (phase) = 400 V (delta)
Rotor induced emf (phase) at 50 Hz.
As per turn ratio,

$$E_2 \text{ (50 Hz)} = \frac{400}{2} = 200 \text{ V (star phase)}$$

At slip $s = 0.04$ $f_2 = 2$ Hz

$$E_2 \text{ (2 Hz)} = 200 \times \frac{2}{50} = 8 \text{ V}$$

$$E_2 \text{ (line)} = \sqrt{3} \times 8 = 13.856 \text{ V}$$

❑ **Rotor Circuit (Phase)** The circuit has rotor resistance in series with reactance sx_2, where x_2 in the rotor reactance at $s = 1$ (50 Hz). Rotor induced emf = sE_2. The circuit is drawn in Fig. 9.21.

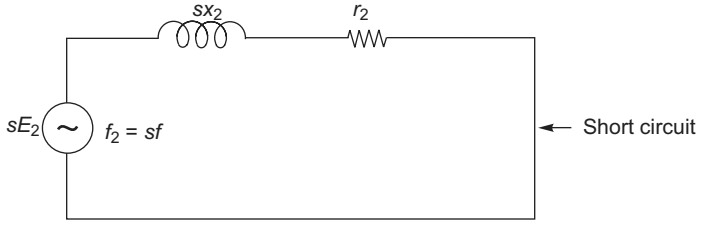


Fig. 9.21

Summary

- Induction motors are of two types:

  Squirrel-cage induction motor—Copper/aluminium bars in rotor slots shorted by end rings. Aluminium is commonly used being of low cost.

  Wound-rotor or slip-ring induction motor—The rotor has three-phase windings with connections brought out through three slip-rings, the winding is shorted externally, also external resistance can be included at the time of starting; expensive and used only where high-starting torque is must.

- Results and statements made here are on per phase basis, powers—active and reactive on three-phase basis. Winding connection will be assumed star (or equivalent star) except where specified otherwise.

- Stator resistance and leakage reactance ignored

  $V_l \approx E_1 = \sqrt{2}\pi K_{w1} N_{ph1}(\text{series}) f \Phi_r$

  f = stator frequency (frequency of V_1), Φ_r = resultant air-gap flux

- Exciting current

  $\bar{I}_0 = \bar{I}_m + \bar{I}_i$

  I_m = magnetising current; 90° lagging
  I_i. = core loss current; in-phase
  Magnitude-wise, $I_m >> 1$.
  PF of I_0 is very low, phase angle slightly less than 90°.

- Rotor standstill emf E_2, frequency same as stator

- At speed n (slip, s)
  Rotor induced emf = sE_2
  Rotor frequency $f_2 = sf$

- $\frac{\bar{I}'_2}{I_2} = \frac{I}{a}$; I'_2,' stator current to counter I_2

- The net stator current

  $$\bar{I}_1 = \bar{I}_0 + \bar{I}'_2 = \bar{I}_0 + \left(\frac{I}{a}\right)\bar{I}_2$$

  I_0 is almost 40% of I_1 (full-load)

- **Power factor**

  Because of large I_0 with phase angle slightly less than 90°, the pf of the line current is of the order of 0.8 to 0.85. At light load, I'_2 reduces and so does the power factor. Therefore, induction motor should not be run at light load for long period of time.

- Rotor standstill reactance = X_2
  Rotor circuit impedance

  $\bar{Z}_2 = R_2 + j\, s\, X_2$

- **Power across air gap**

  P_G = Gross mechanical power output + rotor copper loss

  $= P_m + 3\, I_2^2\, R_2$

➢ Rotor resistance equivalent of mechanical power output

$$\left(\frac{1}{s}-1\right)R_2$$

which means

$$\frac{P_m}{3}=\left(\frac{1}{s}-1\right)I_2^2 R_2$$

➢ **Circuit model**

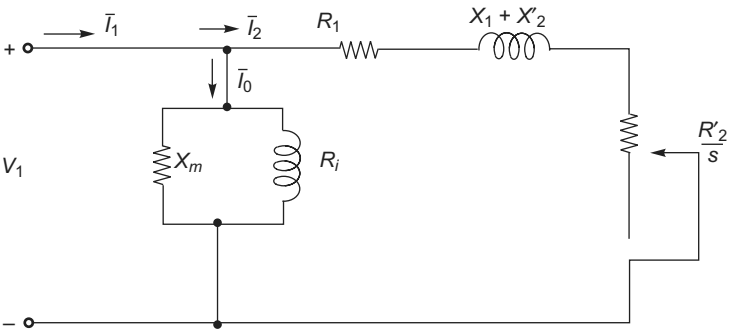


Fig. 9.20

➢ $P_G = 3\dfrac{I_2 R_2}{s} = 3\dfrac{I_2^2 R_2}{s}$

$P = (1 - s)P_G$

$T = \dfrac{P_G}{\omega_s}$, ω_s = synchronous speed in rad (mech)/s

P_G is known as torque in *synchronous watts*

➢ $T = \dfrac{3}{\omega_s}\cdot\dfrac{V_1^2(R'_2/s)}{(R'_2/s)+X_2^2} = \dfrac{3}{\omega_s}\cdot\dfrac{(V_1/a)^2(R_2/s)}{(R_2/s)^2+X_2^2}$

Stator impedance ignored

➢ Torque-slip characteristic; see Fig. 9.10
Motoring $0 \le s \le 1$
Generating $s < 0$
Breaking $s > 1$

➢ $T_{max} = T_{breakdown}$ (T_{BD})
For $T > T_{BD}$; motor stalls

➢ **Resistance added in rotor circuit**—slip-ring induction motor only. T_{BD} no change, slip at given torque increase, motor speed reduces, $T_{(start)}$ increases.

➢ At T_{max}
$R_2 = s_{max\ T} X_2$
$R_2 = S_{max\ T} X_2$

$$T_{max} = T_{BD} = \frac{3}{\omega_s}\left(\frac{V_1^2}{2X'_2}\right) = \frac{3}{\omega_s}\left(\frac{(V_1/a)^2}{2X^2}\right)$$

Stator impedance ignored.

➢ Starting—stator impedance ignored

$$I_{2(start)} = \frac{V_1}{\sqrt{R_2^2 + X'^2_2}} = \frac{V_1/a}{\sqrt{R_2^2 + X_2^2}}$$

$$T_{(start)} = \frac{3}{\omega_s}\left[\frac{V_1^2\, R'_2}{\sqrt{R'^2_2 + X_2^2}}\right] = \frac{3}{\omega_s}\left[\frac{(V_1/a)^2\, R_2}{R_2^2 + X_2^2}\right]$$

➢ **Determination of circuit model parameters**

Quantities measured in test: voltage, current and power

No-load test
Conducted at rated voltage

Determines
Sum of core loss and windage and friction loss and X_m, R_i.

Blocked rotor test
Conducted at reduced voltage, full-load current

Determines
Full-load copper loss

R_2, X_2

Important Note
In the computation of performance based, the circuit model as determined by the above two tests, the windage and friction loss is accounted for in R_i. Therefore, the mechanical power output $P_m = 3\left(\frac{1}{s} - 1\right) I'^2_2\, R_2$ is the net mechanical power output called the *shaft power*.

➢ **Methods of starting**

Squirrel-cage motor
DOL (direct-on-line) starting not permitted for motors of 5 kW and above. As the motor current is 5 to 6 times full-load current, the power supply companies do not allow such heavy short-time currents to be drawn.
—*Reduced voltage start*
—*Series resistance starting*—can be used for fractional kW motor only
—*Star/delta starting*

Start in star, run in delta

Starting current and torque both reduce by a factor of 1/3.

—*Autotransformer starting*

Expensive, used for very large motors

Both starting current and torque reduce by a factor of a^2; a = voltage reduction factor

➢ **Speed control**—slip control, frequency control

—*Slip control*—reduced voltage for very small motors, inefficient

—*Rotor resistance control* for slip-ring induction motor, reduce efficiency drastically, not suitable

—*Frequency control*—in varying frequency (V/f) must be maintained constant for constant air-gap flux

Requires expensive full rated thyristor convertor/inverter equipment

Exercises

Review Questions

1. Give a brief account of squirrel-cage induction motor. Explain qualitatively as to how it develops torque and the nature of its torque-slip characteristic. Why is it called asynchronous motor?
2. What is the effective turn-ratio of an induction motor?
3. What is standstill rotor emf and what is its frequency? How does the emf magnitude and frequency vary with speed?
4. Explain what is meant by standstill reactance of induction motor. How does it vary with speed?
5. The stator of a slip-ring induction motor with slip-ring terminals open-circuited has at stator excited from three-phase source. The rotor is run by a prime mover. What will be the frequency of rotor induced emf at the following speeds?
   (a) Half synchronous speed in the same direction as the air-gap field (AGF)
   (b) Half synchronous speed in opposite to AGF
   (c) At synchronous speed in opposite direction to AGF
6. What is meant by the excitation current of an induction motor? Draw its phasor diagram with applied voltages as the reference phasor showing its components. Which is the larger component and why?
7. What is the difference between excitation current and no-load current?
8. Draw the phasor diagram of an induction motor showing applied voltage, magnetising, core loss, load current and the line current. Label each component.
9. Write the expression for the resistance in the circuit model, the loss in which it is equivalent to the mechanical power developed.
10. What is meant by the torque in synchronous watts? Write its expression in terms of circuit model quantities and then find the torque developed.
11. Show that the maximum torque occurs at a slip $s = \dfrac{X_2}{R_2}$ and further show that $T_{\max}$ is independent of s.
12. Draw the T-s characteristic of an induction motor. Indicate the region where the characteristic is nearly linear.
13. Show that the motor can operate stably at $s \angle s_{\max T}$. Use perturbation technique.
14. Neglect the stator impedance and show that the maximum power output (developed power) occurs at slip $s = \dfrac{R_2 + \sqrt{R_2^2 + X_2^2}}{R_2}$.

    Hint: In the circuit model of Fig. 9.7, use maximum power transfer theorem. The magnitude of fixed impedance should match $\left(\dfrac{1}{s} - 1\right) R_2$
15. Show that at supersynchronous speed, the induction machine acts as a generator. Write the expression for P_G. In which direction does it flow? How can you find the net mechanical power input and net electrical power output?

16. Neglecting stator impedance, derive the expression for the starting torque of an induction motor. Show that it increases with rotor resistance. At what resistance value does it reach the maximum? Resistance added to the rotor of a slip-ring induction motor.
17. Show that in star/delta starting of squirrel-cage induction motor, the starting current and torque get reduced by a factor of 1/3 compared to DOL starting.
18. Elaborate the statement "rotor resistance starting of slip-ring induction motor reduces starting current and increases starting torque".
19. The power input on no-load running of induction motor is consumed in what losses?
20. The power input in blocked rotor test at reduced voltage is consumed in what losses?
21. No-load test determines what parameters of the circuit model of induction motor?
22. Which parameters of the circuit model of induction motor are determined by the blocked-rotor test?
23. Why is DOL starting current very high but the starting torque is still low? Why is DOL not permitted in starting even though the short-duration current cannot harm the motor?
24. What methods are used in starting squirrel-cage induction motor? Which method is used in what size of motor? Which is the most common method and what is it superiority?
25. State the conditions for two interacting rotating fields to create steady torque.
26. Explain the process of how an induction motor develops torque when ac supply is connected to its stator. Why cannot it develop torque at synchronous speed?
27. Define slip of an induction motor. At full load, what is the range of the value of slip.
28. What is the frequency of the rotor currents of an induction motor?
29. Why is an induction motor called asynchronous motor?
30. List the type of losses in as electric machine. What is the nature of each loss?
31. What is the relative speed between stator and rotor rotating fields in an induction motor?
32. Sketch the torque-slip characteristic of an induction motor. Explain the nature of the low slip part of the characteristic. Locate on the characteristic the full-load torque operating point.
33. Explain how an induction motor can self-start but cannot run at synchronous speed.
34. Explain why rotor-induced emf is proportional to slip.
35. Distinguish between time phase difference and space phase difference.
36. State the condition of maximum efficiency of an electric machine. Compare it with that of a transformer.
37. Compare the speed control features of induction motor with dc shunt motor.
38. From no-load to full-load, what is the type of speed-load characteristic of induction motor?
39. Compare and contrast the squirrel-cage and slip-ring induction motors.
40. Upon reducing the load on an induction motor, why does its pf come down?

Problems

1. A 40 kW, 440 V, three-phase, 50 Hz, 8-pole squirrel-cage induction motor has a slip of 0.03 when operated at rated voltage and frequency. It has full-load line current of 68.9 A and an efficiency of 89.6%.
   Find (a) the shaft torque delivered to the load, and (b) the power factor at which the motor operates.
2. A 7.5 kW, 440 V, three-phase, 50 Hz, 6-pole squirrel-cage induction motor operates at a full-load slip of 4.0% when rated voltage and frequency are impressed. Assume that the torque-slip characteristic is linear (Eq. (9.43)). What would be the motor speed if the load torque is increased to 125%, while the impressed voltage is reduced to 80% of the rated value.
3. The no-load test data yielded the following parameters (on star basis) for the shunt branch of the circuit model of a 400 V, 50 Hz, 4-pole induction motor.
   $X_m = 31.25\ \Omega$, $R_i = 242$ Q.
   The motor develops a torque of 95.6 Nm at a slip of 5%. Calculate
   (a) mechanical output,

(b) rotor copper loss, and
(c) motor efficiency.

4. Assuming for an induction motor the stator iron loss to be negligible, derive an expression for efficiency as a function of s in terms of stator and rotor circuit parameters. A three-phase, 6-pole induction motor rated 7.5 kW, 400 V, 50 Hz has the following impedance parameters referred to the stator:
$R_1 = 0.975\ \Omega$; $R'_2 = 0.496\ \Omega$,
$X_1 + X'_2 = 2.38\ \Omega$
Calculate the motor efficiency at slips of 0.04, 0.1 and 0.5.
5. A three-phase, 400 V, 5 kW/50 Hz, 6-pole induction motor with star-connected stator gave the following test results:

No load	400 V	3.5 A	444.5 W
Blocked rotor	200 V	16.7 A	2220 W

Stator phase resistance = 1.25 Ω
Calculate the line current, power factor and efficiency at a speed of 935 rpm.
Calculate also the maximum torque and the speed at which it occurs.
6. The motor of Ex. 9.13 is to drive at a constant torque with a load of 250 Nm. Given effective turn ratio, stator/rotor = 2.45/1.
(a) Calculate the minimum rotor resistance to be added in the rotor circuit for the machine to start up. Ignore variations in mechanical loss due to change in speed.
(b) At what speed will the motor run if the added resistance is (i) left 1 in, and (ii) subsequently shorted out?
(c) To what value must the applied voltage be reduced if the speed in part (b) (i) above if is to be achieved with normal rotor resistance?
(d) Compare also the motor efficiency for these two methods of speed control.
7. A three-phase, 6-pole induction motor rated 7.5 kW, 400 V, 50 Hz has the following impedance parameters referred to the stator:
$R_1 = 0.975\ \Omega$, $R'_2 = 0.496\ \Omega$
$X_1 + X'_2 = 2.38\ \Omega$
The motor is driving a load requiring torque of
$T_L = 75\ (n/ns)^2$ Nm
(a) Determine the speed at which the motor would run at rated terminal voltage.
(b) What would be the motor speed if the terminal voltage is reduced by 15%?
8. A three-phase squirrel-cage induction motor is started by reducing the applied voltage by a factor of 1/2. The exciting current can be ignored. Find the factor by which
(a) the starting current is reduced, and
(b) the starting torque is reduced.
9. A 25 kW, 400 V, three-phase, 50 Hz, 6-pole, delta-connected squirrel-cage motor has the following circuit model parameters:
$R_1 = 0.45\ \Omega$, $R'_2 = 0.36\ \Omega$ per phase
$X_1 + X'_2 = 4.5\ \Omega$ per phase
(a) Estimate the starting line current and torque for DOL starting.
(b) Repeat part (a) if the motor is reconnected in star.

Multiple-Choice Questions

1. At low slip, the torque-slip characteristic is

(a) $T \propto \frac{1}{s^2}$ (b) $T \alpha s^2$ (c) $T \propto \frac{1}{s}$ (d) $T \propto s$

2. For maximum starting torque in an induction motor

   (a) $r_2 = 0.5\, x_2$ (b) $r_2 = x_2$ (c) $r_2 = 2x_2$ (d) $r_2 = 0$

3. During the blocked rotor test on an induction motor, the low is drawn mainly for
   (a) copper loss and core loss
   (b) copper loss
   (c) core loss,
   (d) copper loss, core loss and windage and friction loss

4. If the stator impedance is neglected, the maximum starting torque in an induction motor occurs at (usual symbols are used)

   (a) $r_2 = 2x_2$ (b) $r_2 = x_2$ (c) $r_2 = \frac{1}{2}x_2$ (d) $r_2 = 0$

5. The stator and rotor of an induction machine act like
   (a) an ordinary rotor-winding transformer
   (b) a variable frequency transformer with fixed frequency
   (c) a variable voltage transformer with fixed frequency
   (d) a variable frequency and voltage transformers with *V/f* remaining constant.

6. The breakdown torque in an induction motor, is obtained at a slip of (stator impedance is ignored)

   (a) $(x_2/r_2)^2$, (b) x_2/r_2 (c) r_2/x_2 (d) $(r_2/x_2)^2$

7. During the blocked rotor test on an induction motor, the power from the mains is drawn mainly for

   (a) copper, core and mechanical loss (b) copper and core loss
   (c) core loss (d) copper loss

8. The power input to an induction motor is 50 kW when it is running at 4% slip. The stator resistance and core loss are assumed negligible. The torque developed in synchronous watts is

   (a) 48 W (b) 52 kW (c) 50 kW (d) 2 kW

9. The starting current of an induction motor is five times the full load current while its full load slip is 4%. The ratio of the starting torque to the full-load torque is

   (a) 0.6 (b) 0.8 (c) 1.0 (d) 1.2

10. In an induction motor, *Pc* is the power across the air gap when running at slip *s*. Its rotor copper loss and mechanical output respectively are

    (a) sPG, $(1 - s)\, P_c$ (b) $(1 - s)\, PG$, PG/s
    (c) $P_c/(1 - s)$, P_c/s (d) $P_c\,(1 - s)$, sPG

Answers

Multiple-Choice Questions

1. (d) 2. (b) 3. (b) 4. (b) 5. (c)
6. (c) 7. (d) 8. (a) 9. (c) 10. (a)

Fractional kW Motors

chapter 10

Goals & Objectives

- To familiarise with construction, operation and special importance and application of fractional kW motors
- To explain how they are different than their 3-phase counterparts
- Uses in domestic applications

10.1 INTRODUCTION

In Chapters 8 and 9, three-phase ac motors, which are used for high-power rating applications, have been discussed. For reasons of economy, most homes, offices and also rural areas are supplied with single-phase ac, as the power requirements of individual load items are rather small. Even though input point power to homes or offices may be three-phase, the inside wiring is single-phase, 220–230 V for reasons of safety. This has led to the availability of a wide variety of small-size motors of fractional kilowatt ratings. These motors are employed in fans, refrigerators, mixers, vacuum cleaners, washing machines, other kitchen equipment, tools, small farming appliances, etc. Individual room air conditioners (single-phase) for home and office (where there is no central air conditioning) are being increasingly used.

Obviously, the total number of such small motors in use far exceeds the number of integral kW motors in industrial use. Though these motors are simpler in construction as compared to their three-phase counterparts, their analysis happens to be more complex and requires certain concepts, which have not been developed so far. Also, the design of such motors is carried out by trial and error till the desired prototype is achieved. Because of the vast numbers in which these motors are produced, even a fractional efficiency increase or a marginal cost saving is extremely important. Nowadays, as in other fields, computers are employed for more accurate and optimum paper designs.

The treatment of the fractional kW motors as presented in this chapter is concerned mainly with their method of operation, classification and characteristics of various types, and their typical applications. The analysis of the performance of such motors is beyond the scope of this book.

10.2 SINGLE-PHASE INDUCTION MOTORS

A single-phase induction motor comprises a single-phase winding on the stator and a squirrel-cage rotor as shown in Fig. 10.1. The stator winding is connected to a single-phase source. The winding mmf is

$$F = F_m \cos \omega t \cos \theta; \text{ (see Eq. (8.19))} \tag{10.1}$$

where $F_m = NI_m$

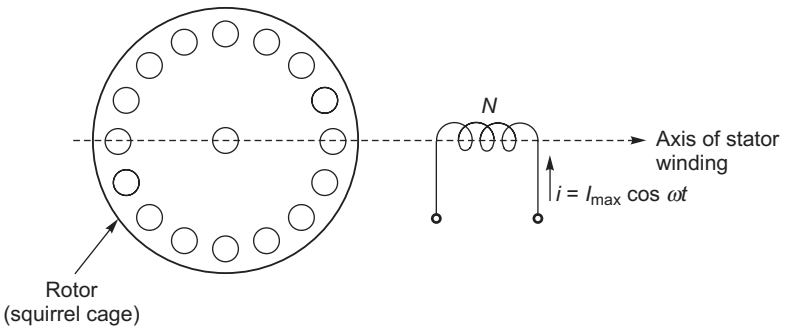


Fig. 10.1 *Single-phase induction motor*

As per Sec. 8.5, this pulsating space-distributed field can be split into time rotating fields as

$$F = \frac{1}{2}F_m(\omega t + \theta) + \frac{1}{2}F_m \cos(\omega t - \theta) \tag{10.2}$$

$$= F_f + F_b$$

or vectorially

$$\mathbf{F} = \mathbf{F}_f + \mathbf{F}_b \tag{10.3}$$

where $\mathbf{F}_f$ and $\mathbf{F}_b$ are respectively forward and backward rotating fields rotating at synchronous speed ($\omega = 2\pi f$ rad(elect/s)). Each field has the same peak mmf equal to ½ F_m.

10.2.1 Rotor Slip with Respect to Two Rotating Fields

Let the rotor be assumed to run at a speed n in the direction of the forward field as shown in Fig. 10.2. It easily follows that

Rotor slip w.r.t. forward field,

$$s_f = \frac{n_s - n}{n_s} = s \tag{10.4}$$

Rotor slip w.r.t. backward field,

$$s_b = \frac{n_s - (-n)}{n_s} = \frac{2n_s - (n_s - n)}{n_s}$$

$$= (2 - s) \tag{10.5}$$

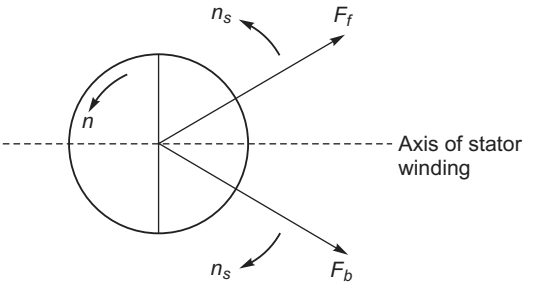


Fig. 10.2 *Rotor slip*

At $s = 0.05$ say,

$$\frac{s_f}{s_b} = \frac{0.05}{1.45} = \frac{1}{39}$$

At $s = 1$ (standstill rotor),

$$s_f = s_b = 1$$

10.2.2 Torque-Speed Characteristic

At standstill, the rotor slip is $s = 1$ w.r.t both the rotating fields. The two fields are therefore equal in strength inducing equal currents in the rotor. As a result, these produce equal but opposite torques with net zero torque. The single-winding, single-phase motor (Fig. 10.1) is therefore *non-self starting*. The two rotating fields induce stator emfs, which together balance the applied voltage (if low impedance stator is assumed).

If the rotor is made to run now at speed n in the direction of the forward field, the rotor slips w.r.t. the two fields are now vastly different, i.e. $(2 - s) >> s$. The forward field (low rotor slip) induces low, high pf currents in the rotor while the backward field (high rotor slip $(2 - s)$) induces high, low pf currents in the rotor. As a consequence, the backward field gets highly attenuated in strength while the strength of the forward field enhances in comparison. The forward torque, therefore, becomes several times the backward torque (torque being nearly proportional to square of field strength). The single-phase induction motor in this region of slip has *T-s* characteristic similar to that of a three-phase motor but has a low efficiency because of the rotor loss caused by the backward field.

The *T*-s characteristic of a single-winding single-phase induction motor as sum of forward and backward field *T-s* characteristics is shown in Fig. 10.3, from which it is obvious that the motor has no starting torque.

The problem posed now is how to create a starting torque. This will be tackled by strengthening the forward field and weakening the backward field at $s = 1$.

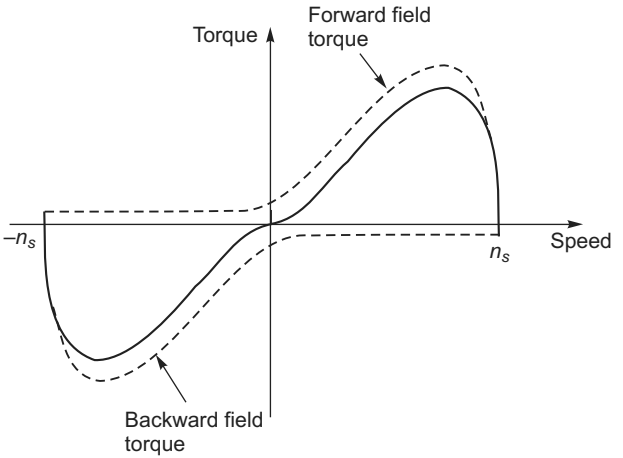


Fig. 10.3 *T-s characteristic of a single-winding, single-phase induction motor*

10.2.3 Two-Phase Motor

Figure 10.4 shows a 2-phase motor. Let

$$\sqrt{2}\, N_m I_m = \sqrt{2}\, N_a I_a = F_m$$

The windings are displaced 90° (elect) in space phase and carry currents with 90° time phase difference. The resultant mmf distribution is

$$\begin{aligned} F &= F_m \cos \omega t \cos \theta + F_m \cos(\omega t - 90°) \cos(\theta - 90°) \\ &= F_m \cos(\omega t - \theta) \qquad (10.6) \\ &= F_f \end{aligned}$$

A single rotating field is thus established rotating at synchronous speed. But the problem now is to create these currents on the 2-phase windings. A 2-phase supply would be necessary, which is not practicable.

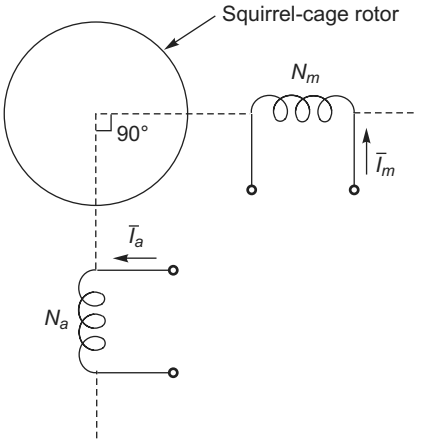


Fig. 10.4 *Two-phase motor*

10.2.4 Split-Phase Motor

It is a 2-winding, single-phase motor, in which the two windings are placed at 90° (elect) but are fed from single phase. The time phase difference in winding currents is obtained by placing suitable impedance in series with one of the windings called the *auxiliary winding* '*a*' while the other winding is called the *main winding m*. The current I_a in the higher impedance auxiliary winding is less than the current I_m in the main winding. The auxiliary winding has fewer turns of thinner wire. Unbalanced 2-phase field conditions are thus created at the start and as a result, the forward rotating field becomes sufficiently stronger than the backward field, resulting in production of starting torque. The auxiliary winding may or may not be left in circuit after the motor starts. For opening the auxiliary winding after motor starts, a centrifugal switch is employed. After starting, the motor runs only on the main winding.

Depending on the method of phase-splitting (causing time phase difference in the currents of the two windings), there are two types of single-phase motors.

Resistance Split-Phase Motor

The schematic diagram of the resistance split-phase motor is shown in Fig. 10.5. Here, high *R*/*X* ratio is used for the auxiliary windings.

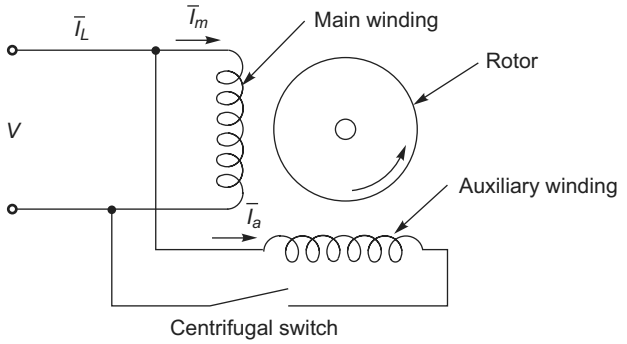


Fig. 10.5 *Resistance split-phase motor*

A phase difference of about 30° is achievable as shown in Fig. 10.6(a) while Fig. 10.6(b) gives a typical *T-s* characteristic.

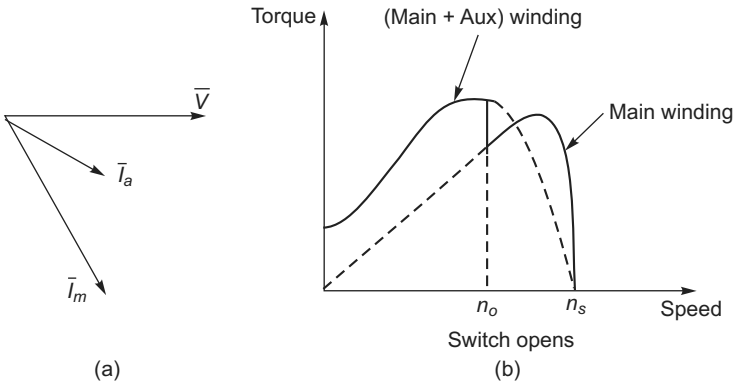


Fig. 10.6 *(a) Phasor diagram at start (b) T-s characteristic*

It is a low efficiency, low pf motor and is available in sizes of 1/20 – 1/2 kW.

Capacitor Split-Phase Motor

For phase splitting, a capacitor is placed in series with the auxiliary winding as shown in Fig. 10.7 along with phasor diagram at start. While the main winding draws a lagging current, the current in the auxiliary winding is leading and it is possible to make the phase difference between them as 90° at start. During running, the auxiliary winding is cut out so that capacitor is only short-time rated. Such a motor is known as capacitor-start motor. It has a far larger starting torque compared to a resistance-start motor. It has wide applications in machine tools, refrigeration, air-conditioning, etc. and is available in up to 5 kW size.

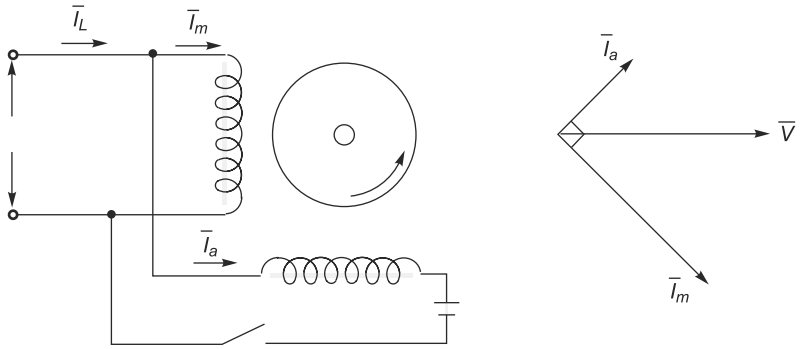


Fig. 10.7 *Capacitor-start motor*

10.2.5 Two-Value Capacitor Motor

The connection diagram is given in Fig. 10.8. A larger capacitance [*C* (run) and *C* (start) in parallel] is employed to yield best starting conditions. The phase separation is adjusted to more than 90° [Fig. 10.9(a)]. The *C* (start) is cut out at a certain speed leaving *C* (run) in circuit to give best running performance; phasor diagram of Fig. 10.9(b). *C*(run) also helps to improve the overall pf of the motor. While *C* (run) is continuous rated, *C* (start) need only the short-time rated. The composite *T-s* characteristic is shown in Fig. 10.10. This motor is employed for hard to start loads.

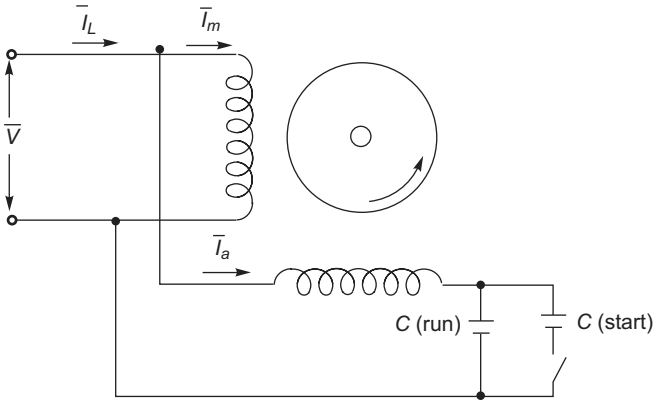


Fig. 10.8 *Two-value capacitor motor*

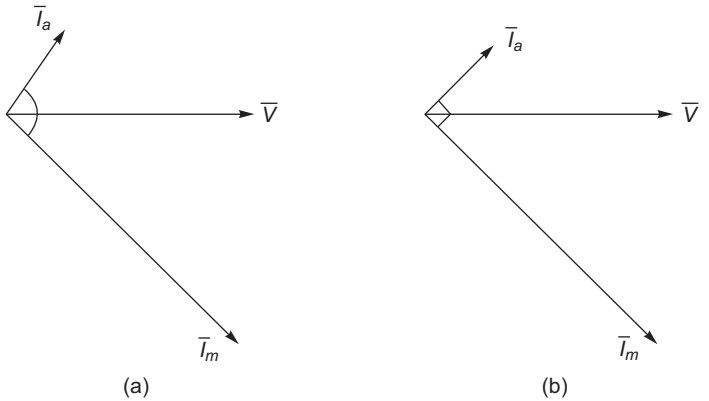


Fig. 10.9 *Phaser diagram two-value capacitor motor: (a) At start (b) During running*

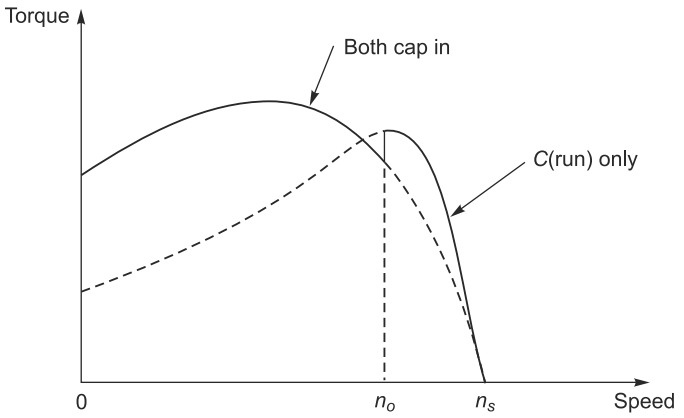


Fig. 10.10 *T-s characteristic two-value capacitor motor*

10.2.6 Shaded-Pole Motor

Figure 10.11 shows a shaded-pole motor. It has a projecting pole stator excited from single-phase ac while part of the poles is enclosed by short-circuited shading coils (sometimes a single shading ring is employed). The shading coil has a large lagging current induced in it, which produces a lagging flux. As a consequence, the resultant flux passing down the shaded portion of each pole lags behind the flux passing down the remaining portion. This difference in phase angle of the two portions of flux causes the production of starting torque.

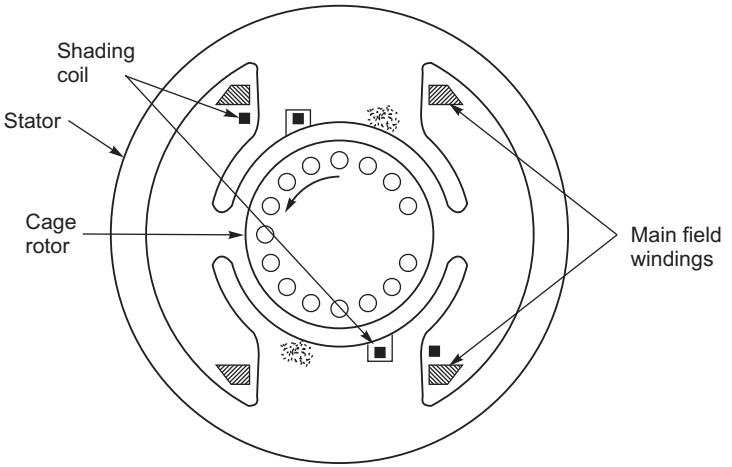


Fig. 10.11 *Shaded-pole motor*

The direction of rotation of the rotor is from the leading flux portion of the pole to the lagging flux portion of the pole, i.e. from the unshaded to the shaded part of the pole. It is as if the flux glides part the rotor surface from the leading to the lagging part of the pole. Reversal of direction of rotation is possible only by providing shading coils at both the pole ends and open circuiting one of these.

Shaded-pole motor inherently has low pf and is available in sizes up to 1/20 kW. It finds application in small fans, convectors, vending machines, photocopying machines, advertising displays, etc.

10.3 SINGLE-PHASE SYNCHRONOUS MOTORS

10.3.1 Reluctance Motor

In single-phase reluctance motor, the rotating field is produced by main and auxiliary winding (split phase) placed in stator slots. The rotor is made of stampings with a projecting structure as shown in Fig. 10.12. Short-circuited bars are placed in the projected stator portions. The motor starts like a single-phase induction motor. Near synchronous speed, the rotor gets locked with the rotating magnetic field in the position of minimum reluctance and thereafter runs at synchronous speed.

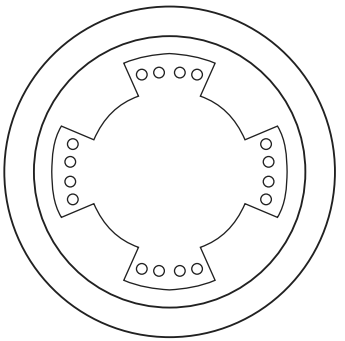


Fig. 10.12 *4-pole single-phase reluctance motor*

10.3.2 Hysteresis Motor

A split-phase stator and a solid iron rotor with high hysteresis loss is employed in a hysteresis motor. The motor starts by induction action and is pulled into synchronism near synchronous speed. Because of hysteresis, the rotor field lags the stator field by an angle δ with consequent torque production as shown in Fig. 10.13. Because of smooth rotor, it has a very low noise figure and is used in phonographic appliances.

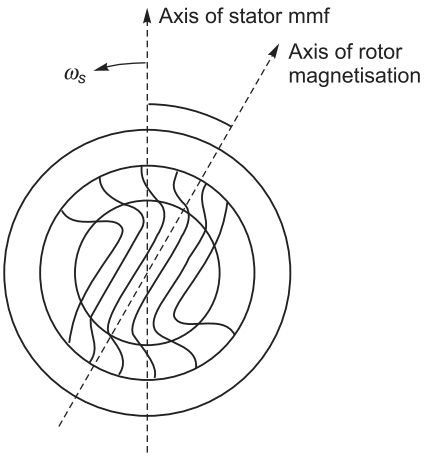


Fig. 10.13 *Torque production in hysteresis motor*

10.4 AC SERIES MOTOR—UNIVERSAL MOTOR

The torque in a dc series motor is given by the expression

$$T = K_T i_a^{\,2}$$

If this motor is ac excited, the torque would be unidirectional with an average component and a second harmonic oscillating component as shown in Fig. 10.14.

The average torque can be obtained from

$$T_{\text{av}} w = E_a I_a$$

where $\overline{E}_a$ and $\overline{I}_a$ must be in phase in a series excited dc armature.

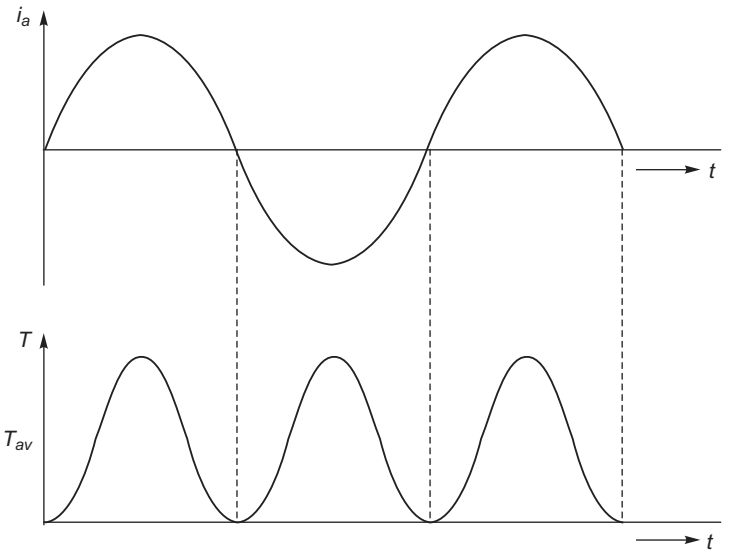


Fig. 10.14 *Torque in ac excited series motor*

There are certain consequences of ac excitation of the dc series motor.

- The field and yoke carry alternating flux and must, therefore, be laminated.
- Apart from speed emf E_a, the armature coils have transformer emf induced in them by the alternating field flux. This reactance emf seriously impairs the commutation qualities of the machine. Interpoles must therefore be provided.
- Because of alternating armature flux (armature reaction), the armature offers a high reactance causing the motor to have a very poor pf. The armature reaction must therefore be cancelled out by providing compensating winding placed in pole faces.

The schematic connection diagram of a series motor is shown in Fig. 10.15.

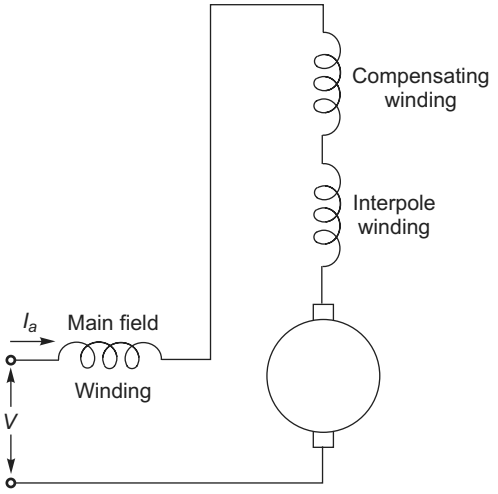


Fig.10.15 *Connection diagram of ac excited series motor*

The no-load speed of a universal motor may be as high as 20,000 rpm unlike that of other motors. Therefore, it has a smaller physical size for a given power capacity. It finds applications where light weight is important and high operating speeds are desired, as in vacuum cleaners and portable tools.

Summary

- ➢ Fractional kW power motors, are generally single-phase motors such as fans, refrigerators, vacuum cleaners, etc.
- ➢ Single-phase induction motor is not self-starting. It can be made as self-starting motor by using two windings (starting, main) which is used only at the time of starting.
- ➢ Both reluctance and hysteresis motor are synchronous speed motor (constant speed motors).

Exercises

Review Questions

1. Why is a single-phase induction motor not self-starting?
2. How can the starting torque in a single-phase induction motor be improved?
3. What is the working principle of a reluctance motor?
4. Why is the power factor of the universal motor low?
5. How does the universal motor run with both ac and dc? Discuss the features of a universal motor.
6. What is hystersis effect and how is it used in the hysteresis motor?
7. Discuss the advantages of a two-value capacitor motor briefly.

Multiple-Choice Questions

1. A single-phase stator winding when excited with ac voltage produces
   (a) a single rotating field rotating at synchronous speed
   (b) two rotating fields rotating at synchronous speed in opposite directions
   (c) two rotating fields rotating in the same direction but at different speeds
   (d) two rotating fields rotating in opposite directions but with different speeds
2. A single winding single-phase motor has
   (a) low starting torque
   (b) zero starting torque
   (c) high starting torque
   (d) starting torque equal to full-load torque
3. A single-phase self-starting motor has two stator windings
   (a) placed at 180° elect and fed with out-of-phase voltages
   (b) placed at 90° elect and fed with in-phase voltages
   (c) placed at 45° elect and fed with out-of-phase voltages
   (d) placed at 90° elect and fed with out-of-phase voltages
4. Phase splitting can be accomplished in a single-phase induction motor
   (a) only by adding a capacitor in series with the auxiliary winding
   (b) only by causing the auxiliary winding to have high resistance
   (c) only by causing the auxiliary winding to have very high resistance
   (d) by any of the above these methods
5. A capacitor start single-phase motor is used
   (a) for easy to start loads
   (b) for medium start loads
   (c) for hard to start loads
   (d) for any type of start loads

6. A shaded-pole motor runs in
   (a) the dissection from the shaded to unshaded part of the poles
   (b) the direction from the unshaded to shaded part of the poles
   (c) any direction depending on the polarity of the applied voltage
   (d) none of the above
7. Compared to a capacitor-start motor, a two-value capacitor motor has
   (a) nearly the same starting torque but better running power factor
   (b) higher starting and higher running power factor
   (c) higher starting torque but lower running power factor
   (d) lower starting torque but higher running power factor
8. A single-phase reluctance motor
   (a) has zero starting torque as it is a synchronous motor
   (b) starts as an induction motor but runs as a synchronous motor
   (c) starts as a hysteresis motor but runs as a synchronous motor
   (d) starts as an induction motor and runs as an induction motor
9. A single-phase hysteresis motor
   (a) can run at synchronous speed
   (b) can run at subsynchronous speed only
   (c) can run at synchronous and super synchronous speed
   (d) can run at synchronous and subsynchronous speed

Answers

Multiple-Choice Questions

1. (b) 2. (b) 3. (d) 4. (d) 5. (c)
6. (b) 7. (a) 8. (b) 9. (d)

Measuring Instruments

chapter 11

Goals & Objectives

- Introduction of electrical and electronic instruments
- Classification of instruments and types of indicating instruments
- Functioning mechanism of millimeter or VOM and oscilloscope
- Frequency and phase measurement
- Digital instruments—resolution and sensitivity
- Oscilloscope

11.1 INTRODUCTION

Measurement normally involves an instrument as a physical means of determining a variable or quantity. An instrument is defined as a device for finding out the value or magnitude of a variable or quantity. Measurement is a means to achieve the final goal, i.e. instrumentation. The electronic instrument depends on electrical or electronic principles for its measurement function.

The measurement of a given quantity is nothing but the result of a comparison between the quantity and a predefined standard (direct method). In engineering applications, indirect methods are normally preferred. It consists of a transducer, which converts the quantity to be measured in an analogous form. This analog signal is then processed by some intermediate means and is fed to the final device, which finally gives the measurement result.

11.2 ELECTRICAL AND ELECTRONIC INSTRUMENTS

The elements used in such instruments are

(i) a detector,
(ii) an intermediate transfer device, and
(iii) an indicator, a recorder or a storage device.

Mechanical instruments, due to their high inertia and noise, are hardly used nowadays. Their application is restricted to measurement of a slowly varying pressure.

Electrical instruments depend on the mechanical movement of an indicating device having some inertia and thus have a limited time response (0.5–24 s). Nowadays, electronic instruments are used for fast responses required for most scientific and industrial measurements. They are used for the detection of electromagnetically produced signals such as radio, video and microwaves, space applications and computers.

Some important terms pertaining to 'measurement' are defined now.

❑ **Instrument** A device for finding the value or magnitude of a quantity or variable.

❑ **Accuracy** It tells us about the nearness of the measured value towards the true value, i.e. the measure of conformity to the true value.

❑ **Precision** It refers to the degree of agreement within a group of measurements or instruments, i.e. the measure of reproductivity. Precision has two characteristics: conformity, and the number of significant figures to which measurements may be made.

❑ **Resolution** It is defined as the smallest change in input that can be detected by an instrument.

❑ **Sensitivity** It is the ratio of output signal or response of the instrument to a change of input or measured variable.

❑ **True Value (A_t)** It is the average of the infinite number of measurements, when the average deviation tends to become zero.

❑ **Error** An error is a deviation from the true value of the measured variable.

11.2.1 Errors

No measurement can be made with perfect accuracy. There are three types of errors: gross, systematic and random. *Gross errors* are mainly human errors like misreading of instruments, incorrect adjustment,

improper application of instruments and computational mistakes. *Systematic errors* have the same magnitude and sign for a given set of conditions. These errors accumulate at the end of the measurement. *Random errors* are caused due to random variations in the parameter or the system of measurement. These errors result in the deviation of magnitude of the variable measured by the instrument from the true value of the variable. The difference in the measured value and the true measured value gives rise to static errors.

Absolute static error $\delta A = A_m - A_t$ (11.1)

where, A_m is the measured value, and
A_t is the true value.

❑ **Relative Static Error** $\varepsilon_r = \delta A/A_t = (A_m - A_t)/A_t$ (11.2)

❑ **Static Error Correction** $\delta C = A_t - A_m = \delta A$ (11.3)

Limiting Error

In most indicating instruments, accuracy is guaranteed to a certain percentage of full-scale reading. The limits of these deviations from the specified value are known as limiting errors.

$$\delta A = A_a - A_s \tag{11.4}$$

where A_a is the actual measurement, and
A_s is the specified (nominal) value.

❑ **Guarantee Error (ε_r)**

$$\varepsilon_r = \delta A/A_S \tag{11.5}$$

11.2.2 Instrument Efficiency

1. Ammeter

$$\eta_A = I_{\text{fsd}}/\text{power consumed} = 1/V_{\text{fsd}} \tag{11.6}$$

2. Voltmeter

$$\eta_{\text{v}} = V_{\text{fsd}}/\text{power consumed} = 1/I_{\text{fsd}} \tag{11.7}$$

where I_{fsd} is the full scale current (A), and
V_{fsd} is the full-scale voltage (V).

Example 11.1

A 60 mV/120 mV dual-range millivoltmeter, when used to measure the voltage across two points in a dc circuit, gives a reading of 27.5–30 mV when 60 mV and 120 mV ranges, respectively, are employed. Assuming that the meter has been correctly calibrated, estimate the true value of the voltage existing across the two points in the dc circuit. It is known that the millivoltmeter has a sensitivity of 10 kΩ/volt.

Solution Let R_x be the resistance between the two points and I be the current through R_x.

For 60 mV range,

Resistance of millivoltmenter $(R_v) = 60 \text{ mV} \times 10 \text{ k}\Omega/\text{V} = 600 \ \Omega$

$\therefore \quad 27.5 \text{ mV} = I \times 600 \ R_x/(R_x + 600)$ (i)

For the 120 mV range,

Resistance of millivoltmeter $(R_v) = 120 \text{ mV} \times 10 \text{ k}\Omega/\text{V} = 1200 \ \Omega$

$\therefore \quad 30 \text{ mV} = I \times 1200 \ R_x/(R_x + 1200)$ (ii)

Dividing Eq. (i) by (ii), we get

$$27.5/30 = (1200 + R_x)/2\ (600 + R_x)$$

Solving $R_x = 120\ \Omega;\ I = 0.275$ mA

$\therefore$ actual voltage $= R_x I = 120 \times 0.275 = 33$ mV

11.3 CLASSIFICATION OF INSTRUMENTS

Instruments are broadly divided into two classes:

Absolute Instruments

These give the quantity to be measured in terms of an instrument constant and its deflection, e.g. tangent galvanometer.

Secondary Instruments

These directly give the magnitude of the electrical quantity to be measured, e.g. ammeter, voltmeter. The principle of working of all electrical measuring instruments depends on the various effects of electric current or voltage. The effects utilised in the manufacturing of electrical instruments are magnetic, heating, chemical and electromagnetic in nature. Indicating instruments consist essentially of a pointer moving over a calibrated scale attached to the moving system pivoted on jewelled bearings.

11.3.1 Basic Requirements for Measurement

For a satisfactory working of indicating instruments, the following three types of torques are required:

Deflection (Operating) Torque

It is necessary to make the moving system of the instrument (pointer) move from its zero position.

$$T_{dc} = N\,Bi\,ld = Gi \tag{11.8}$$

$\therefore$ $T_{dc} \propto$ measurand

where N = number of turns of coil
B = flux density in the air gap at the coil position
l = length of vertical side of coil
d = length of horizontal side of coil
i = current through the coil
$G = NBld$ displacement constant of the galvanometer

Controlling (Restoring) Torque

Some controlling force is employed either by a spring or gravity to limit the movement.

(a) A spring is generally used for controlling torque (phosphor bronze is the most suitable material).

$$T_c = k\theta \tag{11.9}$$

where θ is the deflection of the pointer and k is the controlling torque constant.

(b) Gravity method as shown in Fig. 11.1 is also sometimes used for controlling torque.

$$T_c \propto \sin\theta$$

Damping Torque

This torque is necessary to avoid oscillation of the moving system about its final deflected position owing to the inertia of the moving parts and to bring the moving system to rest in its deflected position quickly.

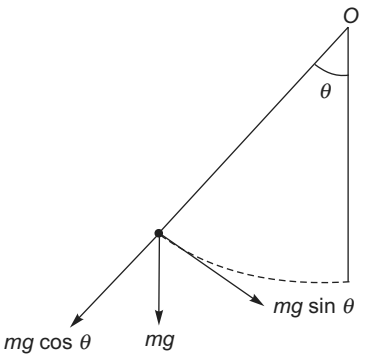


Fig. 11.1 *Controlling torque due to gravity*

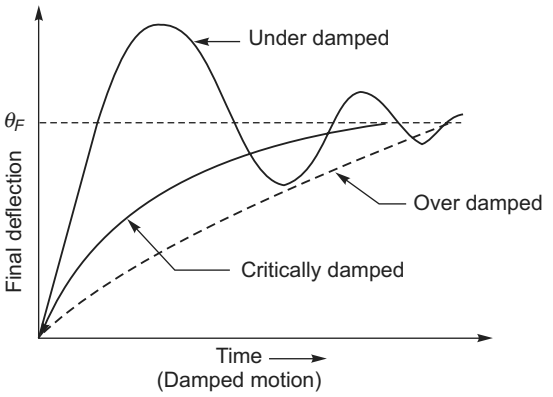


Fig. 11.2 *Different cases of damping of an instrument*

The various methods of obtaining damping are air friction, fluid friction and eddy current. Figure 11.2 shows the possible cases of damping of an instrument.

Damping torque $T_{dm} = D\, \mathrm{d}\theta/\mathrm{d}t$ (11.10)

where D is called the damping constant.

The restarting torque due to inertia of the moving system is

$$T_i = J(\mathrm{d}^2\theta/\mathrm{d}t^2) \tag{11.11}$$

where J is called the inertia constant.

Equation of Damping Motion

The general differential equation of damping motion is

$$J(\mathrm{d}^2\theta/\mathrm{d}t^2) + D(\mathrm{d}\theta/\mathrm{d}t) + k\theta = Gi \tag{11.12}$$

Hence, the auxiliary is

$$Jm^2 + Dm + k = 0$$

$$\therefore \quad m = [-D \pm j\sqrt{(4kJ - D^2)}]/2J$$

Thus, deflection $\theta = A\, e^{m1t} + B\, e^{m2t}$

Under steady state,

$$\frac{d^2\theta}{dt^2} = 0,\ \mathrm{d}\theta/\mathrm{d}t = 0,\ \theta = \theta_f$$

$$\therefore \quad \theta_f = Gi/k = \text{final steady state deflection}$$

Case I: If $D^2 < 4kJ$ then the response is underdamped

Case II: If $D^2 = 4kJ$ then the response is critically damped

Case III: If $D^2 > 4kJ$ then the response is overdamped

The angular frequency of damped oscillation is

$$\omega_d = \frac{\sqrt{4kJ - D^2}}{2J} \tag{11.13}$$

$$\therefore \qquad R = \frac{G^2}{2\sqrt{(kJ)}} \tag{11.14}$$

where, R is the series resistance for critical damping.

11.3.2 Electromagnetic Damping

Electromagnetic damping is produced by the induced effects when the coil moves in the magnetic field and a closed path is provided for the currents to flow. Electromagnetic damping is because of

1. eddy currents produced in the metal core, and
2. current circulated in the coil circuit by emf generated in the coil when it rotates.

11.4 TYPES OF INDICATING INSTRUMENTS

Indicating instruments can be divided into different types according to their working principles.

11.4.1 D' Arsonval Movement

The basic Permanent Magnet Moving Coil (PMMC) mechanism is often called the d'Arsonval Movement, named after its inventor. PMMC instruments are accurate and suitable for dc measurements only.

When the current I passes through a coil, a deflecting torque is produced on the coil.

$$T_{dc} = K_1 I$$

where K_1 = constant = NBA
N = number of turns in a coil
B = flux density
A = area of the coil

The deflecting torque causes a restoring torque in the spring attached to the pointer, which is given by

$$T_c = K_2\theta$$

where θ is the angular deflection of the pointer and k_2 is the controlling torque constant.

For final steady deflection,

$$T_{\text{dc}} = T_c$$

$$K_1 I = K_2\theta$$

$$\therefore \qquad \theta = (K_1/K_2)I \tag{11.15}$$

These instruments require very low power consumption and current for full-scale deflection.

11.4.2 Constructional Details

The permanent magnet (PM) has a semicircular spacing in which is fixed soft iron core to provide low reluctance flux path. The Moving Coil (MC) is placed in the annular space between PM and core. The coil of many turns is wound on a former as shown in Fig. 11.3(a). The coil is connected to a vertical spindle placed in low friction jewelled bearings. Two helical springs are connected to the spindle at one end and at the other end to a fixture. The springs thus counter the MC movement. The pointer P moves along a calibrated scale.

Note: Spindle, centre weight, helical springs points moving on a calibrated scale form part of all measuring instruments. The current to be measured is passed through the MC through flexible links.

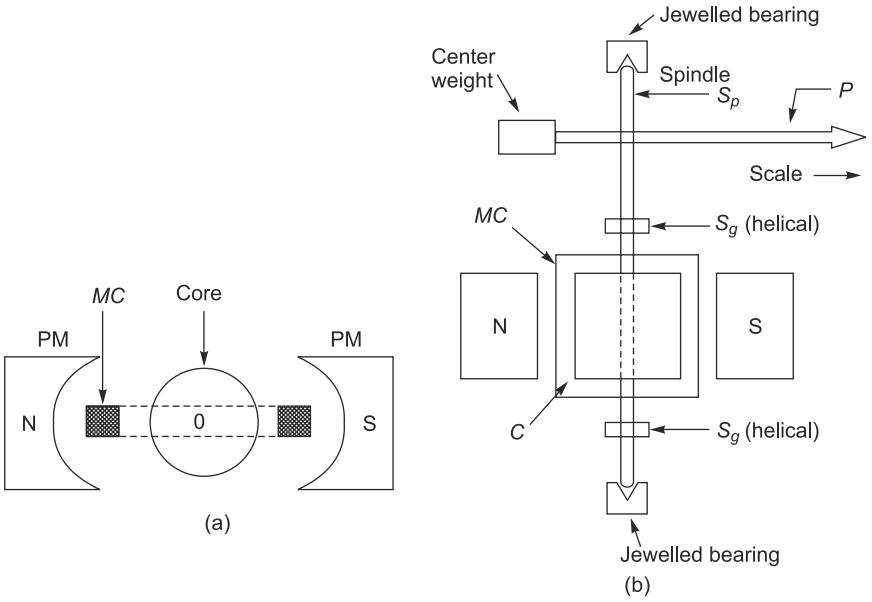


Fig. 11.3 *PMMC instrument*

Galvanometer Sensitivity

The sensitivity of a galvanometer can be specified in terms of current sensitivity and voltage sensitivity.

Current sensitivity $S_I = d/I$ mm/μA (11.16)

where d is the deflection of the galvanometer in scale divisions in mm and I is the galvanometer current in μA.

Voltage sensitivity $S_V = d/V$ mm/mV (11.17)

where V is the voltage applied to the galvanometer in mV.

dc Ammeter

The coil winding of the PMMC movement is small and light and it can carry only small currents. For large current measurement, major part of the current is bypassed through a shunt resistance, R_{sh} (Fig. 11.4).

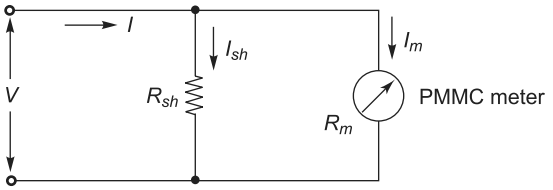


Fig. 11.4 *dc ammeter*

Clearly, $I_{sh} R_{sh} = I_m R_m$

$\therefore$ $R_{sh} = I_m R_m/(I - I_m)$

But $I_{sh} = I - I_m$

The current to be measured is passed through the MC through flexible links.

$$= R_m/(m - 1) \tag{11.18}$$

where $m = I/I_m$ = multiplying factor
R_m = internal resistance of the meter
I_{sh} = shunt current > I_m
I = full-scale current of the ammeter including the shunt

Multirange Ammeter

The current range of the dc ammeter may be further extended by a number of shunts, selected by a range switch. Such a meter is called a multirange ammeter. The meter shown in Fig. 11.5 is called a universal shunt.

dc Voltmeter

The basic d'Arsonval movement can be converted into a dc voltmeter with the addition of a series resistor or multiplier, as shown in Fig. 11.6. The multiplier limits the current through the movement so as not to exceed the value of the full-scale deflection current (I_{fsd}).

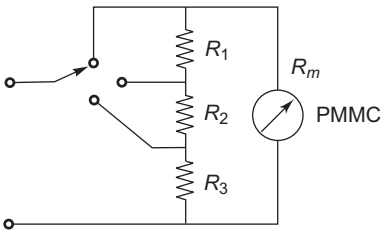


Fig.11.5 *Multirange ammeter*

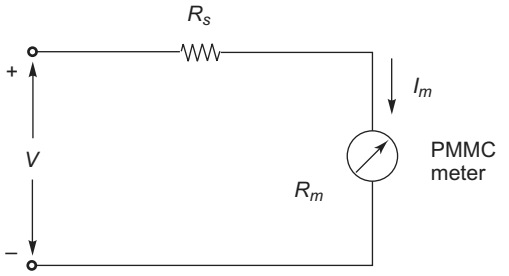


Fig. 11.6 *dc voltmeter*

A dc voltmeter is connected across a source of emf or a circuit component. The terminals are generally marked positive and negative since polarity must be observed.

The value of a multiplier required to extend the voltage is calculated as follows:

$$V = I_m (R_s + R_m) \quad \text{or} \quad R_s = V/I_m - R_m \tag{11.19}$$

Multiplying factor $m = V/V_m = I_m (R_m + R_s)/I_m R_m$

$$m = 1 + R_s/R_m$$

$$\therefore \quad R_s = (m - 1)R_m \tag{11.20}$$

where I_m = deflection current of the meter
R_s = multiplier resistance
V = full-scale voltage of the instrument
V_m = Voltage across movement

Multirange Voltmeter

A multirange voltmeter can be obtained by the addition of a number of multipliers together with a range switch. There are two types of multirange voltmeters.

1. The meter shown in Fig. 11.7(a) has only one resistance connected to the PMMC meter.
2. The meter shown in Fig. 11.7(b) has all multipliers connected in series with the PMMC meter.

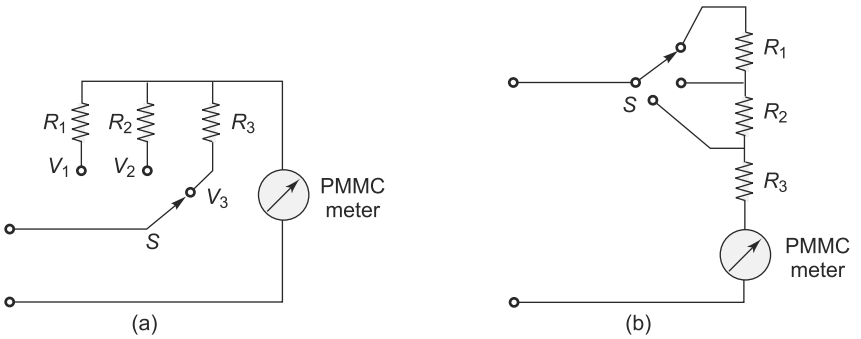


Fig. 11.7 *Multirange voltmeters*

Voltmeter sensitivity (ohm/V rating)

$$S = 1/I_{\text{fsd}}\ \Omega/\text{V} \tag{11.21}$$

The total resistance of the voltmeter will be

$$R_{\text{total}} = S \times V,\ R_s = (S \times V) - R_m \tag{11.22}$$

❑ **Loading Effect** A low sensitivity meter may give a correct reading when measuring voltages in low resistance circuits. A voltmeter when connected across two points in a highly resistive circuit, acts as a shunt for that portion of the circuit and thus reduces the equivalent resistance in that portion of the circuit. The meter will give a lower indication of the voltage drop that actually existed before the meter was connected. This effect is called the *loading effect* of an instrument.

Example 11.2

A moving-coil instrument gives full-scale deflection with 25 mA. The resistance of the coil is 5 Ω. It is required to convert this meter into an ammeter to read up to 5 A. Find (a) the resistance of the shunt to be connected in parallel with the meter, and (b) the value of series resistance for the above meter to read up to a voltage of 20 V.

Solution

(a) Full scale $I_{\text{fsd}} = 25$ mA

$\therefore$ current through shunt resistance $(R_x) = 4.975$ A

$$25\ \text{mA} \times 5\ \Omega = R_x \times 4.975\ \text{A}$$

$$\therefore \quad R_x = 0.025\ \Omega$$

(b) For the meter to read 20 V,

$$20\ \text{V} = (R_x + 5) \times 25\ \text{mA}.$$

$$\therefore \quad R_x = 795\ \Omega$$

Example 11.3

If the instrument of Example 11.2 is to be converted into a multirange voltmeter to read up to 40 V and 60 V, find the additional resistance to be connected in series with the instrument.

Solution Let R_1 be the resistance in series (Fig. 11.8)

$$40 = (R_1 + 5) \times 0.025$$

$$\therefore \quad R_1 = 1595\ \Omega$$

Let R_2 be the other resistance in series.

Then, $$60 = (R_1 + R_2 + 5) \times 0.025$$

$$R_2 = 800\ \Omega$$

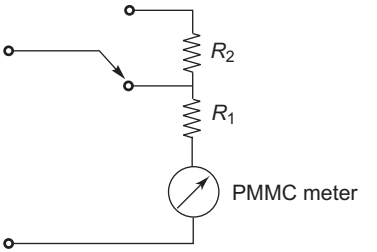


Fig. 11.8

11.4.3 Ohmmeter

This instrument is used to measure resistance. It is mainly of two types.

Series-Type Ohmmeter

It essentially consists of a d'Arsonval movement connected in series with a resistance and a battery to a pair of terminals to which the unknown resistance is connected, as shown in Fig. 11.9. The current through the movement thus depends on the magnitude of the unknown resistor R_x and the meter indication is proportional to the value of R_x.

When R_x is zero, maximum current flows in the circuit and shunt resistance R_2 is adjusted until the movement indicates full-scale current. The full-scale current position of the pointer is marked 0 Ω on the scale. When R_x is infinity, the current drops to zero and movement indicates zero current, which is marked as '∞' on the scale.

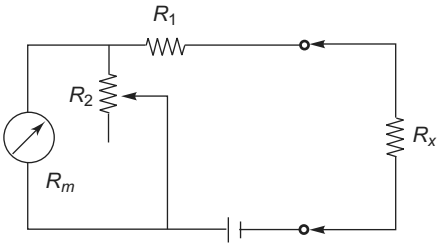


Fig. 11.9 *Series type ohmmeter*

A convenient quantity to use in the design of a series type ohmmeter is the value of R_x (= R_h) which causes half-scale deflection of the meter.

$$R_h = R_1 + (R_2 \parallel R_m)$$

Then, total resistance for the battery is 2 R_h.

$$\therefore \quad I_t = 2\, I_h = E/R_h,\ I_2 = I_t - I_{\text{fsd}}$$

where I_t = current through R_x for producing full-scale meter deflection
I_h = current for producing half-scale meter deflection
I_{fsd} = current through movement causing full-scale deflection
I_2 = current through R_2

Also, voltage across shunt (R_2) is equal to voltage across movement, (R_m), i.e. $E_{\text{sh}} = E_m$

or $$I_2 R_2 = I_{\text{fsd}}\, R_m \tag{11.23}$$

$$\therefore \quad R_2 = I_{\text{fsd}}\, R_m\, R_h/(E - I_{\text{fsd}}\, R_h)$$

$$R_1 = R_h - I_{\text{fsd}}\, R_m\, R_h/E \tag{11.24}$$

Shunt-Type Ohmmeter (Fig. 11.10)

When R_x is zero, the meter current is zero. If R_x is infinity, a current finds a path only through the meter and by appropriate selection of the value of R_x, the pointer can be made to read full scale. This ohmmeter has a zero mark at the right-hand side of the scale. It is particularly used for low resistance.

When R_x is infinite, the full-scale meter current will be

$$I_{fsd} = EV/(R_1 + R_m)$$

For any value of R_x,

$$I_m = ER_x/[R_1 R_m + R_x (R_1 + R_m)]$$

Then

$$S = I_m/I_{fsd}$$

$$\therefore \quad S = R_x/[R_x + R_1R_m/(R_1 + R_m)]$$

$$= R_x/(R_x + R_p) \qquad (11.25)$$

where

$$R_p = R_1 \| R_m$$

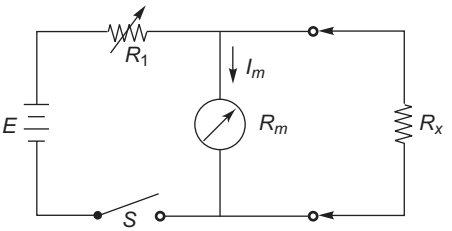


Fig. 11.10 *Shunt-type ohmmeter*

11.4.4 ac Indicating Instruments

PMMC meters cannot be used for measuring ac signals because the meter will show the average value of ac, i.e. zero deflection.

Electrodynamometer

It can be used for ac as well as dc measurements. It contains two types of coils, a fixed coil and a moving coil. The field is produced by a fixed coil. This coil is divided into two sections to give a more uniform field.

Deflecting torque $T_d = BANI$ (11.26)

where B = flux density of the magnetic field in which the coil moves
A = area of cross section of coil
I = current through the coil
N = number of turns of coil

But $B \propto I$

$\therefore \quad T_d \propto I^2$

Instantaneous deflecting torque $T_i = i_1 i_2 \dfrac{dM}{d\theta}$ (11.27)

where i_1 = instantaneous current in the fixed coil
i_2 = instantaneous current in the moving coil
M = mutual inductance of coils
θ = deflection of pointer

❑ Operation with dc

$$T_d = I_1 I_2 \frac{dM}{d\theta} \qquad (11.28)$$

where I_1 and I_2 are dc currents through fixed and moving coils, respectively.

This deflecting torque deflects the moving coil to such a position where the controlling torque ($k\theta$) of the spring is equal to the deflecting torque.

$$\therefore \quad k\theta = I_1 I_2 \frac{dM}{d\theta}$$

$$\therefore \quad \theta = (I_1 I_2/k) \frac{dM}{d\theta} \qquad (11.29)$$

❑ **ac Currents** The meter will show the average value of the deflecting torque.

$$\therefore \quad T_{av} = \frac{dM}{d\theta}\frac{1}{T}\int i_1 i_2\, dt \tag{11.30}$$

❑ **Sinusoidal Currents**

Let $i_1 = I_{m1} \sin \omega t$

and $i_2 = I_{m2} \sin (\omega t - \phi)$

The average torque $(T_{av}) = (dM/d\theta)\ (1/T)$

$$\int I_{m1} I_{m2} \sin \omega t \sin (\omega t - \phi) dt = (I_{m1} I_{m2}/2) \cos \phi\, dM/d\theta$$

$$\therefore \quad T_{av} = I_1 I_2 \cos \phi \frac{dM}{d\theta} \tag{11.31}$$

where I_1 and I_2 are the rms values of i_1 and i_2, respectively. At steady state,

$$k\theta = I_1 I_2 \cos \phi \frac{dM}{d\theta}$$

$$\therefore \quad \theta = \frac{I_1 I_2}{k} \cos \phi \frac{dM}{d\theta} \tag{11.32}$$

Electrodynamometer in Current and Voltage Measurement

In an electrodynamometer, current under measurement itself produces a magnetic field flux in which the movable coil rotates.

A Fixed Coil (FC) splits into equal halves and provides the magnetic field in which the movable coil (MC) rotates. The two coil halves are connected in series and are fed by the current under measurement as shown in Fig. 11.11.

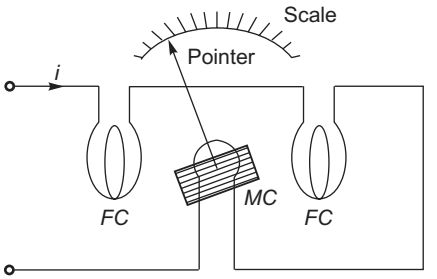


Fig. 11.11 *Electrodynamometer type ammeter*

Meter deflection $\propto \sqrt{(\text{average } i^2)}$

The meter, therefore, reads the rms or effective value of ac.

In ammeters, fixed and movable coils are connected in series and, therefore, carry the same current. Hence,

$$I_1 = I_2 = I,\ \phi = 0$$

$$\therefore \quad \theta = (I^2/k)\frac{dM}{d\theta} \tag{11.33}$$

In the voltmeter, the fixed and movable coils are connected in series with a high non-inductive resistance.

Hence,

$$I_1 = I_2 = V/Z,\ \phi = 0$$

$$\therefore \quad \theta = (V^2/Z^2 k)\ dM/d\theta \tag{11.34}$$

The appropriate selection of the shunt value converts the electrodynamometer into the desired range of the ammeter and the addition of the series resistance converts the meter into a voltmeter exactly like the dc ammeter and voltmeter discussed earlier.

These types of ammeters and voltmeters can measure either ac or dc quantities.

Electrodynamometers in Power Measurement

The electrodynamometer movement is used extensively in measuring power. It may be used to indicate both dc and ac power for any waveform of voltage and current and is not restricted to a sinusoidal waveform.

The fixed or field (current) coil, shown in Fig. 11.12 as two separate elements, is connected in series and carry the total line current (i_c). The movable (potential) coil located in the magnetic field of fixed coils is connected in series with a current-limiting resistor (R_p) across the power line and carries the small current (i_p). The instantaneous value of current in the movable coil is

$$i_p = e/R_p$$

where e is the instantaneous voltage across the power line, and R_p is the total resistance of the movable coil and its series resistor.

The deflection of movable coil is proportional to the product of the two currents i_c and i_p.

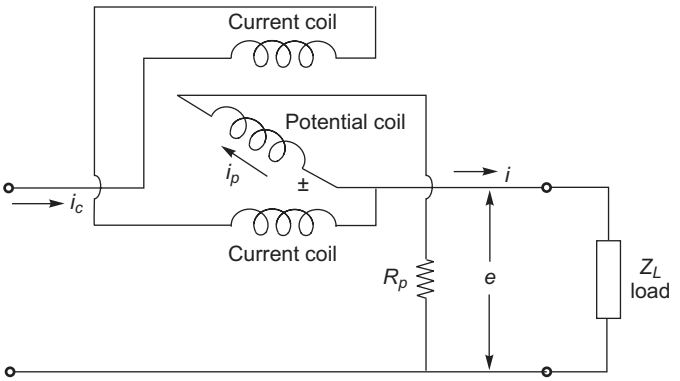


Fig. 11.12 *An electrodynamometer in power measurement*

Average deflection over one period

$$\theta_{av} = (k/T) \int i_c\, i_p\, dt$$

Average power in circuit

$$\therefore \qquad P_{av} = 1/T \int ei\, dt \tag{11.35}$$

$$\therefore \qquad P_{av} = \theta_{av}$$

which indicates that the electrodynamometer movement of Fig. 11.12 has a deflection proportional to the average power.

Electrodynamometer Wattmeters

An electrodynamometer wattmeter, shown in Fig. 11.13, has a current coil and a pressure coil.

The instantaneous torque is

$$T_i = i_1 i_2 \frac{dM}{d\theta}$$

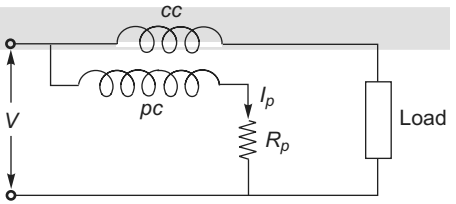


Fig. 11.13 *Electrodynamometer wattmeter*

where i_1 and i_2 are the instantaneous currents in the two coils and M is the mutual inductance of coils.

Therefore, the average deflecting torque is

$$T_i = (V I_c / R_p)\cos\phi \frac{\mathrm{d}M}{\mathrm{d}\theta}$$

where ϕ is the lagging phase angle of current in the current coil, I_c is the current coil current and R_p is the series resistance of pressure coil circuit.

$$\theta = (V I_c / kR_p)\cos\phi \frac{\mathrm{d}M}{\mathrm{d}\theta} \tag{11.36}$$

If the pressure coil has some inductance then

$$W = (V I_c / kR_p)\cos(\phi - \alpha)\cos\alpha \frac{\mathrm{d}M}{\mathrm{d}\theta} \tag{11.37}$$

where α is the lagging phase angle between current in pressure coil and voltage supply. But the true value of power is

$$W_{\text{true}} = (V I_c / kR_p)\cos\phi \frac{\mathrm{d}M}{\mathrm{d}\theta}$$

$$\therefore \quad W/W_{\text{true}} = \cos\alpha\,[\cos\alpha + (\sin\alpha)\,(\tan\phi)] \tag{11.38}$$

11.4.5 Three-Phase Power Measurement

There are several ways in which three-phase power can be measured. Most important and common of these is the one called the *two-wattmeter method*, especially used when the load is unbalanced. Two wattmeters are used in a three-wire system (Fig. 11.14) with delta or star-connected load. The total instantaneous power consumed by the load is $v_1 i_1 + v_2 i_2 + v_3 i_3$

Instantaneous reading of $W_1 = i_1 (v_1 - v_3)$

Instantaneous reading of $W_2 = i_2 (v_2 - v_3)$

$\therefore$ Total instantaneous power in the load = $v_1 i_1 + v_1 i_2 - v_3 (i_1 + i_2)$

From Kirchhoff's law, $i_3 = -(i_1 + i_2)$

$\therefore$ Total instantaneous power = $v_1 i_1 + v_2 i_2 + v_3 i_3$

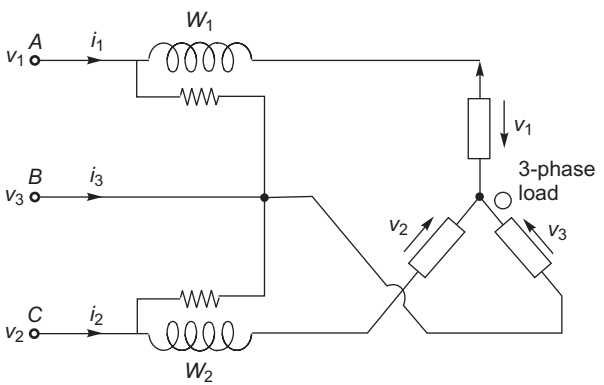


Fig. 11.14 *Two-wattmeter method*

Thus, the sum of the two wattmeter readings is equal to the power consumed by the load (balanced or unbalanced). Figure 11.15 shows the phasor diagram for a balanced star-connected load of Fig. 11.14.

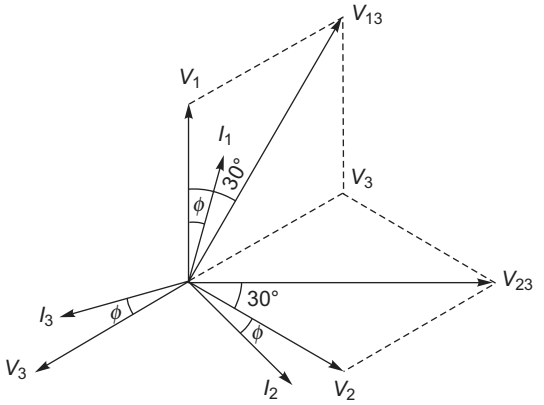


Fig. 11.15 *Phase diagram for balanced star-connected load of Fig. 11.14*

Consider a balanced load for the sake of simplicity.

Let $I_1 = I_2 = I_3 = I$; $V_1 = V_2 = V_3 = V$ (say) rms values

Line voltages $V_{13} = V_{23} = V_{12} = \sqrt{3}$ V

The phase currents lag the corresponding phasor voltages by an angle ϕ. The current I_1 flows through W_1 and voltage across its pressure coil is V_{13}. I_1 leads V_{13} by an angle $(30° - \phi)$.

$$\therefore \quad \text{reading of } W_1 = V_{13}\, I_1 \cos (30° - \phi) = \sqrt{3}\, VI \cos (30 - \phi) \tag{11.39}$$

The current through the wattmeter W_2 is I_2 and voltage across its pressure coil is V_{23}. I_2 lags V_{23} by an angle $(30° + \phi)$.

$$\therefore \text{ reading of wattmeter } \quad W_2 = V_{23} I_2 \cos (30° + \phi)$$

$$= \sqrt{3}\, VI \cos (30° + \phi) \tag{11.40}$$

$$\therefore \text{ sum of the wattmeter readings} = W_1 + W_2$$

$$= \sqrt{3}\, VI \ \ [\cos (30° - \phi) + \cos (30° + \phi)] = 3\, VI \cos \phi \tag{11.41}$$

$$= \text{three-phase power in the load}$$

Difference of readings of two wattmeters is

$$W_1 - W_2 = \sqrt{3}\, VI\, [\cos (30° - \phi) - \cos (30° + \phi)]$$

$$= \sqrt{3}\, VI \sin \phi \tag{11.42}$$

$$\frac{W_1 - W_2}{W_1 + W_2} = \frac{\sqrt{3}\, VI \sin\phi}{3VI \cos\phi} = \frac{1}{\sqrt{3}} \tan\phi$$

or

$$\phi = \tan^{-1} \sqrt{3}\, \frac{W_1 - W_2}{W_2 + W_2} \tag{11.43}$$

From Eq. (11.43), power factor (cos ϕ) may be found.

Some points worth noting are as follows:

(i) At unity power factor, the readings of the two wattmeters are equal.
(ii) When the power factor is 0.5, one of the wattmeters reads zero and the other reads total power.
(iii) With zero power factor, the readings of the two wattmeters are equal, but of opposite sign.
(iv) It should be noted that when the power factor is below 0.5, one of the wattmeters will give negative reading. Thus, to read the wattmeter, we must either reverse the current coil or the pressure coil connections. The wattmeter will then give a positive reading but this must be taken as negative for calculating the total power.

Example 11.4

Two wattmeters are connected to measure power in a three-phase circuit. One of the wattmeters reads 500 W and the other points out in reverse direction. After reversing the voltage coil terminals, the reading of this wattmeter is found to be 200 W. Determine the power factor of the load and the total three-phase power of the circuit.

Solution

$$W_1 = 500 \text{ W} \qquad W_2 = -200 \text{ W}$$

$\therefore$ total power $= W_1 + W_2 = 300$ W

$$\tan \phi = \frac{500 - (-200)}{500 + (-200)} = \frac{700}{300} = \frac{7}{3}$$

$\therefore$ $\phi = 66.8°$

$$\text{pf} = \cos \phi = 0.39$$

11.4.6 Induction-Type Instruments

Induction-type instruments depend upon magnetic induction for operation and are used for ac measurement only.

$$\text{Deflecting torque } (T_d) \propto \phi_1, \phi_2 \tag{11.44}$$

$\therefore$ fluxes ϕ_1 and ϕ_2 both are proportional to some current I.

$\therefore$ $T_d \propto I^2$

The induction-type ammeter and voltmeter employ coil spring control and electromagnetic damping. The induction-type instrument is primarily used as a watt-hour meter or energy meter.

Watt-hour Meter or Energy Meter

It is used for commercial measurement of electrical energy. Figure 11.16 shows the elements of a single-phase watt-hour meter.

The current coil is connected in series with the line, and the voltage coil is connected across the line. Both coils are wound on a metal of special design providing two magnetic circuits. A light aluminium disc is suspended in the air gap of the current coil field which causes eddy currents to flow in the disk. The reaction of the eddy currents and the field of voltage coil creates a torque on the disk, causing it to rotate. The number of rotations of the disk is proportional to the energy consumed by the load in a certain time interval.

At very light loads, the voltage component of the field produces zero torque that is not directly proportional to the load. Compensation for error is provided by inserting a shading coil with the meter operating at 10% of rated load. Two holes are drilled in the disk of the energy meter on the opposite side of the spindle to eliminate creeping on no load.

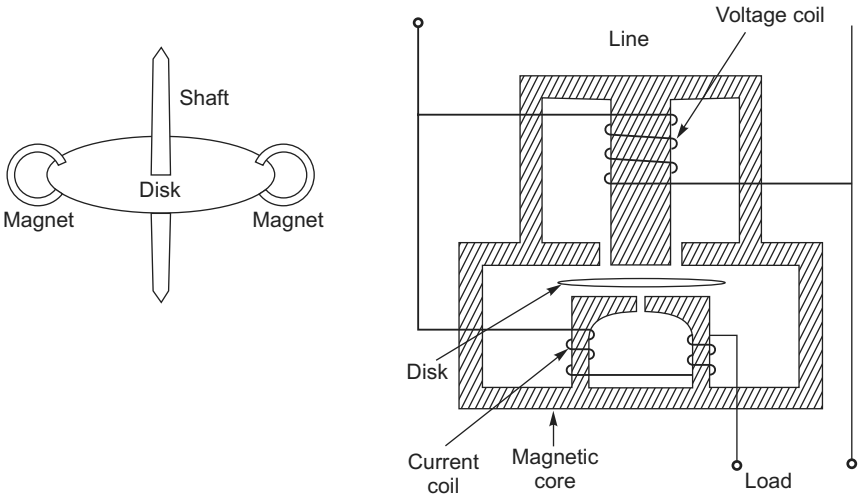


Fig. 11.16 *Watt-hour meter or energy meter*

Electronic energy meters are now available and are gradually finding acceptability.

Moving Iron Instrument

In this type of instrument, a plate of soft iron is the moving element of the system. This iron moves in a magnetic field produced by a stationary coil. The coil is excited by a current or voltage under measurement.

There are two types of moving iron instruments:

❑ **Attraction Type** In this type, a sheet of soft iron is attracted towards a solenoid.

❑ **Repulsive Type** In this type, two parallel strips of soft iron magnetised inside a solenoid repel each other.

The deflection of the pointer,

$$\theta = (I^2/2k)\, \mathrm{d}L/\mathrm{d}\theta \tag{11.45}$$

where k is the control spring constant, L is the instrument inductance and I is the initial current.

$$\therefore \quad \theta \propto I^2_{\text{rms}} \text{ for ac}$$

$$\propto I^2 \text{ for dc}$$

11.4.7 Attracted-iron Type

The schematic diagram is drawn is Fig. 11.17. As the current to be measured passes through the solenoid, magnetic flux created within it. The flux, causes the oblong soft iron disc to be attracted inwards and so the pointer moves through a certain angle. As the solenoid current increases, soft-iron disc is attracted more inwards increasing the pointer angle.

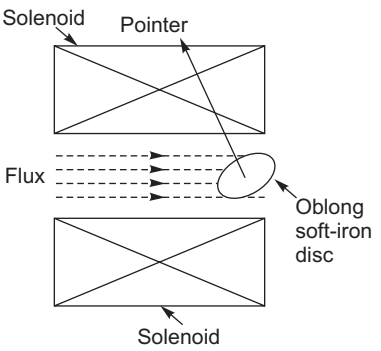


Fig. 11.17 *Attracted-iron instrument*

11.4.8 Repulsion-iron Type

Here are two soft iron long pieces inside the solenoid—one fixed and other mobile are shown in Fig. 11.18.

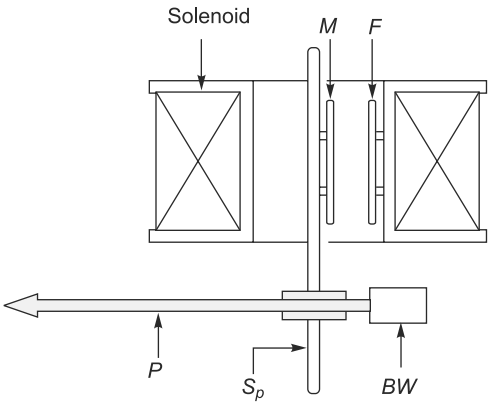


Fig. 11.18

As the current to be measured is passed through the solenoid, the two soft-iron pieces get magnetised in the same direction and so repel each other. This causes the mobile piece to turn, and the spindle and pointer turns along with it, and the current value is read on as a calibrated scale.

Megger

Megger is an insulation testing instrument. It is used to measure very high resistances of the order of megaohms. This instrument works on the principle of an ohmmeter. The required deflecting torque is produced by both the system voltage and the current. Because of interaction between the magnetic fields produced by the voltage and the current, the deflecting torque is produced.

11.5 MULTIMETER OR VOM

The ammeter, the voltmeter, and the ohmmeter are all used as d'Arsonval movement. The difference between these instruments is in the circuit in which the basic movement is used. It is therefore obvious that a single instrument can be designed to perform the three measurement functions. This instrument, which contains a *function switch* to connect the appropriate circuits to the d'Arsonval movement, is often called a *multimeter* or *volt-ohm-milliammeter* (VOM).

A representative example of a commercial multimeter is shown in Fig. 11.19. The circuit diagram of this meter is given in Fig. 11.20. The meter is a combination of a dc milliammeter, a dc voltmeter, an ac voltmeter, a multirange ohmmeter, and an output meter.

Figure 11.21 shows the circuit for the dc voltmeter section, where the common input terminals are used for voltage ranges of 0–1.5 to 0–1,000 V. An external voltage jack, marked "dc 5,000 V," is used for dc voltage measurements to 5,000 V.

Fig. 11.19 *General-purpose multimeter. This instrument has been a familiar sight in electronics laboratories for many years (Courtesy, Simpson Electric Company)*

The basic movement of the multimeter of Fig. 11.19 has a full-scale current of 50 μA and an internal resistance of 2,000 Ω. The values of the multipliers are given in Fig. 11.21. Notice that on the 5,000 V range, the range switch should be set to the 1,000–V position, but the test lead should be connected to the external jack marked "dc 5,000 V". The normal precautions for measuring voltages should be taken because of its fairly sensitivity (20 kΩ/V). The instruments are suitable for general service work in electronics field.

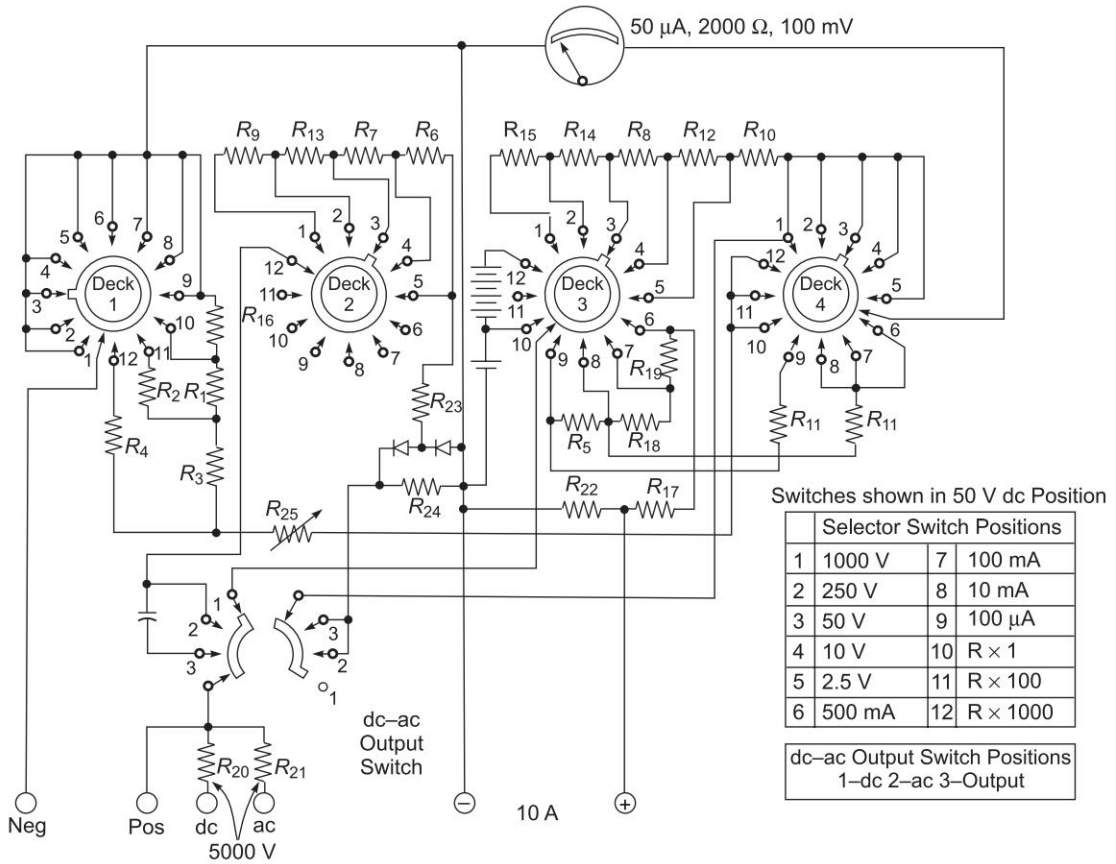


Fig. 11.20 *Schematic diagram of the Simpson Model 260 multimeter (Courtesy, Simpson Electric Company)*

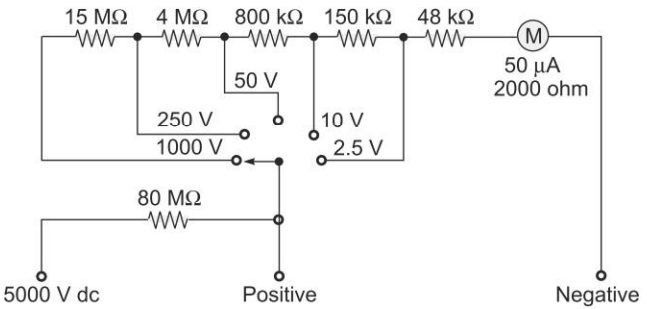


Fig. 11.21 *dc voltmeter section of the Simpson Model 260 multimeter (Courtesy, Simpson Electric Company)*

11.6 OSCILLOSCOPE

The Cathode Ray Oscilloscope (CRO) is probably the most versatile tool for the development of electronic circuits and systems. The CRO allows the amplitude of electrical signals (e.g. V, I or P) to be displayed as a function of time. The CRO depends on the movement of an electron beam, which is bombarded (impinged) on a screen coated with a fluorescent material, to produce a visible spot. If the electron beam is deflected on both the conventional axes (X and Y axes), a two-dimensional display is produced. Typically, the X-axis of the oscilloscope is deflected at a constant rate, relative to time, and the vertical or Y-axis is deflected in response to an input stimulus such as voltage. This produces the time-dependent variation of the input voltage, which is very important to the design and development of electronic circuits.

The oscilloscope is basically an electron-beam voltmeter. The electron beam follows rapid variations in signal voltage and traces a visible path on the CRT (Cathode Ray Tube) screen which is the heart of the oscilloscope. Thus, rapid variations, pulsations or transients are reproduced and the analyst can observe the waveform as well as measure amplitude at any instant of time.

The oscilloscope can reproduce HF waves which are too fast for electromechanical devices to follow. Thus, it is a kind of recorder, which uses an electron beam instead of a pen. The oscilloscope is capable of displaying events that take place over periods of microseconds and nanoseconds.

A storage CRT can retain the display much longer, up to several hours after the image was first written on the phosphor. The retention feature will be useful while displaying the waveform of a very low frequency signal. A better method of trace storage is the digital storage oscilloscope. In this technique, the waveform to be stored is digitised, stored in a digital memory and retrieved for display on the storage oscilloscope. One very important feature of a digital storage oscilloscope is its ability to provide 'pretrigger view'. This means that the oscilloscope can display what happened before a trigger input is applied. This is useful when a failure takes place. To find the reason of the failure, it would be necessary to see different waveforms before the failure.

By combining a special fibre optic CRT with an oscillograph type paper drive (which panes the paper over the CRT face where it is exposed by light from the CRT phosphor), a recording oscilloscope with useful characteristics is obtained.

Oscilloscope Block Diagram

The heart of the oscilloscope is the cathode ray tube, which generates the electron beam, accelerates the beam to a high velocity, deflects the beam to create the image, and contains the phosphor screen where the electron beam eventually becomes visible. To accomplish these tasks, various electrical signals and voltages are required, and these requirements dictate the remainder of the blocks of the oscilloscope outline as shown in Fig. 11.22. The power-supply block provides the voltages required by the cathode ray tube to generate and accelerate the electron beam, as well as to supply the required operating voltages for the other circuits of the oscilloscope. Relatively high voltages are required by cathode ray tubes, of the order of a few thousand volts, for acceleration, as well as a low voltage for the heater of the electron gun, which emits the electrons. Supply voltages for the other circuits are various values, usually not more than a few hundred volts.

The laboratory oscilloscope has a time base which generates the correct voltage to supply the cathode ray tube to deflect the spot at a constant time-dependent rate. The signal to be viewed is fed to a vertical amplifier, which increases the potential of the input signal to a level that will provide a usable deflection of the electron beam. To synchronise the horizontal deflection with the vertical input, such that the horizontal deflection starts at the same point of the input vertical signal each time it sweeps, a synchronising or triggering circuit is used. This circuit is a link between the vertical input and the horizontal time base.

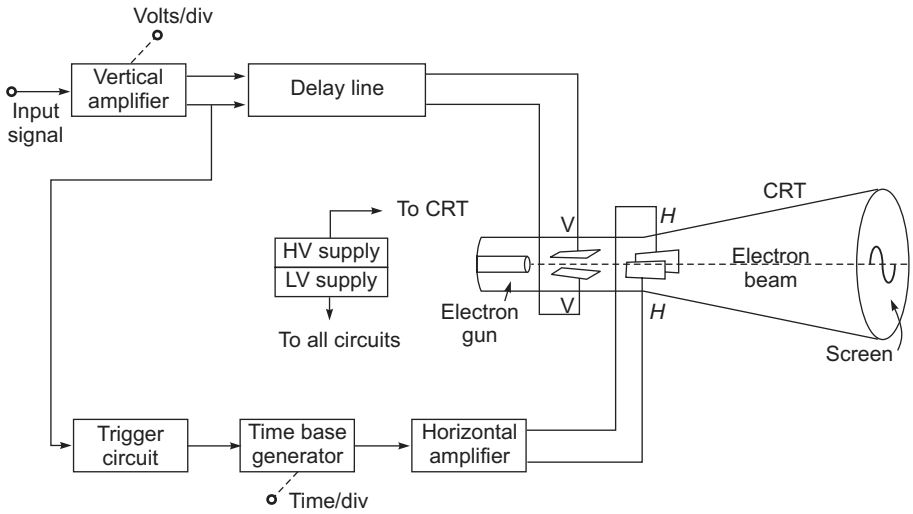


Fig. 11.22 *Block diagram of a general-purpose oscilloscope*

11.7 FREQUENCY MEASUREMENT

CRO Method

From the calibrated time base, display the wave and see the time interval for a cycle and calculate the frequency.

Frequency $f = (1/T)$ Hz (11.46)

where T is the time period in seconds.

Dual-Trace Method (Fig. 11.23)

Display a known frequency wave on one channel to an unknown wave on the second channel. Count the number of cycles of both the waves.

$$f_{\text{unknown}} = (n/N) f_{\text{known}} \tag{11.47}$$

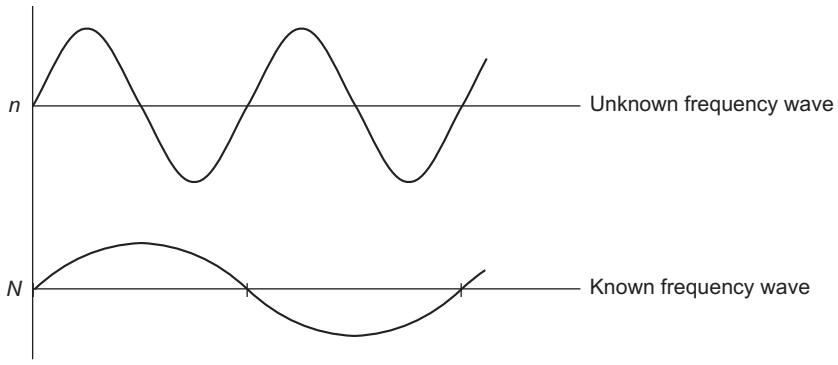


Fig. 11.23 *Dual trace method*

Lissajous Pattern Method

An unknown frequency wave is applied to the *X*-plates and a known frequency wave is applied to the *Y*-plates of the CRO of Fig. 11.24. Adjust the known frequency wave until an elliptical loop appears on the screen as shown in Fig. 11.24. At this point, the two frequencies will be equal.

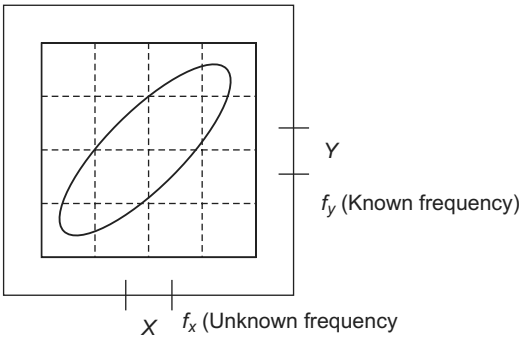


Fig. 11.24 *Lissajous-pattern method*

If f_x and f_y are equal then the Lissajous pattern could take one of the three shapes depending on the phase difference between the two signals as shown in Fig. 11.25.

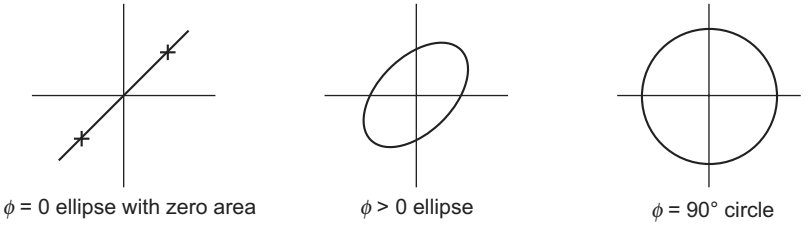


Fig. 11.25 *Lissajous patterns*

Z Modulation Method

This method is specially useful for high frequency measurement. It could be used up to a known to unknown frequency ratio of 1:50.

11.8 PHASE MEASUREMENT

CRO Method

The two signals for which the phase difference is to be measured are applied to the *X*-plates and *Y*-plates to obtain a Lissajous pattern, are shown in Fig. 11.26. Then

$$\sin \phi = B/A = D/C$$

$$\therefore \quad \text{Phase difference } \phi = \sin^{-1}(B/A) = \sin^{-1}(D/C)$$

❑ **Direct Reading Analogue Phase Meter** (Fig. 11.27)

$$V_{av} = E_0\, t/T = E_0\, \phi°/360°$$

Since E_0 and 360° are constant, $V_{av} \propto \phi°$

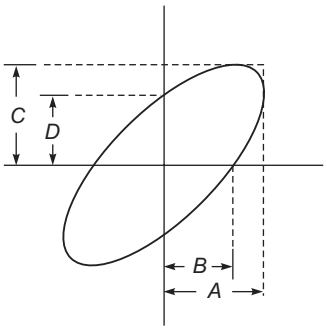


Fig. 11.26 *CRO method*

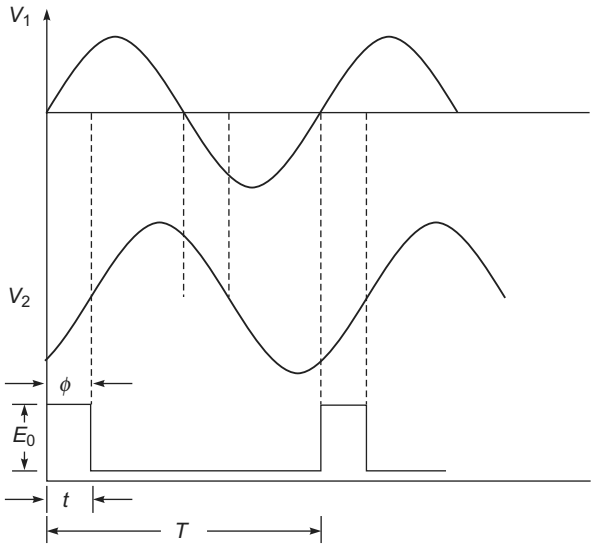


Fig. 11.27 *Direct reading analogue phase meter*

A multivibrator is being set at the edge of signal V_1 and gets reset at the edge of signal V_2, as shown in Fig. 11.28. Reading of the PMMC meter is calibrated in terms of the phase difference angle.

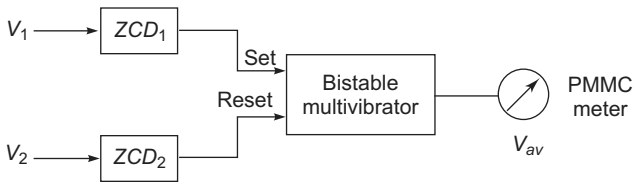


Fig. 11.28 *Block diagram*

11.9 DIGITAL INSTRUMENTS

Analog instruments display the quantity to be measured in terms of the deflection of a pointer. Digital instruments indicate the value of the measured in the form of a decimal number. The digital meters work on the principle of quantisation.

The advantages of digital instruments are as follows:

1. The readings are indicated directly in decimal numbers and, therefore, errors on account of human factors, such as errors due to parallax and approximation, are eliminated.
2. The readings may be carried to any significant figure by merely positioning the decimal point, i.e there is higher accuracy.
3. As compared to analog meters, digital instruments have a very high resolution.
4. Since output is in digital form, it may be directly fed into memory devices like tape recorders, printers and digital computers, etc. for storage and future computations.

11.9.1 Resolution in Digital Meters

The number of digits used in a digital meter determines the resolution. Thus, a three-digit Display Volt Meter (DVM) for a 0–1 V range will be able to indicate values from zero to 999 mV, with the smallest increment or resolution of 1 mV.

Half Digit

In practice, a fourth digit, usually capable of indicating 0 or 1 only, is placed to the left of active digits. This permits going above 999–1999 to give an overlap between ranges for convenience. This is called *over-ranging*. This type of display is known as a half digit.

The resolution of a digital meter, however, is determined by the number of active or full digits used. If n is the number of full digits, then resolution is $1/10^n$.

For an 8-digit display, the resolution is 1 in 10^8, while for analog meters, in general, it is only 1 in 500.

11.9.2 Sensitivity of Digital Meters

Sensitivity is defined as the smallest change in the input which a digital meter is able to detect.

$$\text{Sensitivity} \qquad S = (fs)_m \times R \tag{11.48}$$

where $(fs)_m$ is the lowest full-scale value of the meter and R is the resolution expressed as decimal.

Example 11.5

A 4½ digit voltmeter is used for voltage measurement.

(a) Find its resolution.

(b) How would 11.76 V be displayed on the 10 V range?

(c) How would 0.5434 be displayed on the 1 V range?

(d) How would 0.5434 be displayed on the 10 V range?

Solution

(a) Resolution = $1/10^4 = 0.0001$ or 0.01% V

(b) There are 5 digit places in a 4-digit display

$\therefore$ 11.76 V would be displayed as 11.760 V on its 10 V scale.

(c) Resolution on the 1 V range = $1 \times 0.0001 = 0.0001$ V

$\therefore$ on the 1 V range, any reading can be shown to the fourth decimal place.

Thus, 0.5434 V would be displayed as 0.5434 V on the 1 V range.

(d) Resolution on the 10 V range = $10 \times 0.0001 = 0.001$ V

Hence, on a 10 V range, readings can be displayed only up to the third decimal place.

$\therefore$ 0.5434 V will be shown as 00.543 V on a 10 V range. The digit 4 in the fourth decimal place will be lost. However, by employing a suitable range, e.g. 1 V, the digit 4 can be retained.

11.9.3 Digital Voltmeters

The schematic block diagram of a DVM is shown in Fig. 11.29.

An analog to Digital Converter (ADC) is the most critical block of a DVM. It decides the accuracy, resolution, etc.

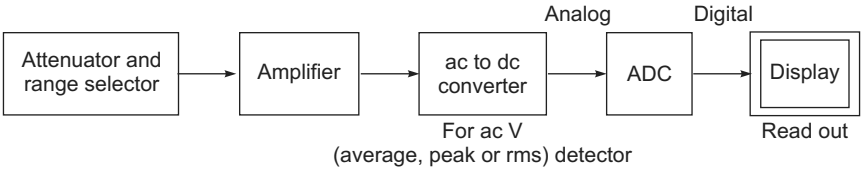


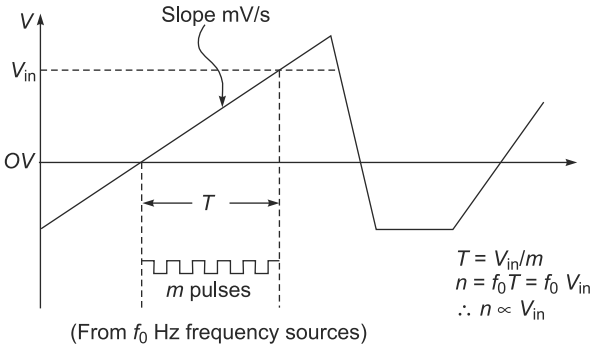
Fig. 11.29 *A digital voltmeter*

The types of DVM (according to the ADC principle) are as follows:

Ramp-Type DVM

The principle behind ramp-type DVM is based on the measurement of the time it takes for a linear ramp voltage to rise from zero to the level of the input voltage, or to decrease from the level of the input voltage to zero.

Conversion from a voltage to a time interval is illustrated by the waveform diagram of Fig. 11.30(a). At the start of the measurement cycle, a ramp voltage is initiated, which is continuously compared with the unknown input voltage. At the instant the ramp voltage is zero, the comparator 1 generates a pulse; another pulse is generated by the comparator 2, when the continuously increasing ramp voltage equals the unknown voltage. The start/stop circuit gives a pulse of width T using the two pulses.



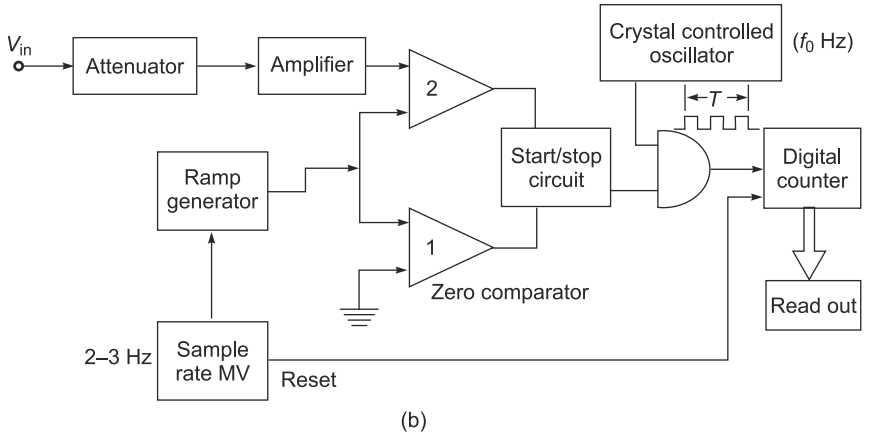


Fig. 11.30 *(a) Waveforms for ramp-type DVM (b) Block diagram of a ramp-type DVM*

The output of oscillator (f_0 Hz) is ANDED with the pulse of width T. Gate output goes to the number of decade counting units (dcUs), which totalise the number of pulses passed through the gate. The decimal number displayed by the readout is the input voltage.

Dual-Slope-Type DVM

We change the capacitor for fixed time T_0 by V_{in}; then, it is discharged to fixed voltage V_{ref} and discharge time T is measured (see Fig. 11.31).

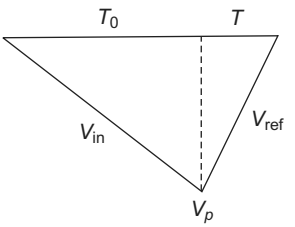


Fig. 11.31 *V-T diagram of dual-slope-type DVM*

Charging: $nVp = -(1/RC) \int V_{in}\, dt$

where V_p = voltage across the capacitor after charging for time T_0

R = charging resistance (in series with the capacitor)

Discharging: $V_p = -(1/RC) \int V_{ref}\, dt$

$$V_p = -(1/RC) \int V_{in} dt = -(1/RC) \int V_{ref} dt$$

$$T = V_{in} T_0 / V_{ref} \quad \text{or} \quad T \propto V_{in}$$

Both T_0 and T times are measured by pulses on the same frequency (f_0) with the same counter.

T_0: count by number of pulses

T: N count: pulses passed discharging

n: $V_{in}\, N_0 / V_{ref}$ or $n \propto V_{in}$

Figure 11.32 shows a complete dual-slope A/D converter. Electronic switches, usually FET switches, are used to switch the input of the integrator alternatively between the reference voltage and the unknown. Another pair of switches apply the integrator output to the automatic zero capacitor and ground the input for the automatic zero function. The switch timing and the counting of the clock pulses to determine the unknown voltage are under control of the control logic. The output is made available to the external electronics after the conversion is complete.

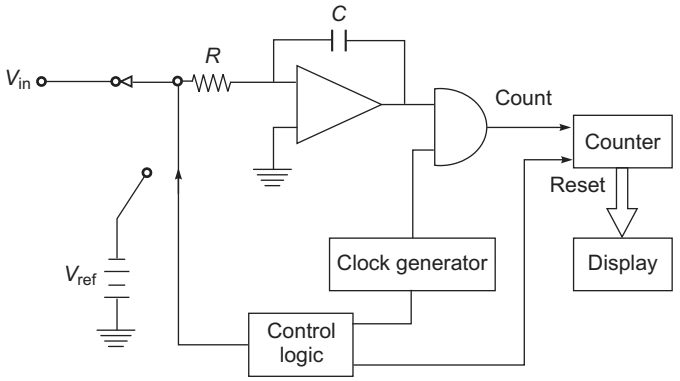


Fig. 11.32 *Dual-slope A/D converter*

Example 11.6

A dual-slope integrating type of A/D converter has an integrating capacitor of 0.22 μF and a resistance of 100 Ω. If the reference voltage is 5 V and the output of the integrator is to remain below 10 V, find the maximum time the reference voltage can be integrated.

Solution Let T be the maximum time for which the reference voltage can be integrated. Then, the voltage across the capacitor after charging for time T is

$$V_p = (1/RC) \int V_{\text{ref}} dt$$

$$V_p = 10 \text{ V}, V_{\text{ref}} = 5 \text{ V}$$

$$\therefore \quad 10 = (1/10^5 \times 0.22 \times 10^{-6}) \int 5 \, dt$$

Thus, $T = 44$ ms

Successive-Approximation-Type DVM

This is the fastest compared to any other type of DVM. It is an electronic implementation of a technique called *binary regression*. This converter compares the analog input to a DAC reference voltage which is repeatedly divided in half. The process is shown in Fig. 11.33, where a three-digit binary number, representing the full voltage E_r, is divided in half (binary number 100), to the corresponding voltage $E_r/2$. A comparison of this reference voltage $E_r/2$ and the analog voltage is made. If the result of this comparison shows that this first approximation is too small (i.e. $E_r/2$ is smaller than the analog input) then the next comparison is made against $E_r/4$ (binary number 010). After four successive approximations, the digital number is resolved.

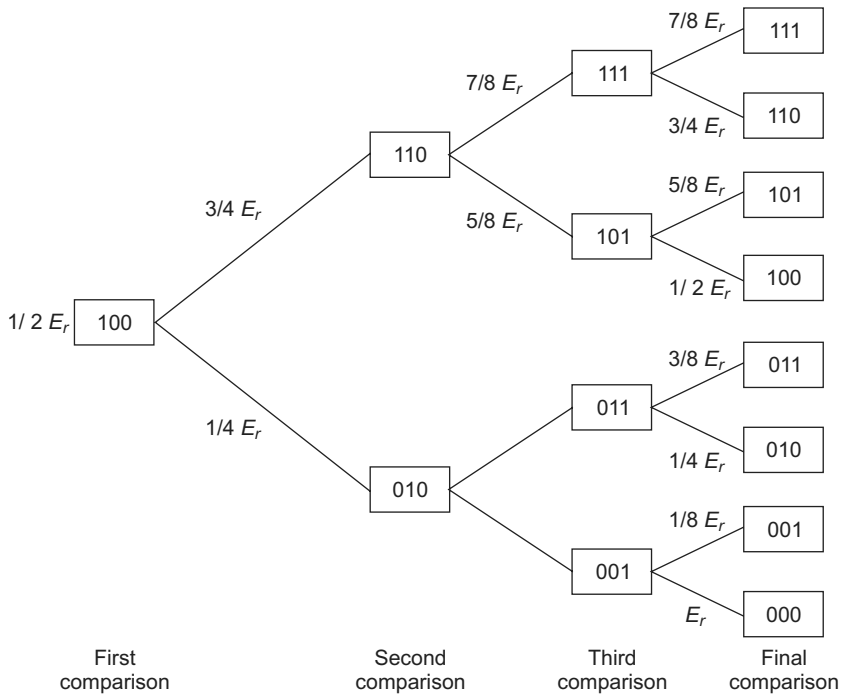


Fig. 11.33 *Operation of successive approximation A/D converter*

At the start of the conversion cycle, both the control resistor and the distribution register are set with a 1 in MSB and 0 in all bits of less significance. Thus, the distribution register shows 1000 and this causes the output voltage at the D/A convertor section to be one half of reference supply. At the same time, a pulse enters the time-delay circuitry. By the time the D/A converter and the comparator have settled, this delayed pulse is gated with the comparator output.

When the next MSB is set in the control register by the action of the timing circuit, the MSB remains in the state 1 or it is reset to 0, depending on the comparator output. The single 1 in the distribution register is shifted to the next position and keeps track of the comparison mode.

The procedure repeats itself (see Fig. 11.34) until the final approximation has been made and the distribution register indicates the end of the conversion.

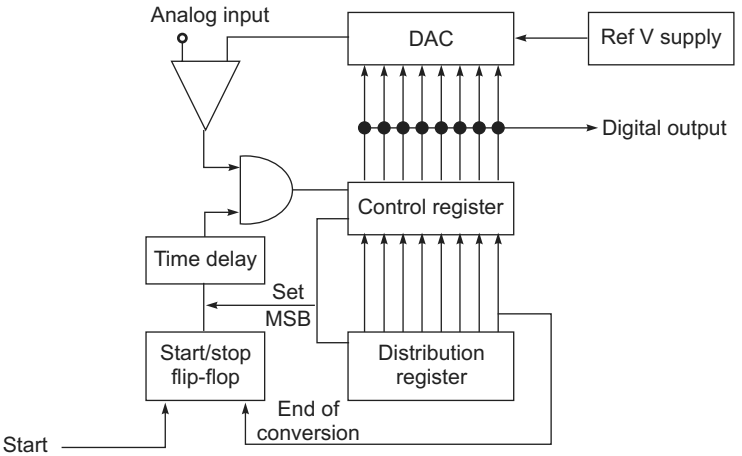


Fig. 11.34 *Block diagram of the successive approximation A/D converter*

Example 11.7

Find the successive approximation A/D output for a 4-bit converter to a 3.217 V input if the reference is 5 V.

Solution For a 4-bit converter, only 4 digits can be shown. Input 3.217 V is approximately equal to 3.25 V. The output can be shown in tabular form as follows:

Pulse number	Value represented	Output (binary number)
1	2.5	1
2	1.25	0
3	0.625	1
4	0.3125	0

$\therefore$ the 4-bit representation is 1010.

Example 11.8

A series type ohm-meter is designed to operate with a 6 V battery with a circuit diagram as shown in Fig. 11.35. The meter movement has an internal resistance of 2 kΩ and requires a current of 100 μA for full-scale deflection. The value of R_1 = 49 kΩ.

(a) Assuming the battery voltage has fallen to 9.5 V, calculate the value of R_2 required to obtain zero reading in the meter.

(b) Under the condition mentioned in part (a), an unknown resistor is connected to the meter causing 60% meter deflection. Calculate the value of the unknown resistance.

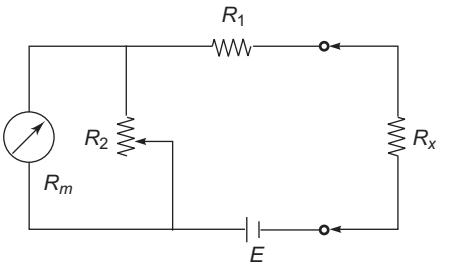


Fig. 11.35

Solution

(a) $R_x = 0$ for zero meter reading, $R_m = 2\ \text{k}\Omega$, $R_1 = 49\ \text{k}\Omega$,

$$I_{\text{fsd}} = 100\ \mu\text{A}$$

Voltage across movement = $2000 \times 100\ \mu\text{A} = 0.2\ \text{V}$

Then $IR_1 + 0.2 = 5.9$

$$I = 116.32\ \mu\text{A}$$

$$I_{\text{sh}} = 116.32\ \mu\text{A} - I_{\text{fsd}} = 16.32\ \mu\text{A}$$

$$R_2 = 0.2\ \text{V}/16.32\ \mu\text{A} = 12.25\ \text{k}\Omega$$

(b) for 60% deflection

$$I = 60 \times 116.32\ \mu\text{A}/100 = 69.8\ \mu\text{A}$$

$$R_{\text{eq}}\ (\text{for meter}) = 5.9/69.8\ \mu\text{A} = 84.53\ \text{k}\Omega$$

$$R_x = 84{,}530 - 49000 - 2000 \times 12.25/11.25$$

$$= 33.81\ \text{k}\Omega$$

Example 11.9

The resistance of the pressure coil branch of the wattmeter W in the circuit of Fig. 11.36 is $R_p\ \Omega$. In the position 2 of the switch, an inductive reactance of $R_p\Omega$ is connected in series with the pressure coil branch. If the readings of the wattmeter in switch positions 1 and 2 are W_1 and W_2 respectively, determine the reactive power taken by the load in terms of W_1 and W_2. Neglect current coil impedance and pressure coil reactance.

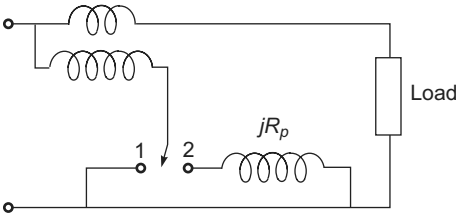


Fig. 11.36

Solution The wattmeter reading at the position 1 is

$$W_1 = (VI_c/k\ R_P)\cos\phi\ d\,M/d\theta \tag{i}$$

The wattmeter reading at the position 2 is

$$W_2 = (VI_c/k\ R_P)\cos(\phi - \alpha)\cos\alpha\ \frac{dM}{d\theta} \tag{ii}$$

where $\alpha = \tan^{-1}(\omega L/R_p)$

$\omega L = Rp$, reactance in series with pressure coil

$\alpha = 45°$

Dividing Eq. (ii) by Eq. (i), we get

$$W_2/W_1 = \cos 45° \cos (\phi - 45°)/\cos \phi$$

$$= (1 + \tan \phi)/2$$

$$\therefore \quad \tan \phi = (2\ W_2 - W_1)/W_1$$

Now reactive power $(P_r) = W_1 \sin \phi$

Thus, $$P_r = W_1 (2W_2 - W_1)/\sqrt{4W_2^2 + 2W_1^2 - 4W_1 W_2}$$

Summary

- Moving Iron (MI) instrument is used to measure both ac and dc, but it gives rms value of ac and average value of dc.
- The two types of MI meters are:

  1. Attraction type 2. Repulsion type.
- Megger is an insulation testing instrument. It is used to measure very high resistance of the order of mega ohms.
- Instrument transformers are used in ac systems for the measurement of current, voltage, power and energy.

  Types: Current transformer, Potential transformer.
- Wheatstone bridge is used to measure resistance.
  Maxwell bridge is used to measure inductance.
  Hay bridge is used to measure high inductance.
  Schering bridge is used to measure high inductance.
  Owen's bridge is used to measure inductance.
  Anderson's bridge is used to measure inductance
  Wien's bridge is used to measure frequency.
- The cause of errors in measuring instruments is distributed capacitance and self-capacitance.
- **Sensitivity of digital meters:**

  It is defined as the smallest change in the input which a digital meter is able to detect.
  Sensitivity $S = (Fs)\ m \times R$
  $(Fs)\ m$ = lowest full-scale value of meter
  R = resolution expressed in decimal.
- An electrical transducer is a device which converts non-electrical input into electrical output.

Exercises

Review Questions

1. What are the basic elements of a measuring instrument?
2. How can we get true values from measurements?
3. Why is the controlling torque needed in a measuring instrument?
4. How can the range of an ammeter/voltmeter be extended?
5. How can an electrodynamometer be converted into an ammeter/voltmeter?
6. Can we measure three-phase power with a single wattmeter and how?
7. In three-phase measurement using the two wattmeter method, if the power factor is zero, what are the two watt readings?
8. A thermocouple instrument measures average value or rms value? Why?
9. How can an instrument transformer extend the range of the ac measuring instrument?
10. Which will give accurate reading, bridge or meter measurement?

Problems

1. A 0–150 V voltmeter has a guaranteed accuracy of 1% full-scale reading, and the voltage measured by this instrument is 85 V. Calculate the limiting error in percentage.
2. The coil of a moving coil galvanometer has 250 turns and a resistance of 150 Ω. The coil dimensions are 2 cm × 2.5 cm. The strength of the uniform magnetic field is 0.12 Wb/m^2. The inertia constant of the moving system in 1.6×10^{-7} kg m^2 and the control torque constant is 2.4×10^{-6} Nm per radian. Assuming that the damping is entirely electromagnetic, determine the value of the resistance to be connected across the galvanometer terminals to obtain critical damping of the moving system.
3. For the instrument mentioned in Example 11.2, find the values of shunt resistances to convert the interament into a multirange ammeter reading upto 10 A, 15 A.
4. Figure 11.37 displays the lissajous patterns for a case where voltage of the same frequency out of different phases are connected to the *Y* and *X* plates of the oscilloscope. Find the phase difference in each case. The spot generating the patterns moves in a clockwise direction.

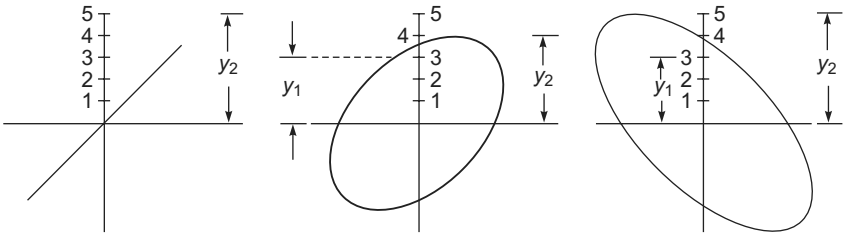


Fig. 11.37

5. The lowest range of a 4.5 digit voltmeter is 10 mV full scale. Find the sensitivity of the meter.
6. A certain 3 digit DVM has an accuracy specification of 0.5% of reading ± 2 digits.
   (a) What is the possible error in volts, when the instrument is reading 6.00 V on its 10 V range?
   (b) What is the possible error in volts, when the instrument is reading 0.20 V on the 10 V range?
   (c) What percentage of the reading is the possible error in the case of (b)?

Multiple-Choice Questions

1. In an instrument, the error when reading at half scale is
   (a) less than the full-scale error
   (b) equal to the full-scale error
   (c) greater than the full-scale error
   (d) equal to half of the full-scale error
2. Which of the following meters has the best accuracy?
   (a) Moving-iron meter (b) Moving-coil meter
   (c) Rectifier-type meter (d) Thermocouple meter
3. A resistor of 10 kΩ with a tolerance of 5% is connected in parallel with a 5 kΩ resistor of 10% tolerance. What is the tolerance limit for the series network?
   (a) 5% (b) 6.67% (c) 10% (d) 8.33%
4. A resistor of 10 kΩ with a tolerance of 5% is connected in parallel with a 5 kΩ resistor of 10% tolerance. What is the tolerance limit for the parallel network?
   (a) 5% (b) 6.67% (c) 10% (d) 8.33%
5. A moving-coil instrument is used
   (a) for low-frequency ac only (b) for both ac and dc circuits
   (c) in dc circuits only (d) for measuring high-frequency ac
6. Moving-iron instruments have a scale, which is
   (a) uniform (b) squared (c) log (d) none of these
7. Electrostatic instruments are used as
   (a) voltmeters only (b) ammeters only
   (c) both voltmeters and ammeters (d) wattmeters only
8. Dynamometer-type instruments can be used for
   (a) ac only (b) dc only (c) both ac and dc (d) none of these
9. Dielectric loss can be measured by
   (a) an energy meter (b) the Wheatstone bridge
   (c) an electrostatic meter (d) none of the above
10. Which of the following ranges of a meter requires the smallest shunt resistance?
    (a) 0–10 mA (b) 0–100 mA (c) 0–1 A (d) 0–10 A

Answers

Multiple-Choice Questions

1. (b) 2. (a) 3. (b) 4. (d) 5. (c)
6. (b) 7. (a) 8. (c) 9. (c) 10. (a)

Power Systems

chapter 12

Goals & Objectives

- Introduction of electric energy and Power system
- Electric supply systems and their energy conversion
- Concept of power generation, transmission and distribution
- Comparison of conductor costs of transmission systems and power factor improvement
- Transmission line performance; transmission and distribution systems
- High voltage dc (HVDC) transmission
- Cable-introduction and types

12.1 INTRODUCTION

Electric energy is most convenient and efficient means for production of light and rotational mechanical motion. It can be transported easily and efficiently over long distances from the production site to myriad points of use (compare this with transporting coal). Electric energy must be generated centrally and instantly transported to vast geographical regions within and beyond national boundaries. It cannot be stored in large quantities, except in batteries for limited use.

Because of these qualities of electric energy, its use has been growing fast in all sectors: industrial, commercial and domestic. With increasing industrial production, new products and new home appliances, the demand for electric energy has been rising very fast. This is particularly so in developing countries, which are trying to catch up with the developed countries, and in a chain reaction, the undeveloped countries are following suit. Apart from industrial conditioning, comfort conditioning of commercial and home areas is adding newer and fast growth electric loads. With limited resources of the globe, this may not go on forever. Intensive research efforts are already on to (i) make electric energy products more efficient, (ii) look for renewable energy sources, (iii) make industrial drives, processes and appliances more efficient (iv) conserve energy and avoid its wastefull use, and (v) limit growth to a sustainable level. This sustainable level has so far eluded every nation.

Usage of electricity in the world has been growing at the rate of about 7%, implying doubling of demand every 10 years. This growth is presented in Fig. 12.1 along with the Indian picture. In India, the means (i.e. generation of electric energy) to meet this burgeoning demand have considerably lagged behind all along

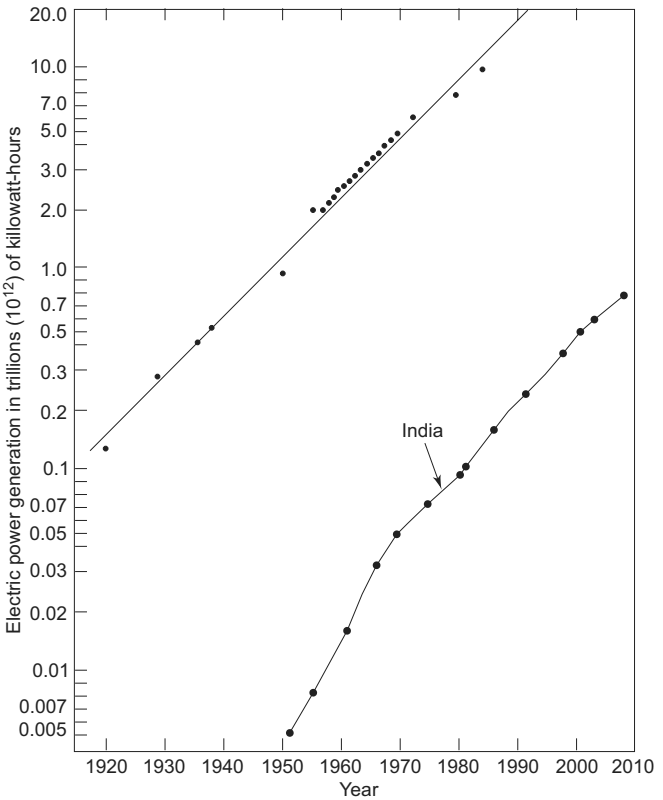


Fig. 12.1 *World growth rate for electricity*

and more so in the past two decades when the effects of compounded growth rate have shown up. Of course, there are many other factors, like inefficient generation, maintenance, insufficient outlay of transmission lines and above all management, which have contributed to the acuteness of the problem. Radical solutions are being groped but have to be applied fast.

The readers interested in reading *Power Systems* in greater and fuller details may refer to the following textbooks on power systems.

1. D P Kothari, and I J Nagrath, *Power System Engineering,* McGraw Hill Education (India), 2nd edn. 2007.
2. D P Kothari and I J Nagrath, *Modern Power System Analysis*, 4th edn. MHE(I), 2011.

Factors Influencing Generation and Transmission

Four main factors that influence electricity supply are as follows:

1. Typical hourly load curves for summer and winter months in a North Indian metropolis are shown in Fig. 12.2. The generation and transmission system must meet this fluctuating load, which is not under the control of generating station engineers. The study of these curves show that there is a steady component of the load, called the *base load*, plus peaks depending on the season and time of the day.
2. Demand is continuously rising over the years as seen from Fig. 12.1 This requires planning, addition of generation and also adding high-voltage and medium-voltage transmission lines. Planning of expansion and construction work must start years ahead. In India, generation and transmission are both heavily lagging behind the rising load. The result is load shedding, both scheduled and unscheduled, particularly in summer.

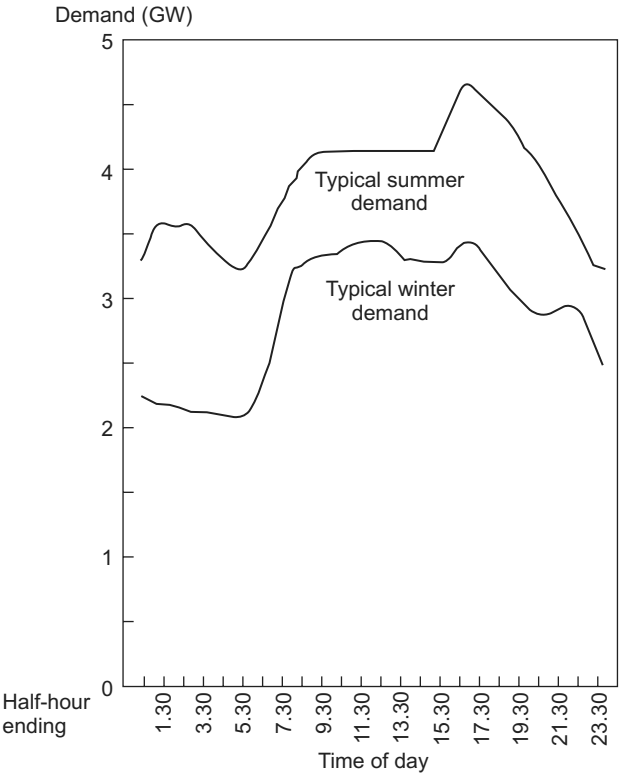


Fig. 12.2 *Typical hourly load demand curve is in gigawatts (GW)*

3. Where coal is the fuel (this is largely so in India), the generating stations have to be sited near the coal mines. The electric power then has to be transmitted over long distances by HV (high voltage) transmission lines. In India, northern and western regions are devoid of coal.
4. Nuclear stations can be sited reasonably close to load centres. Also, with the gas grid continuously expanding, peaking load can be met by gas generating stations.

A picture of the intensity with which load demand is galloping in India, the following statistics, based on Electric Power Survey and prepared by Central Electricity Authority (CEA), are presented in Table 12.1.

Table 12.1 *Energy demand in India*

Year	*Energy demand (billion kWh)*	*Peaking demand (MW)*	*Annual load factor**
2007	665482	89612	0.85
2010		107192	0.844
1012	910475	119089	0.8727

12.2 ENERGY CONVERSION

Electric energy is obtained by conversion from other forms of energy stored in naturally occurring materials or from energy being continuously received from the sun in its primary form or in its secondary manifestations, for example, rain, snow at high altitude, wind plants, etc.

Energy is stored in natural materials (coal, oil, gas and in the atom) in a chemical form. Coal, oil and gas (methane) were formed by natural processes over enormous periods of time aeons ago. These are available near the earth surface or underground, mostly at great depths, particularly, oil and gas. These are limited resources provided by nature and are nonreplenishable. Their extraction leaves gorges, which, when near the earth's surface, render vast tracts of land unfit for use. It is not clearly known what effect is caused by voids deep under the earth caused by oil extraction.

Energy from the atom (nuclear energy) can be obtained from certain materials with a high atomic number like uranium/thorium. Their resources are also limited, though they contain a great amount of energy.

Energy directly received from the sun (during daytime) can be used directly but the surface density of solar energy is quite low and is variable during the day, cloudy weather and different seasons. It is the solar energy, which is responsible for rain/snow and winds. Rain collected at high altitude has potential energy and winds possess kinetic energy. Further, trees, plants and vegetation absorb solar energy, which is stored there in a chemical form. Pull of the moon on earth imparts energy to sea water in the form of tidal waves. High winds cause energy to be imparted to sea waves. Energy in the forms enumerated here are replenishable (*renewable*) and further they are nonpolluting, when used for conversion to the electric-energy form.

The aim of this section is to describe various means and processes for converting the above listed energy forms to electric energy. With certain exceptions, this conversion requires the first step of conversion to rotational mechanical energy, which then is used to run a generator for conversion to electric form.

A panoramic view of energy conversion to electric form is presented in Fig. 12.3, which at a glance brings into focus all aspects of electric energy including conservation. Energy is converted to a mechanical rotational form by means of the following turbines.

- Steam turbine
- Gas turbine
- Hydraulic turbine

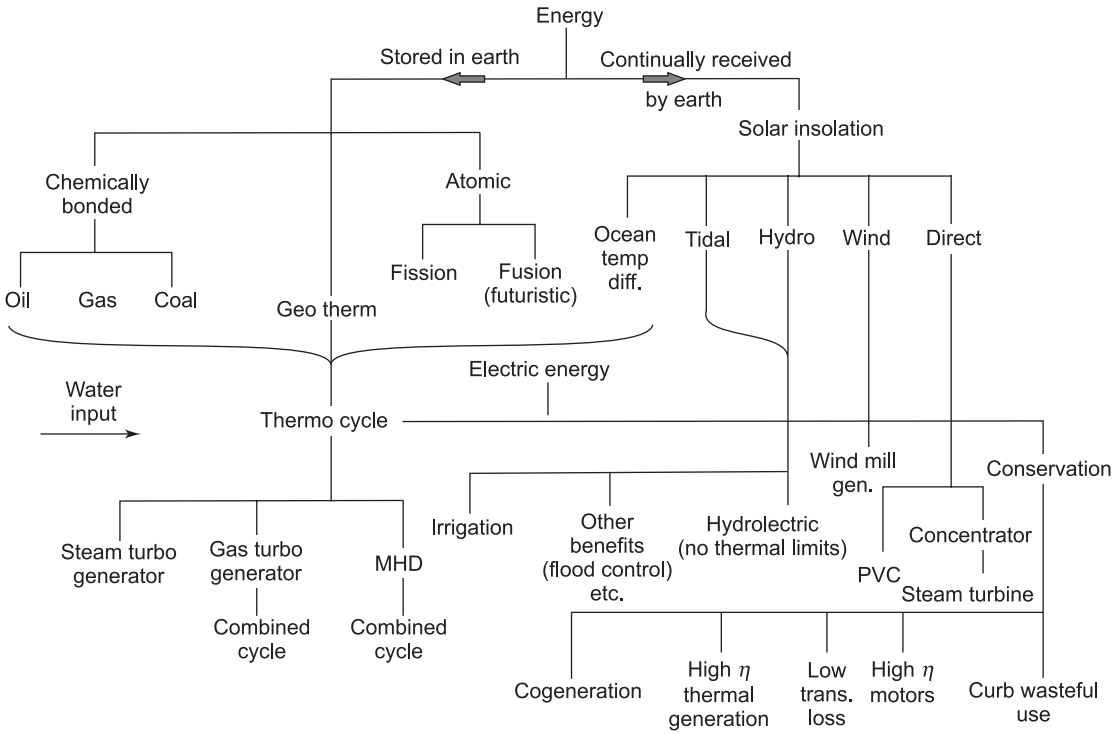


Fig. 12.3 *Energy conversion to electric form*

Steam is raised in a boiler by heat released by combustion of coal/oil or by atomic fission in a suitable vessel called the reactor. Combustion and steam raising is combined into a single boiler unit for coal-oil-based operation. However, in the fission process, steam is raised by heat exchange-processes from the reactor to boiler (or directly in the reactor). A gas turbine directly extracts energy from the products of combustion. In a hydraulic turbine, water's potential energy is directly converted to a rotational form.

12.3 ELECTRIC SUPPLY SYSTEMS

Electric power systems serve two basic functions.

1. Generation of continuous electrical energy at minimum economic and ecological cost.
2. Transporting or transmitting this energy to consumers with maximum efficiency and high reliability and quality (at almost constant voltage and fixed frequency, which is 50 Hz universally, except in USA, where it is 60 Hz.)

The electric energy can be in the ac (alternating current) form or dc (direct current) form. It is now universal to generate ac electric power. Electric energy is integral of power over a period of time. As the size of a power equipment is concerned with power, we shall mostly use the term *power* but sometimes the term *energy* could also be used. Its transmission is also predominantly ac. However, in a part of the power system (modern power system is a complex network) transmission could be in dc. The dc for this purpose is obtained by converters, composed of solid-state switching devices, which interconvert ac to dc and back to

ac. This makes the dc transmission line(s) part of the rest of the system which is ac. The dc power, wherever needed for consumer use, is obtained from ac line through converters.

❑ **Three-phase System** Generation and transmission of electric power is universally ac three-phase 50 Hz. At utilisation end of the system, single-phase loads are fed from each phase.

Components of a power system are broadly classified as follows.

Prime Mover—Generator

The prime mover is normally a turbine, which through mechanical coupling runs a synchronous generator. This arrangement converts mechanical power to electrical form, which is three-phase ac at usually 11/25 kV.

Transformers

These step up the generated voltage to much higher level for transmitting large amounts of power. Transformers are then employed to reduce the voltage to several lower levels till the consumer level of 440/231 V is reached (this is the lowest voltage for electric use).

Transmission Lines

These connect the generator-transformer units to various load centres or to a large system. Power can be transmitted to a large system over a line either way depending on the need.

Power Station

A power station or a power plant is a complex where electrical power is generated starting from the primary energy source (coal, gas, hydro, nuclear) for transmission over line. Present-day power plants are super thermal or mega power plants with large unit sizes to cater to the ever-increasing demand for electric power. In India, such plants, to avoid the high cost of transporting coal, are being build at pit head (near coal mines).

In a thermal Ultra Mega Power Plant (UMPP), the unit system is adopted where a boiler, turbo generator and transformer (step-up) form an independent unit, the unit sizes are in the range of 500–750 MW while 1000 MW unit is being completed.

Hydro plants are dependent on sources of water and nuclear plants must be located at remote places away from populated areas due to safety considerations. This necessitates that power (in hundreds of megawatts) must be evacuated from these plants and transported over EHV (Extra High Voltage) transmission line covering distances of several hundred kilometers. EHV are voltage in the range above 220 kV and UHV (Ultra High Voltage) means voltage greater than 700 kV.

Power Grid

A modern power system is a large complex network feeding several load centres from where the consumers are fed. The power system spreads over vast geographical areas wherein transmission lines may be several hundred kilometres long, transporting power from one area to another. Such power flows are directionally controllable.

This kind of interconnection in power-system parlance is known as power grid (or grid in short). The advantage and economics of grid formation shall be taken up later in this chapter. In India, we have a state-owned company, *Power Grid Corporation of India* to manage power flows as per inter-area contracts for sale/purchase of power.

12.4 ELECTRICAL ELEMENTS

Electrical equipment are composed of (or can be modelled as) active and passive elements. Active elements are sources or sinks of power, which can supply or receive unlimited amount of energy. There are electric generators or motors in electrical power systems. The passive elements are dissipative (nonconservative) and conservative. The conservative elements are inductor and capacitor, which can store electric energy or the same can be retrieved from the element without any loss of energy. The dissipative element is the resistor which only absorbs electric energy and converts it to heat form (the process is irreversible).

Electric-power system components are modelled as sources, with resistors (R), inductors (L) and capacitor (C) elements. Their electrical terminal behaviour is governed by linear laws. The element has temperature dependency which has been pointed out in Chapter 1.

12.5 CONCEPT OF POWER TRANSMISSION

Consider an elementary system composed of an ac generator (coupled to prime mover), *LV-HV* transformer, a transmission line and *HV-LV* transformer feeding the load as shown in Fig 12.4(a). In a power-system diagram, the prime mover is normally not indicated. This is the representation of *one phase of a three-phase* system. A three-phase transmission line has only three lines as the common neutral line is not needed to carry any current.

We shall develop the circuit model of this system itemwise.

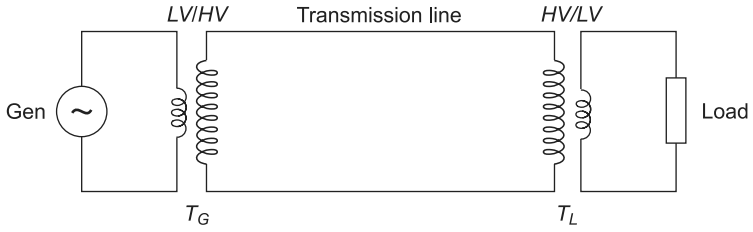


Fig. 12.4(a) *Elementary power-transmission system*

12.5.1 Circuit Model

Generator

It has an induced emf and a series inductive reactance (synchronous reactance).

Transformer

It has a series inductive reactance but negligible resistance.

Transmission Line

It has resistance and inductance in series and capacitance between lines, which is in shunt. These parameters (R, L, C) are proportional to line length.

Load

It can be represented by resistances and inductances in series or in parallel as the overall load is normally inductive. Load comprises lighting, fans (small motors), household appliances driven by small motors, cooking ranges (heating elements), industrial motors (predominantly induction motors), and welding appliances, etc.

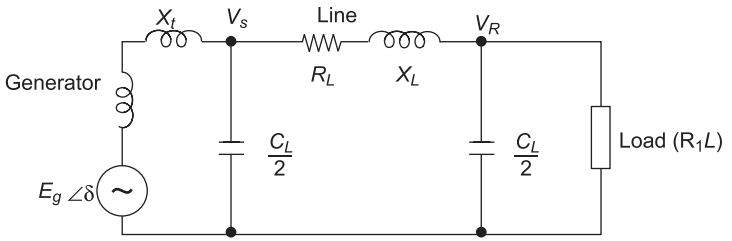


Fig. 12.4(b) *Circuit model of Fig. 12.4(a)*

The circuit model of the system of Fig. 12.4(a) is drawn in Fig. 12.4(b). In the load, I^2R is converted to useful form at the consumer, while I^2R in the transmission line is lost (in form of heat to environment). This loss determines the power efficiency of the system, so it should be kept low.

The line capacitance is very small and can be ignored except for long lines. In our study, we shall consider the line to have only resistance and inductance.

In the system of Fig. 12.4(a), the power flows from the generator to load. It can be shown and should be noted that power always flows from the terminal whose voltage leads the other terminal.

12.5.2 Classification of Lines

Direct Current (dc) Systems

(a) dc 2-wire, 1 wire earthed
(b) dc 1-wire, earth return
(c) dc 2-wire, mid-point earthed
(d) dc three-wire

Alternating Current (ac) Systems

(a) Single-phase, 2-wire, 1 wire earthed
(b) Single-phase, 1-wire, earth return
(c) Single-phase, 2-wire, mid-point earthed
(d) Single-phase, three-wire
(e) Two-phase, three-wire
(f) Two-phase, 4-wire
(g) Three-phase, three-wire
(h) Three-phase, 4-wire, one is neutral which is earthed

All these systems can be used in practice. Each has its own field of application. Direct current, 2-wire, mid-point earthed system is used for transmitting large amounts of power over long distances. A three-phase 3-wire ac system is used for transmission and primary distribution. For secondary distribution, a three-phase, 4-wire system is normally employed and it supplies industrial and other large consumers. The domestic

and other small loads are supplied with single-phase system whose one wire is the phase of three-phase, of 4-wire and the second wire is the neutral.

The lines are predominantly overhead. Underground cables are used where it is a must, as in a congested area. For connection across small sea distances, the only choice is an underwater cable. Cables are several times more expensive than overhead lines.

12.6 SYSTEM VOLTAGE AND TRANSMISSION EFFICIENCY

Consider a three-phase system.

Let P = power to be transmitted per phase in MW
V = voltage/phase in kV
I = current/phase in A
L = line length in km
A = conductor cross-sectional area in m^2
ρ = specific resistance of the conductor material in ohm-m
R = resistance of each conductor in ohms
J = permissible current density in A/m^2
$\cos \phi$ = power factor of the load

Active (Real) power per phase is given by

$$P = VI \cos \phi$$

$$\therefore \quad I = P/V \cos \phi \tag{12.1}$$

But current density $J = \dfrac{I}{A}$

$$\therefore \quad A = \frac{P}{JV \cos \phi} \tag{12.2}$$

Resistance of conductor is $R = \dfrac{\rho L}{A} = \dfrac{\rho LJV \cos \phi}{P}$ (12.3)

Real Power Loss

The power loss in the line per phase is

$$P_L = I^2R = \left(\frac{P}{V \cos \phi}\right)^2 \frac{\rho LJV \cos \phi}{P}$$

or

$$P_L = \frac{J \rho LP}{V \cos \phi} \tag{12.4}$$

Then it is easy to see that *transmission line power loss is inversely proportional to both the system voltage and the power factor*. Lower power loss implies high system efficiency as is shown by the derivation given below.

Transmission Efficiency

The efficiency of transmission (η_T) is given by

$$\eta_T = \frac{\text{Line output}}{\text{Line output + Line loss}}$$

$$= \frac{P}{P + \frac{J\rho LP}{V\cos\phi}} = \frac{1}{1 + \frac{J\rho L}{V\cos\phi}}$$

$$= \left[1 + \frac{J\rho L}{V\cos\phi}\right]^{-1} \tag{12.5}$$

Expanding using Binomial theorem and neglecting higher order terms, we get

$$\eta_T \cong 1 - \frac{J\rho L}{V\cos\phi} \tag{12.6}$$

It is clear from Eq. (12.6) that the *efficiency of transmission increases with increase of supply voltage and power factor.*

It immediately follows from the above results that for large power transmission, there is no choice but to go for higher line voltage such as 440 kV (line to line) or 750 kV (line to line).

Kelvin's Law

The most economical size of the copper aluminum conductor for the transmission of electrical energy will be formed by comparing the annual interest of money value of the conductor copper with the money value of the energy lost annually due to current flow in conductor. The most economical conductor area is given by Kelvin's law presently graphically in Fig. 12.5, in which

C_1 = PAx; P is constant
A = area of the conductor
x = annual interest and depreciation
C_2 = $\frac{Q}{A}$; Q is constant
A = area of the conductor

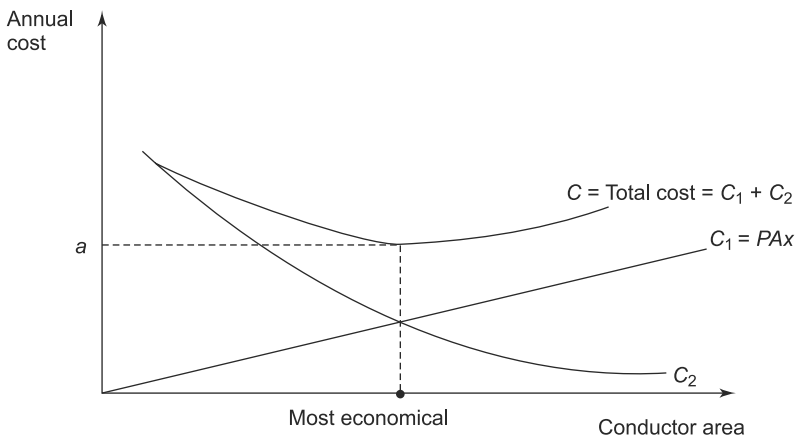


Fig. 12.5 *Graphical form of Kelvin's law*

The annual cost of conductor is proportional to conductor area, so it is a straight line. The annual cost of energy dissipated is inversely proportional to conductor area, so it is a rectangular hyperbola shaped in the graph. It is also clear that the most economical conductor area is given by the point where the two graphs intersect each other.

Modified Kelvin's Law

The actual Kelvin's law is based on the assumption that cost of towers and their foundation, insulators and their erection, etc. are all independent of the conductor area but practically it is not true. The increase in conductor size results in increased mechanical stress to the towers and so they need heavier insulators and towers. Therefore, $C_1 = R_s\,(PA + K)\,x$ where P and K are constants and x is the rate of annual interest and depreciation.

12.7 COMPARISON OF CONDUCTOR COSTS OF TRANSMISSION SYSTEMS

The conductor cost forms the main expenditure of the line. Therefore, it is necessary to compare it in various systems. It is assumed that power transmitted, length of line, and maximum voltage to earth are same in all cases.

1. dc Three-wire System (Fig. 12.6)

In this system, there are three conductors, namely two outers and one middle conductor. The middle conductor is earthed at the supply end. When the load is balanced, the current in the middle (neutral) conductor is zero. Therefore,

Current $\qquad I_1 = \dfrac{P}{2V}$

Line losses $= 2I^2$,

$$R_1 = 2\frac{P^2}{4V^2}R_1 = \frac{P^2 R_1}{2V^2} \qquad (12.7)$$

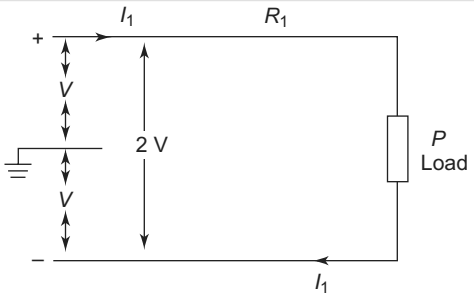


Fig. 12.6 *dc three-wire system*

2. Single-phase 2-wire System with One Wire Earthed (Fig. 12.7)

Let V be the maximum voltage to earth.

$\therefore$ the rms voltage to be earth is

$$V_{\text{rms}} = V/\sqrt{2}$$

Let I_2 be the load current and cos ϕ be the power factor of the load.

$$\therefore \qquad I_2 = \frac{P}{V_{\text{rms}}\cos\phi} = \frac{P}{\frac{V}{\sqrt{2}}\cos\phi}$$

$$\therefore \qquad \text{line losses} = 2\,I_2^2 R_2$$

$$= \frac{2\times 2P^2 R_2}{V^2\cos^2\phi} = \frac{4P^2 R_2}{V^2\cos^2\phi}$$

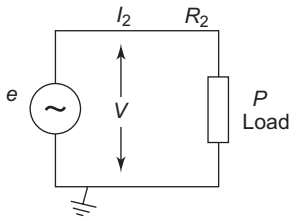


Fig. 12.7 *Single-phase, 2-wire system, one wire earthed*

3. Three-phase, Three-wire, Star-connected System *(Neutral point at earth potential)*

The system is shown in Fig (12.8).

rms phase voltage = $V/2$

Line voltage = $3V/\sqrt{2}$

$$\text{Current} = I_3 = \frac{P}{\sqrt{3}\frac{\sqrt{3}}{2}V\cos\phi} = \frac{\sqrt{2}\,P}{3V\cos\phi} \tag{12.8}$$

$$\text{Line losses} = 3\,I^2{}_3\,R_3 = \frac{3\times 2P^2\,R_3}{9V^2\cos^2\phi} = \frac{2P^2\,R_3}{3V^2\cos^2\phi} \tag{12.9}$$

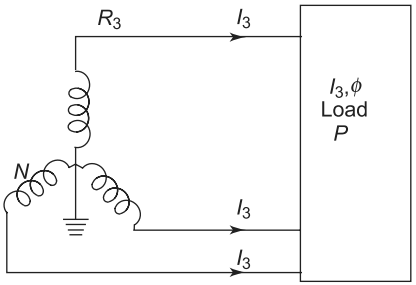


Fig. 12.8 *3-phase, 3-wire, star-connected system*

❑ **Comparison** We assume equal line losses and therefore equal efficiency of transmission.

Equating equations $P = VI = I^2R = V^2/R$ and Eq. (12.9) we get

$$\frac{P^2R_1}{2V^2} = \frac{4P^2R_2}{V^2\cos^2\phi} = \frac{2P^2\,R_3}{3V^2\cos^2\phi}$$

$$\frac{R_1}{2} = \frac{4R_2}{\cos^2\phi} = \frac{2R_3}{3\cos^2\phi}$$

Let us compute the ratios 01.

Resistance, i.e. area

$$\frac{R_2}{R_1} = \frac{\cos^2\phi}{8}$$

$$\therefore \quad \frac{A_1}{A_2} = \frac{\cos^2\phi}{8};\ \frac{R_3}{R_1} = \frac{3\cos^2\phi}{4}$$

$$\frac{A_1}{A_3} = \frac{3\cos^2\phi}{4}$$

$$A_1 : A_2 : A_3 = 1 : \frac{8}{\cos^2\phi} : \frac{4}{3\cos^2\phi} \tag{12.10}$$

In cases (1) and (2), there are two conductors, but in the case (3) there are three conductors.

Hence, the volume of copper or aluminium is

$$V_1 : V_2 : V_3 = 2 : \frac{16}{\cos^2\phi} : \frac{12}{3\cos^2\phi}$$

$$= 1 : \frac{8}{\cos^2\phi} : \frac{2}{\cos^2\phi} \tag{12.11}$$

Thus, it is concluded that dc, 2-phase, 2 wire mid-point earthed system is the cheapest on the basis of conductor cost alone and ac three-phase, three-wire star-connected system is far more economical than single-phase system.

Even though three-wire dc transmission is cheapest on copper volume and on line-loss basis, dc voltage levels cannot be changed as easily and as cheaply as the ac voltages with transformer. Consequently, dc has come into use recently for transmission of a large chunk of power at high voltage. As such, it is interconnected to the remaining part of the system, which is high voltage ac.

12.8 POWER-FACTOR IMPROVEMENT

This has already been discussed briefly in Chapter 4. At low power factor, the load draws a large current with consequent increase in voltage drop, losses resulting in lower efficiency and higher voltage regulation. Larger current requires higher current rated lines, switchgear, transformers, etc. with consequent increase of equipment cost. Thus, both the capital and running costs are increased due to low pf (lagging or leading) and this is uneconomical from the supplier's point of view. The usual reason for low power factor is the presence of large number of inductive loads like induction motors, particularly if these are lightly loaded. Further, arc lamps, electric discharge lamps, industrial-arc furnaces and welding equipment operate at low lagging power factors.

As low-load pf is uneconomical to the electric-supply company, it charges a two-part tariff; one based on electric energy consumed and the other based on maximum kVA demand. As low pf for a given real power load means larger current and so higher kVA, the consumer is thereby forced to install power-factor improvement at its installation.

12.8.1 Concept of VARs—Positive and Negative

This concept is helpful in understanding the method of pf improvement or, in general, pf correction. Consider an inductance and capacitance current as in Figs 12.9(a) and (b) respectively.

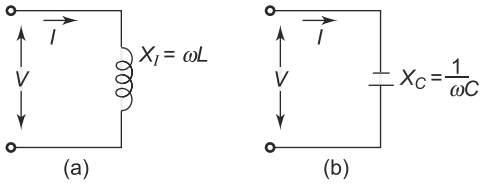


Fig. 12.9 *VARs concept*

Inductance

Its current I lags the voltage V across it by 90°. The inductance draws volt-amp of

$$VAR = VI = V\frac{V}{X_L} = \frac{V^2}{X_L}$$

$$= (IX_L)I = I^2X_L$$

The VARs drawn by inductance (or inductive reactance) are labelled as positive VARs. It can be alternatively considered that inductive reactance supplies negative VARs.

Capacitance

Its current leads the voltage V across it by 90°. The capacitance draws volt-amp of

$$VAR = VI = V^2/X_C = I^2X_C$$

The capacitance (capacitive reactance) draws negative VARs or alternatively supplies positive VARs.

The basic principal of pf improvement is thus to supply positive VARs (from a capacitor across load) to compensate the VARs drawn by the inductive (low pf) load.

The power factor of any load can be improved by the following methods.

(a) By using static compensator (static capacitors)

(b) By using dynamic compensator (synchronous motors)

12.8.2 Power-factor Correction by Static Capacitors

Consider *RL* load supplied at voltage *V* as given in Fig 12.10(a). The phasor diagram of this circuit is given in Fig. 12.10(b).

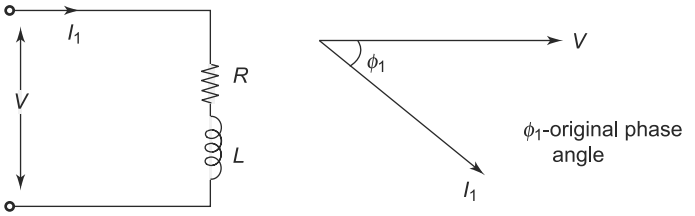


Fig. 12.10

Let a capacitor *C* be placed in parallel with the load [Fig 12.11(a)]. It will draw I_c (leading) form the supply. The resultant current will now be $\overline{I}_2 = \overline{I}_1 + \overline{I}_C$.

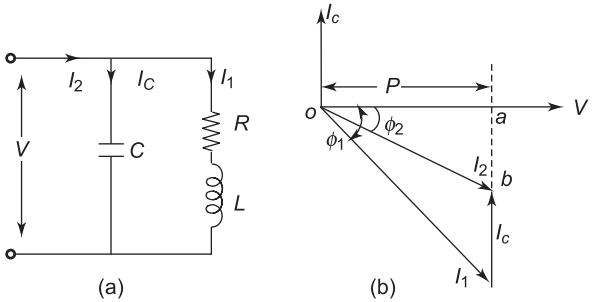


Fig. 12.11 *Phasor diagram*

The phasor diagram is drawn in Fig. 12.11(b) wherein we find $\phi_2 < \phi_1$. The real power *P* in given as

$$Oa = I_1 \cos \phi_1 = I_2 \cos \phi_2, \cos \phi_2 > \cos \phi_1 \quad \therefore I_2 < I_1$$

It means that the current I_2 drawn from the supply is less than the load current I_1, thereby reducing system losses and improving efficiency as well.

Further, since $VI_2 \cos \phi_2 = VI_1 \cos \phi_1$, real power taken from the supply remains the same.

Computation of Capacitor Rating

From Fig. 12.11,

$$I_C = I_1 \sin \phi_1 - I_2 \sin \phi_2$$

or $$VI_C = VI_1 \sin \phi_1 - VI_2 \sin \phi_2$$

Using the fact that load power

$$P = VI \cos \phi_1 = VI_2 \cos \phi_2$$

We can write $Q_C = P (\tan \phi_1 - \tan \phi_2)$

where $Q_C = VI_C$ = capacitor volt-amp

The capacitor current is given as

$$I_C = I_1 \cos \phi_1 (\tan \phi_1 - \tan \phi_2) \tag{12.12a}$$

Also $$I = \frac{V}{X_C} = V\omega_C ; Q_C = VI_C = V^2\omega_C \quad (12.12b)$$

which gives the capacitor value of $C = \frac{Q_C}{\omega V^2}$.

For a given power P, cos ϕ_1 load pf and required pf cos ϕ_2 are known from which we can find the capacitor needed from Eqs (12.12a) and (12.12b). It is seen that compensating capacitor needed for pf improvement is inversely proportional to V^2.

For achieving unity pf($\phi_2 = 0$),

$$Q_c = P \tan \phi_1 \quad (12.13)$$

Apart from the consumer improving the pf of its load to reduce the electricity bill as per two-part tariff, there is need to install VAR compensators (or generators) at certain important system buses to improve the system voltage and to increase the real power transfer over a high-tension (high voltage) transmission line. Under heavy load condition, the system voltage tends to sag which is remedied by injecting positive VARs into the system by the compensator. Under light load conditions, the voltage tends to rise and so negative VARs are injected into the system.

Advantages and Drawbacks of Static Capacitors

Capacitors are static, robust, easy to install, occupy less space and not require any special foundation. They can be used in modules; easy maintenance and loss free are other advantages.

When negative VARs are needed, inductor banks are switched on.

Capacitor banks can be switched on in steps. However, stepless (smooth) VAR control can now be achieved using SCR (Silicon Controlled Rectifier) circuitry. The effectiveness of capacitors becomes less as the voltage sags under full load conditions, (see Eq. (12.12). If the system voltage contains appreciable harmonics, the capacitors may be overloaded considerably. $I_C = V\omega C$; at high ω, I_C is high causing overload. Also, capacitors act as short circuit when switched in and further there is a possibility of series resonance with line inductance, particularly at harmonic frequencies.

12.8.3 Power-Factor Correction by Synchronous Motors

When a synchronous motor runs at no load with adjustable excitation over a wide range, pf can be improved. It can generate or absorb VARs by varying the excitation of its field winding. It can be made to feed positive VARs into the line under over-excited conditions and feed negative VARs when under-excited. A machine thus running is called a *synchronous condenser or a dynamic compensator*. They can provide both positive and negative VARs, which are continuously adjustable. VAR injection at a given excitation is less sensitive to change in bus voltage. But these are costly as installation, maintenance and remote-controlled operations are not easy.

Economics of Power-Factor Improvement

As KVA demand is reduced with improvement in pf, it results in annual saving over the maximum KVA demand charges. However, there is capital investment on the power-factor correction equipment. Thus, there is expenditure every year in the form of interest, depreciation, etc. on the initial cost of pf improvement equipment. The net annual saving will be equal to the annual saving on the maximum KVA demand charges minus annual expenditure on the equipment. The most economical pf will be that pf at which net annual saving is maximum.

12.9 THE ONE-LINE (SINGLE-LINE) DIAGRAM

A one-line diagram of a power system shows the main connections and arrangement of components. Any particular component may or may not be shown depending on the information required in a system study, e.g. circuit breakers need not be shown in a load-flow study but are a must for a protection study. Power-system networks are represented by one-line diagrams using suitable symbols for generators, motors, transformers and loads. It is a convenient practical way of network representation rather than drawing the actual three-phase diagram, which may indeed be quite cumbersome and confusing for a practical size network. Generator and transformer connections—star, delta and neutral grounding—are indicated by symbols drawn by the side of the representation of these elements. Circuit breakers are represented as rectangular blocks. Figure 12.12 shows the one-line diagram of a simple power system.

A balanced three-phase system is studied on a per-phase basis. A three-phase balanced system is effectively and concisely represented by a single-line diagram. A single line diagram cannot be used for all types of studies. For example, it fails to depict the conditions during unbalanced operation of a power system.

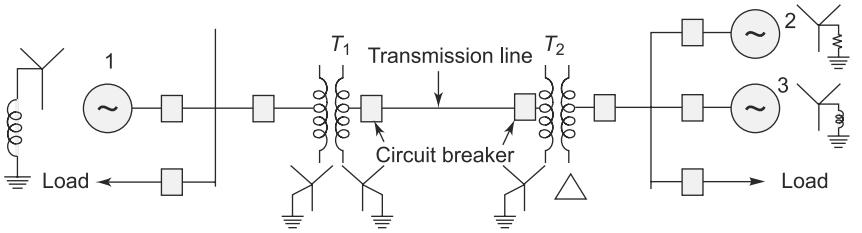


Fig. 12.12 *One-line representation of a simple power system*

12.10 TRANSMISSION LINE PERFORMANCE

One phase diagram of a transmission-line feeding load is drawn in Fig. 12.13(a). Here, line resistance is ignored. In this diagram, V_S = sending end voltage, V_R = receiving end voltage, X_L = line reactance. The phasor diagram for this system is drawn in Fig. 12.13(b) wherein reactance voltage drop in line = $I_R X_L$. It leads line current I_R by ϕ.

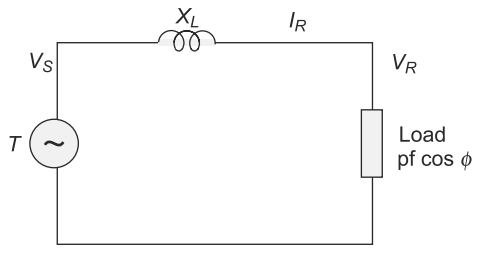


Fig. 12.13(a) *Transmission-line feeding load*

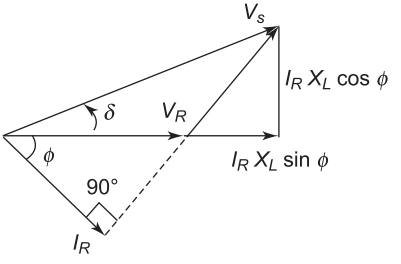


Fig. 12.13(b) *Phasor diagram*

From the phasor diagram,

$$V_S = [(V_R + I_R X_L \sin \phi)^2 + (I_R \times X_L \cos \phi)^2]^{1/2} \tag{12.14}$$

$$= [V_R^2 + 2V_R I_R X_L \sin\phi + I_R^2 X_L^2]^{1/2}$$

or $$V_S = V_R\left[1 + \frac{2I_R X_L}{V_R}\sin\phi + \frac{I_R^2 X_L^2}{V_R^2}\right]^{1/2} \quad (12.15)$$

For short lines,

$$I_R X_L << V_R; \text{ so } \frac{I_R^2 X_L^2}{V_R^2} \simeq 0$$

It is sufficiently accurate to consider only the first term in Taylor series expansion of Eq. (12.15). Thus,

$$V_S = V_R + I_R X_L \sin\phi \quad (12.16a)$$

Voltage regulation of the line is the line voltage drop as a percentage of the receiving and voltage at full load.

Thus, Voltage regulation $= \frac{V_S - V_R}{V_R}$; under full load at specified pf

$$= \frac{I_R X_L \sin\phi}{V_R} \quad (12.17a)$$

Equation (12.16a) get modified as below if the line resistance R_L is taken into account

$$V_S = V_R + I_R X_L \sin\phi\, I_R R_L \cos\phi \quad (12.16b)$$

and voltage regulation $= \frac{I_R X_L \sin\phi + I_R R_L \cos\phi}{V_R}$ (12.17b)

12.11 TRANSMISSION AND DISTRIBUTION SYSTEMS

Large power plants are located close to regions where fossil fuels are mined. Hydraulic dams can be but near foothills or where there is sufficient change in river level. Even nuclear power plants are located away from populated areas. This means that electrical power has to be transported to load centres over transmission lines and suitably distributed.

Electricity supply systems are invariably three-phase and they are so designed and loaded that the operation is balanced three phase. This is assured by allotting nearly equal domestic load on each phase; industrial loads are usually three-phase and balanced.

Symbols used in one line diagram of a power system are depicted in Fig. 12.14. A typical line diagram of part of a power system is drawn in Fig. 12.15 for illustration. The generator is star connected with neutral grounded through resistance. The purpose of grounding is that if a line or any phase of any part of the system faults to ground, sufficient current will flow from the fault point to neutral via the ground connection. This is sensed by protective devices, which disconnect the faulty part of the system so that no equipment damage occurs.

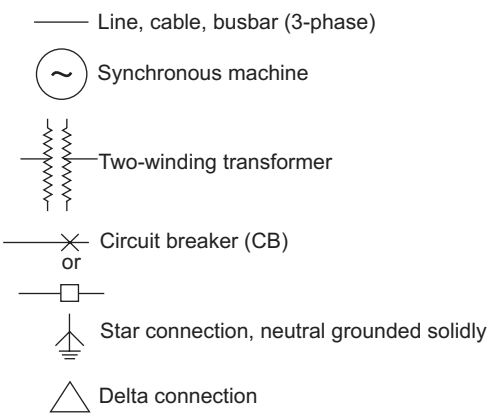


Fig. 12.14 *Symbols for representing the components of a three-phase power system*

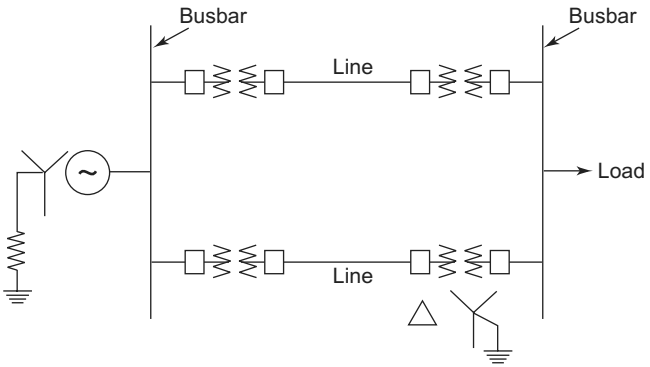


Fig. 12.15 *Line diagram of part of a power system*

The generator voltage is raised to transmission-line level by the two (independent) line transformers. The voltage is brought down by the transformers at the end of the line to the values required for feeding the load. Circuit breakers are located on each side of the transformer to disconnect transformer and line from the generator and load in the event of a fault on the line. Two lines in parallel build security into the system as in the event one is faulted, the other can feed the load, though not the full load.

Before proceeding further, the terminology used in power systems is listed below, with explanations wherever necessary.

Systems

The complete electrical networks: prime movers, generators, transformers, lines and loads.

Busbar

It is a solid electrical connection (of zero impedance) made of aluminium or copper bars connecting various power-system components like generators, transformers, lines, loads, etc. Busbars are shown in Fig. 12.16.

Load

It is a device or devices, which draw electrical power from the busbar to do useful work for the consumers: drive motors and other processes in industry; domestic load is lighting, refrigeration, comfort conditioning, small electrical appliances, etc.

Earthing

Earth connecting entails burying deep into ground large assemblies of (grounding) conducting rods embedded in moist coal (powdered) and lime. Conductors of large cross sections are used to bring the earth connection to the ground level. This is used to connect the frames of electrical devices, neutral of generators and ground conductor of the lines, sheathing of cables, etc. This prevents the voltage of any of these devices rising above the ground voltage in the event of fault to earth on any part of the system.

Outage

Removal of a circuit either deliberately (in case of fault or for maintenances) or inadvertently.

Security of Supply

Provisions made to ensure continuity of supply to consumers in the event of some outage or loss of generator. Only certain combination of events can be covered, while other combinations are considered a rare event (very low probability of occurrence).

In India, with long hours of load shedding being a daily routine, it is not meaningful to talk of security at present.

12.11.1 Transmission

Transmission of the system implies bulk transfer of power by high voltage links between generation and load centres. A distribution network conveys the power form the bulk load centres to consumers by lower voltage network, which then is reduced to consumer voltage level at the distribution substations.

Generator voltage is usually in the range of 11 to 25 kV, which is raised by transformers to the main transmission voltage. Large amounts of power are transmitted at ac voltage of 400 kV, 500 kV and even 750 kV (not in India yet). The network formed by these high-voltage lines is referred as *supergrid*. Subtransmission voltage levels are 132 kV, 115 kV and distribution voltage levels are 33 kV, 11 kV. The consumer feeders are at 400/230 V three-phase/1-phase.

High-Voltage Dc (HVDC) transmission is presented in Section 12.12. Higher voltage levels imply that large chunks of power can be transmitted for same current level, but it has to be economically balanced against cost of higher transmission towers and higher cost of insulators, and stronger conductor reinforcement because of longer span between towers. To make it economical, towers may be designed to carry two three-phase lines, on both the sides.

A small portion of a large transmission network is shown in Fig. 12.16 in one line. The figure shows the high-voltage grid, Grid Power Supply (GPS) and interconnection to the rest of the system and one distribution bus with embedded generators and local generators.

It is seen from above that the power system is made up of interconnected networks (grids) at various voltage levels and also fed by power plants of large, medium and small size. This is illustrated in the conceptual diagram in Fig. 12.17.

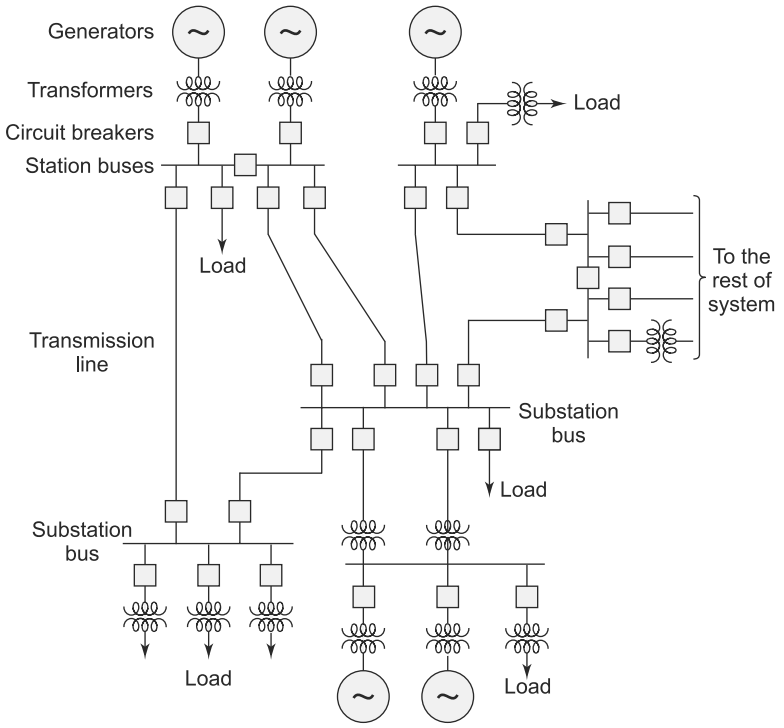


Fig. 12.16 *One-line diagram, power system grid*

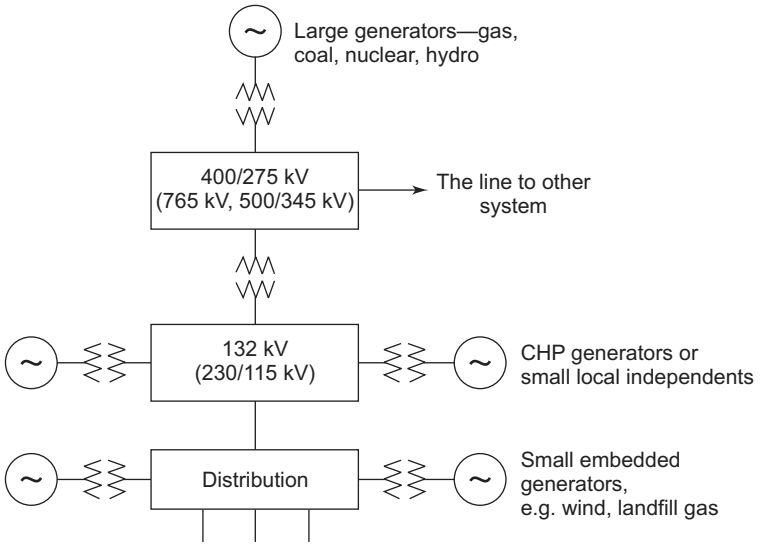


Fig. 12.17 *Schematic diagram of the constituent networks of a power-supply system*

Why Interconnection

Interconnection, or grid formation, in a power system provides the following facilities and advantages:

- Evacuating power from surplus areas and transporting it to power-deficient areas. This situation can also arise in case of generation outage.
- Load can still be met in case of an line outage: also see Fig. 12.11.
- Power plants of various kinds, efficiencies and ages can be scheduled to meet the loads on the grid in an economical manner by scheduling a particular mix of generation on hourly basis. The main base load is always fed by high-efficiency generators, nuclear plants, etc.

12.11.2 Distribution System

Here, the voltage is stepped down to 132 kV or 11 kV/400 V (230 V single phase). This part of the system feeds industrial, commercial and domestic consumers. Usually, there are no interconnections, but isolators are used to interconnect two sections, when there is an outage on one side. A typical radial distribution system along with its link to subtransmission and transmission is shown in Fig 12.18.

Ring Mains

The radical distribution is simple and economic. But the reliability of the system is poor and it leads to interruption of energy supply if there is fault in the line. To overcome this, ring-main type distribution is used.

The ring main distributors are of two types:

❑ **Single Ring** Here, the distribution is carried out by forming a closed circle, i.e. two ends are connected together as shown in Fig. 12.19.

❑ **Double-ring Distributor** It looks like an interconnected distribution system. To minimise the voltage drop at the far end, the interconnector is used as shown in Fig. 12.20.

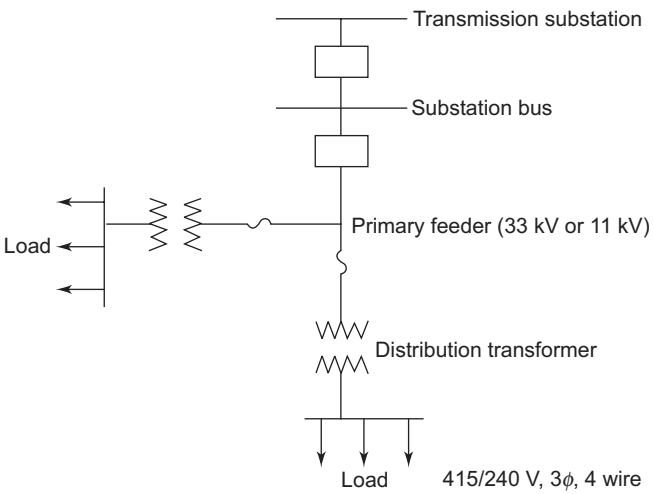


Fig. 12.18 *Simple form of radial distribution system*

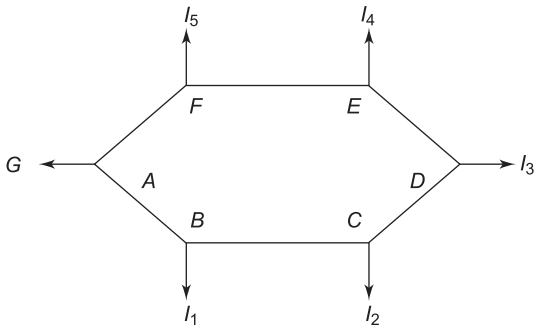


Fig. 12.19 *Single-ring system*

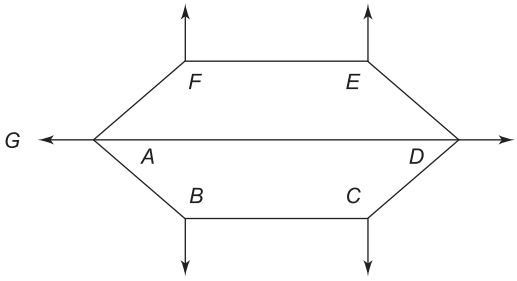


Fig. 12.20 *Double-ring distributor*

Line Loss

In transmission and distribution networks, there are PR losses in lines and transformers. These average at about 20% of the power input. It is also to be remarked here that only 1/5 of the heat energy put in the furnace reaches the user. All this should make us realise that electric energy must be utilised in a conservative manner.

12.12 HIGH VOLTAGE dc (HVDC) TRANSMISSION

It has been shown in Section 12.7, that dc transmission requires much less conductors than ac three-phase transmission. However, dc transmission was not possible, as high voltage needed high power transmission, which has not been possible since large power could not be generated. Further, it has not been possible to transfer the level of dc volts. However, dc transmission became operational as early as 1954 with the

development of power switching devices. After the advent of high-current, high-voltage solid-state switching devices (thyristor), several HVDC lines have been constructed in the world for transmitting dc power in thousands of MWs. Such HVDC lines are embedded in an overall ac transmission and are connected to the rest of the system for power exchanging through transformers and converters.

Apart from three back-to-back HVDC stations already in operation in India, HVDC lines from Chandrapur to Padghe have been commissioned in 1999. The rating of this system is 1500 MW, ±500 kV bipolar with a length of 754 km.

Principle of ac/dc Conversion

HVDC transmission consists of two converters, which are connected to each other by a dc cable or an overhead dc line. A typical arrangement of main components of an HVDC transmission is shown in Fig. 12.21.

Two series connected 6-pluse converters (12-pulse bridge) consisting of thyristor valves and converter transformers are used. The valves convert ac to dc, and the transformer provides a suitable voltage ratio to achieve the desired direct voltage and galvanic separation of the ac and dc systems. A smoothing reactor in the dc circuit reduces the harmonic currents in the dc line, and the possible transient overcurrents.

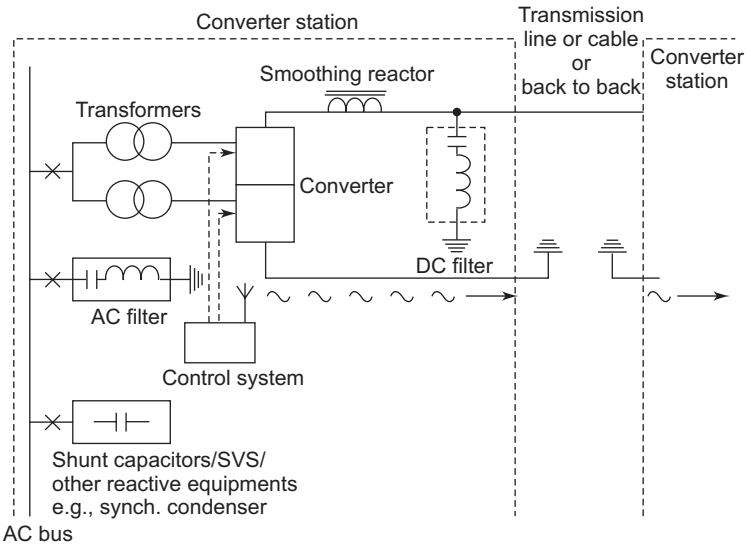


Fig. 12.21 *Main components of a HVDC transmission—a typical arrangement*

Filters are used to take care of harmonics generated at the conversion. Thus, we see that in an HVDC transmission, power is taken from one point in an ac network, where it is converted to dc in a converter station (rectifier), transmitted to another converter station (inverter) via line or a cable and injected into an ac system.

Economics of dc Transmission

The cost of terminal equipment is much more in case of dc (converting stations) than in case of ac (transformer/substations). If we plot the variation of cost of power as a function of transmission distance, it will be as shown in Fig. 12.22. The slope gives the cost per unit length of the line and other accessories. The point of intersection *P* is called a breakeven point, which shows that if the transmission distance is more than *OP*, it is preferable to use dc; otherwise ac should be used.

There is hardly any scope to reduce the cost of ac terminal equipment. But, a lot of progress has been made in the development of converting devices, and the breakeven distances are reducing with further development of these devices.

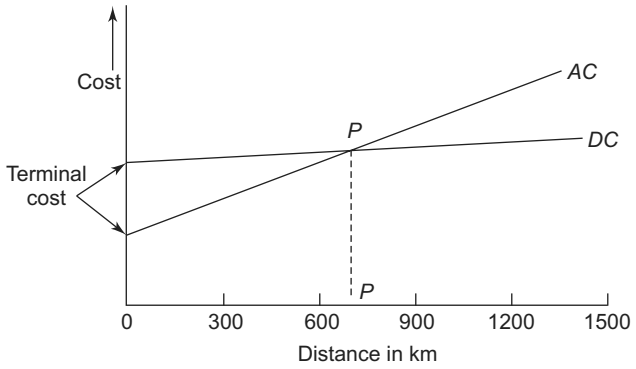


Fig. 12.22 *Variation of power cost w.r.t. distance*

Present-day breakeven distance in favour of dc transmission is 700 km for overhead lines. However, the breakeven distance varies with each individual project and should always be checked.

Advantages of HVDC Systems

The advantages of the HVDC systems are as follows:

(a) These systems are economical for long-distance bulk power transmission by overhead lines.
(b) There is greater power per conductor and simpler line construction.
(c) Ground return is possible.
(d) There is no charging current.
(e) The voltage-regulation problem is much less serious for dc, since only the IR drop is involved ($X_L = 0$).
(f) There is easy reversibility and controllability of power flow through a dc link.
(g) There is considerable insulation economy. The peak voltage of the 400 kV ac line is $\sqrt{2} \times 400 = 564$ kV. So the ac line requires more insulation between the tower and conductors, as well as greater clearance above the earth as compared to corresponding 400 kV dc line.
(h) Smaller amount of right of way is required. The distance between two outside conductors of a 400 kV ac line is normally 20 m, whereas the same between a corresponding dc line is roughly half, i.e. 10 m only.
(i) Line losses are smaller.

Disadvantages of HVDC Systems

(a) The systems are costly since installation of complicated converters and dc switchgear is expensive.
(b) Harmonics are generated which require filters.
(c) Converters do not have overload capability.
(d) Lack of HVDC circuit breakers hampers network operation. There is no dc device, which can perform excellent switching operations and ensure protection.
(e) There is nothing like a dc transformer, which can change the voltage level in a simple way. Voltage transformation has to be provided on the ac sides of the system.

Further, power system would include a transmission mix of ac and dc. Future controllers would be more and more microprocessor based, which can be modified or upgraded without requiring hardware changes,

and without bringing the entire system down. While one controller is in action, the duplicate controller is there as a 'hot standby' in case of a sudden need

It is by now clear that HVDC transmission is already a reliable, efficient and cost-effective alternative to HVAC for many applications. Currently, a great deal of effort is being devoted to further research and development in solid-state technology.

12.13 CABLES

In big cities and densely populated areas, overhead lines become impractical owing to safety regulations. In such places, insulated conductors are usually laid underground, and are called cables. Underground transmission and distribution is no doubt more expensive than the overhead alternative. Cables developed should be not only economically attractive, but physically they should be able to carry large chunks of power. The main constraint is the temperature rise of the insulating material used, the limit of conductor temperature being 90°C. For flexible cables, there exists an upper limit to overall diameter, and hence to the size of the conductor. The combination of paper and oil is still the most effective dielectric for HV cables. Cable installations are useful for submarine, crossings, railway yards, inside power stations and in densely populated areas. Underground cables also provide greater safety, less interference with amenities and better outlook.

12.14 TYPES OF CABLES

Many types of cables are used depending upon the mechanical properties required, the transmission voltage range, and the type of insulation used. The insulating material used for cables should have good insulation resistance and high dielectric strength. It should be nonhygroscopic and should not react with acids and alkalies. The maximum current rating of a cable varies with the cable size, the insulation used, earth thermal resistivity and the method of laying the cable in the ground.

For LV (below 1 kV) applications, plastic cables are used. Aluminium is increasingly being used as both a conductor and sheath material. At lower voltages, oil-impregnated, paper-insulated cables are used mostly with the three conductors contained in a single sheath. Such a cable is called *belted-type cable* (Fig. 12.23). For mechanical protection, steel armouring is employed. Jute is used for covering the cables. The tangential stresses are completely eliminated in case of the shielded construction.

For up to 11 kV HV systems, paper-insulated cables are used, whereas for a 33 kV system, H-type (designed by M Hochstadter) cables are preferable. In 'SL' type cables, each core has its own lead sheath, with an additional lead sheath enclosing the three cores. In HSL type cables, there is a perforated screen, and a separate lead sheath is used for each core. For HV cables for 66 kV and more, single-core cables are used, since three-core cables would otherwise be too thick to bend.

For 220 kV (and higher) cables, it is necessary to avoid cable ionisation by preventing the void formation. Voids are formed by cyclic heating and cooling of the impregnant. Void formation can be prevented by the use of a very thin film of oil under pressure. Such pressurised cables are known as oil-filled cables. In this type, a hollow conductor of soft-drawn stranded copper, fed by oil reservoirs placed at intervals along the line, is used. The oil is maintained under pressure by these reservoirs. As the cable heats on load, oil is driven from the cable into the reservoirs and vice versa, hence the formation of voids is prevented. Impregnated paper is used for insulation, and a lead sheath and jute covering are employed to give waterproofing. Figure 12.24 depicts a cross section of a 220 kV oil-filled cable. Oil-filled cables require relatively smaller amount of insulation as compared to the solid type for the same operating voltage, and therefore, are used for higher voltages (66 kV–400 kV). At 500 kV, the oil-filled cable has a working stress of 15 kV/mm.

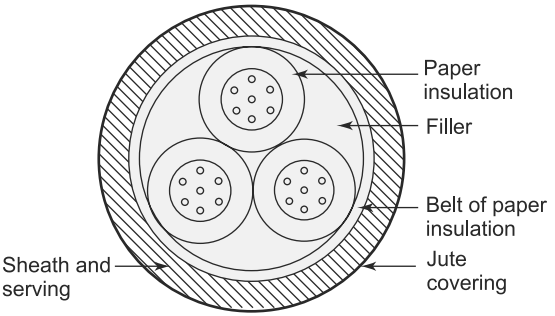


Fig. 12.23 *A three-core belted type cable*

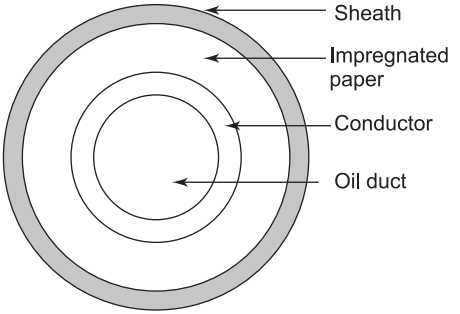


Fig. 12.24 *Oil-filled cable*

To counter the disadvantages of oil-filled cables in terms of expansion and contraction of oil during loading cycles, gas-filled cables are used. A gas-filled cable consists of a conductor supported in a rigid external pipe filled with a pressurised gas (usually SF_6 or nitrogen or air) at 3 atm pressure. The pressure makes the voids small by compression and reduces ionisation. Because of the good thermal characteristic and high dielectric strength of SF_6, it is preferred for insulating cables.

Gas-pressure cables are mainly of two types, namely impregnated gas-pressure cables and gas-filled cables. A three-in-one earthed enclosure, filled with SF_6 gas is less costly as compared to the rigid isolated phase construction. Disc-type spacers [Fig. 12.25(a)] or column-type spacers [Fig. 12.25(b)] may be used. A rigid tripolar compressed-gas-insulated (C.G.I.) cables are shown in Fig. 12.25 (a) and (b). Gas is maintained at a pressure of about 1.38 MN/m^2.

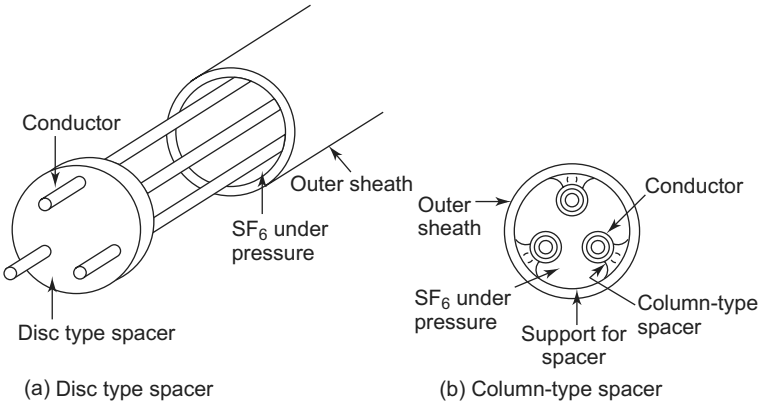


Fig. 12.25 *Rigid tripolar CGI cables*

A flexible CGI cable has the advantages of a flexible form of a spacer cable. Another development, which is promising, is the use of two or more subconductors per phase. Development of a cable with lapped polyethylene pressurised with SF_6 has also been reported.

One advantage of the gas-filled cable is its better head dissipation by natural convection in the gas. More revolutionary are the cables incorporating cryogenic coolants. An alternative to the superconducting cable is the resistive operation of an Al or Cu conductor at *cryogenic* temperatures. Such a cable is called *cryoresistive*.

Oil-filled and gas-filled cables are used in the range of 132 kV to 500 kV. SF_6 filled cables can be used for transporting thousands of MVA even at UHV whereas conventional cables are confined to 1000 MVA and 500 kVA.

12.14.1 XLPE Cables (Cross-Linked Polythene Cables)

Low-density polythene, when vulcanised under controlled conditions, results in cross linking of carbon atoms and produces cross-linked polythene. This new material has extremely high melting point with light weight, small dimension, low dielectric constant and high mechanical strength.

XLPE cable has high maximum continuous temperature rating of 90°C with dielectric strength of 20 kV/cm. Due to high temperature-withstand capability and very low moisture absorption, these cables can be directly laid on soil bed and are suitable upto 33 kV.

12.14.2 Cables for HVDC Transmission

Due to absence of periodic charging current in HVDC system, cables play an effective role in dc transmission links. The dielectric loss is also low. There is no limitation of distance of transmission as there is no periodic charging current.

Summary

- High voltage is essential for transmission of large power in order to reduce the conductor cost and bring the efficiency to acceptable levels. *Of all possible power transmission methods, the most economical is dc 2-wire followed by ac 3-phase, 3-wire.*
- The ac transmission is universal because of generating power at high voltage and the facility of step-up and step-down of voltage levels. This is not possible in dc transmission.
- Economy of HVDC transmission becomes visible for transmitting large power over long distances (700 km and above). Devoted lines are used for HVDC embedded in large interconnected ac power networks.
- For improving the efficiency of power-transmission lines, the receiving-end load power factor must be high.
- Most power loads have a lagging power factor, which can be improved by shunt capacitors which supply positive VARs.
- The value of capacitor bank to provide Q_C VARs is

  $$C = \frac{Q_C}{\omega V^2} \text{ Per phase basic}$$

- At light load the receiving-end voltage becomes high. The corrective measure is to switch in inductor bank to feed negative VARs.
- In place of capacitor and inductor banks synchronous condenser (synchronous motor at low-load) can be employed. When over-excited, it feeds positive VARs to the line and upon under-exciting, it feeds negative VARs. Installation is expensive needs regular maintenance.
- To provide security and reliability of power supply and for power sharing, large power networks are interconnected through transmission forming a grid.

Exercises

Review Questions

1. List the merits and demerits of having high transmission line voltage.
2. Tabulate the current, voltage and line losses in various transmission system types.
3. Study the effects of poor power factor and compare the power-factor correction methods.
4. Brief the effect of reactive power flow on transmission-line voltage.
5. When and where are underground cables used?

Multiple-Choice Questions

1. Which type of system is used for transmitting large amounts of power over long distance
   (a) dc 2-wire, mid-point earthed
   (b) 3-wire, 3-phase
   (c) 4-wire, 3-phase, one is neutral
   (d) single-phase, 2-wire, mid-point earthed
2. Efficiency of transmission increases with
   (a) increase of supply voltage and power factor
   (b) increase of supply voltage but decrease of power factor
   (c) decrease of supply voltage but increase of power factor
   (d) decrease of supply voltage and power factor
3. Low power factor
   (a) increases both capital and running cost
   (b) increases capital cost but decrease running cost
   (c) decreases capital cost but increase running cost
   (d) decreases both capital and running cost
4. In a short transmission line,
   (a) shunt capacitance is ignored
   (b) line resistance and shunt capacitance cannot be ignored
   (c) line resistance is considered but shunt capacitance is ignored
   (d) line resistance is ignored but shunt capacitance is considered
5. Disadvantages of HVDC systems are
   (a) the system is costly due to installation of converters
   (b) harmonics are generated which requires filters.
   (c) converters do not have overload capability
   (d) all of the above
6. For which voltage level are plastic cables used?
   (a) Below 1 kV
   (b) 1 kV–2 kV
   (c) 5 kV – 11 kV
   (d) None of these
7. XLPE has
   (a) high melting point with light weight
   (b) low melting point with light weight
   (c) low melting point with low dielectric cost
   (d) melting point with high dielectric cost
8. The power loss in the line per phase is where symbol have these usual meanings
   (a) $P_L = \dfrac{JSLP}{V\cos\phi}$
   (c) $P_L = \dfrac{JLP\cos\phi}{VS}$

(b) $P_L = \dfrac{JLP}{VS\cos\phi}$ (d) $P_L = \dfrac{LP\cos\phi}{JVS}$

(9) Range of ultra high voltage is
(a) greater than 700 kV (b) 500–600 kV
(c) 400–500 kV (d) 600–700 kV

10. Which one of the following is not true regarding HVDC transmission?
(a) Corana loss is much more in HVDC transmission.
(b) The lower transmission capability of binder line is almost the same as that of single-circuit ac line.
(c) HVDC line can operate between two ac system whose frequencies need not be equal.
(d) There is no distance limitation for HVDC transmission by underground cable.

Answers

Multiple-Choice Questions

1. (a) 2. (a) 3. (a) 4. (a) 5. (d)
6. (a) 7. (a) 8. (a) 9. (a) 10. (a)

Semiconductors

chapter 13

Goals & Objectives

- Introduction to semiconductors and insulators
- Conduction in solids and metals
- Explanation of doped semiconductors
- Definition of diffusion

13.1 CONDUCTION IN SOLIDS

Solid materials, from the point of view of current carrying capability are of three types—*conductors*, *insulators* and *semiconductors*. Conductors have an abundance of free electrons, which act as the charge carriers, which means that they have high conductivity. Insulators, on the other hand, have hardly any free electrons and therefore practically cannot conduct any current, i.e. these are poor conductors. Semiconductors, as such, have conductivity intermediate between conductors and insulators and have the special feature of having two types of charge carriers—electrons and holes (which are absence of electrons in covalent bonds and act equivalently as positive charge carriers). Further, semiconductors have the peculiar property such that by doping with certain elements, their conductivity gets increased by several orders of magnitude (up to about six). It is this property, in fact, which is exploited in constructing electronic devices and integrated circuits from semiconductor materials.

13.1.1 Conduction in Metals

Typically, in metals (copper, aluminium, silver, etc.), atoms are arranged in systematic array in the form of crystals. The electrons of the outer orbit of metal atoms being loosely bound to the nuclei get detached and become free because of attractions from neighbouring nuclei. The metal crystal thus exists in the form of a lattice of positive ions with fixed (but vibrating) locations surrounded by randomly moving free electrons such that any macrosize metal piece acts electrically neutral as shown in Fig. 13.1. Electrons move about rapidly and randomly (in Brownian motion) losing kinetic energy upon elastic collision with positive ions and gaining energy (accelerating) between collisions because of attractive forces of adjoining ions with net zero movement as shown in Fig.13.2(a).

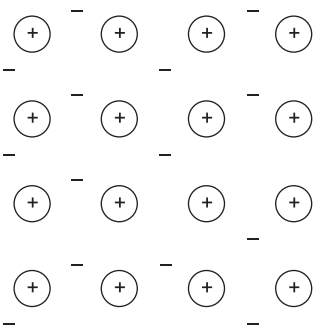


Fig. 13.1 *Two-dimensional representation of a metal crystal*

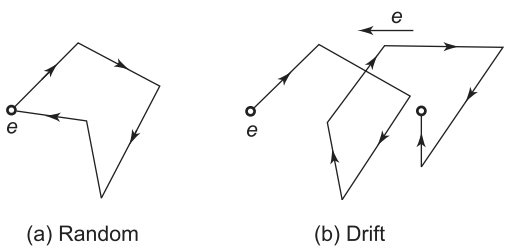


Fig. 13.2 *Electron motion in a metal crystal*

Upon application of uniform electric field ε (V/m), electrons while still moving rapidly and randomly, acquire a net (average) component of velocity in opposite direction to that of the field as shown in Fig. 13.2(b). This directed average velocity is known as *drift velocity* u_d and is proportional to ε.

Thus,

$$u_d = \mu(-\varepsilon) \text{ m/s; electrons drift in direction opposite to the electric field} \quad (13.1)$$

where μ = *mobility* (m/s per V/m or m^2/V.s) which is a property of the material and decreases with temperature (with faster vibration of ions in the lattice, chances for collision of electrons with these increase).

The drift of electrons carrying charge $-q$ constitutes electric current. If there are n free electrons/m^3, the current density J(A/m^2) is

$$J = n(-q)u_d = n-q\ \mu\ -\varepsilon = \sigma\varepsilon \quad (13.2)$$

where $\sigma = nq\mu$ = conductivity of the material in siemens/m. The reciprocal of conductivity is called resistivity in ohm-m.

It is observed that the conductivity of a material is directly proportional to n, the number of free electrons/unit volume (m^3). For conductors like copper and silver, n is very large ($\approx 10^{28}$) and so these have high conductivity, whereas for insulators like wood, plastic, etc., n is small ($\approx 10^7$) because these materials have a *forbidden energy gap* so wide that few electrons cross it at room temperature.

13.1.2 Semiconductors

Semiconductors differ from conductors and insulators. They have two types of mobile charge carriers. Two of the most important semiconductors are silicon and germanium, which belong to the fourth column of the periodic table. It means that these have four valence electrons in the outer orbit (tetravalent). The crystalline structure of both silicon and germanium is the tetrahedral pattern as shown in Fig. 13.3(a), wherein each atom shares four of its valence electrons with each of the four neighbouring atoms. Such bonding is known as *covalent bonding* and can be represented schematically in two dimensions as shown in Fig. 13.3(b). At zero temperature (K), all the valence electrons are tightly bound to the nuclei and there are no free charge carriers, i.e. the material behaves as an insulator.

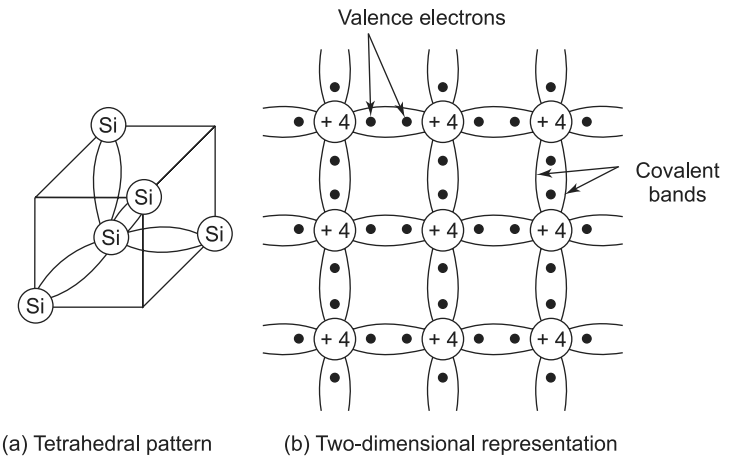


Fig. 13.3 *Arrangement of atoms in a silicon crystal*

The energy required to break a covalent bond is about 14.1 eV for silicon and about 0.7 eV for germanium at room temperature (about 300 K). Figure 13.4 shows the energy band diagram of silicon from which it is seen that a valence electron must acquire quantum energy jump of well above 14.1 eV to cross over to the conduction band.

*eV (electron-volt) is unit of energy when an electron moves through 1 volt.

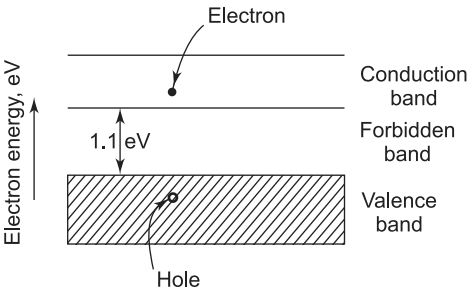


Fig. 13.4 *Energy-band structure of silicon*

At room temperature a few electrons have sufficient thermal energy to break the covalent bonds becoming free, leaving behind a vacancy with a net positive charge in the region, while the region surrounding the free electron has a negative charge. This is pictorially represented in Fig. 13.5, which shows one free electron, one missing covalent electron with effective positive charge called, the *hole*. Figure 13.5 also shows an electron, which has moved over to conduction band leaving behind a hole. The holes have larger effective mass than electrons.

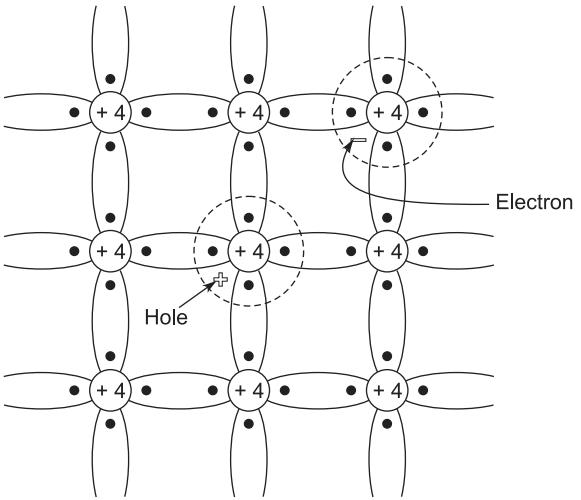


Fig. 13.5 *Silicon crystal with one covalent bond broken*

An electron released from a covalent bond leaves behind a hole and it may fill the hole vacancy in a neighbouring bond which is equivalent to the movement of the hole from one position to another. In other words, the hole has moved to the position vacated by the electron from that of the earlier vacant bond, which is now occupied by the electron. Thus, both electrons and holes act as charge carriers in semiconductors as different from the conduction in metals (only free electrons are the charge carriers). It must be observed here that where holes are involved, current flow always occurs because of movement of electrons but the effect is that of a hole moving in the opposite direction.

When electric field ε is applied to the semiconductor material, electrons drift in opposite direction to ε while holes drift in the direction of ε both adding to a current in the positive direction. Equation (13.2) for current density now generalises for a semiconductor as

$$J = (n\mu_n + p\mu_p)q\varepsilon \text{ A/m}^2 \tag{13.3a}$$

and conductivity

$$\sigma = (n\mu_n + p\mu_p)q \text{ S/m} \tag{13.3b}$$

where μ_n = electron mobility,
μ_p = hole mobility; the hole mobility being much lower than the electron mobility, and
n, p = number of electrons or holes/unit vol (m^3).

In a pure sample of a semiconductor material, electron-hole pairs are simultaneously generated so that

$$n = p = n_i = \text{number of electrons or holes/m}^3$$

Such a semiconductor is called *intrinsic semiconductor*. Constantly new electron-hole pairs are being generated and older ones are recombining (electron is captured by a hole and the pair vanishes). At room temperature the density of free electron-hole pair (n_i) is not very high, i.e. only a small fraction of valence electrons are in free state (about 1 in every 10^{12} atoms).

Some of the properties of Si and Ge are given in Table 13.1.

Table 13.1 *Properties of silicon and germanium at room temperature (300 K)*

Properties	*Silicon*	*Germanium*
Atomic number	14	32
Density (g/m^3)	2.33×10^6	5.32×10^6
Energy gap (eV)	14.12	0.67
Intrinsic carrier density, n_i ($/m^3$)	14.5×10^{16}	2.4×10^{19}
Intrinsic resistivity (Ω-m)	2300	0.46
Electron mobility (m^2/V.s)	0.135	0.39
Hole mobility (m^2/V.s)	0.048	0.19

* Ref: "Properties of Silicon and Germanium II" Proc. IRE, June 1958, p. 1281.

Example 13.1

Estimate the relative concentration of germanium atoms and electron-hole pairs at 300 K (room temperature). Also, predict the intrinsic resistivity. Given atomic weight of germanium, 72.60 g/g-atom; $q = 14.6 \times 10^{-19}$ coulombs.

Solution Using figures for germanium from Table 13.1,

$$\text{Density} = 5.32 \times 10^6 \text{ g/m}^3$$

$$n_A = \frac{6.022 \times 10^{23} \text{ atoms/g-atom} \times 5.32 \times 10^6 \text{ g/m}^3}{72.60 \text{ g/g-atom}}$$

$$= 4.41 \times 1028 \text{ atom/m}^3$$

Intrinsic concentration n_i (at 300 K) = 2.4×10^{19} electron-hole pairs/m^3 (see Table 13.1). $n_A/n_i = 4.41 \times 10^{28}/2.4 \times 10^{19} = 14.84 \times 10^9$ germanium atoms/electron-hole pair

$$\sigma_i = (n\mu_n + p\mu_p)q = (\mu_n + \mu_p)n_i q$$
$$= (0.39 + 0.19) \times 2.4 \times 10^{19} \times 14.6 \times 10^{-19}$$
$$= 2.227 \text{ S/m}$$

Intrinsic resistivity, $\rho_i = 1/\sigma_i = 1/2.227 = 0.449$ Ω-m

13.2 DOPED SEMICONDUCTORS

When pentavalent/trivalent impurity atoms are introduced into the crystalline structure of a semiconductor (Si or Ge), there is tremendous increase in the concentration of free electrons/holes with a corresponding enhancement in conductivity of the material which is then known as *doped* or extrinsic semiconductor. *Pentavalent* elements commonly used are nitrogen, phosphorus, arsenic and antimony, while the *trivalent* elements are boron, aluminium, gallium and indium.

Consider the introduction of a small amount of pentavalent (impurity atoms) in the crystal structure of silicon as shown in Fig. 13.6(a). The pentavalent atom has five valence electrons, only four of which participate in the covalent bonding with neighbouring silicon atoms. The fifth electron becomes a free electron leaving behind a positively charged but immobile ion, which cannot take part in the conduction process. This type of impurity is called *donor* or *N-type impurity* as it contributes free electrons from the donor atoms. Of course, the material as a whole is neutral.

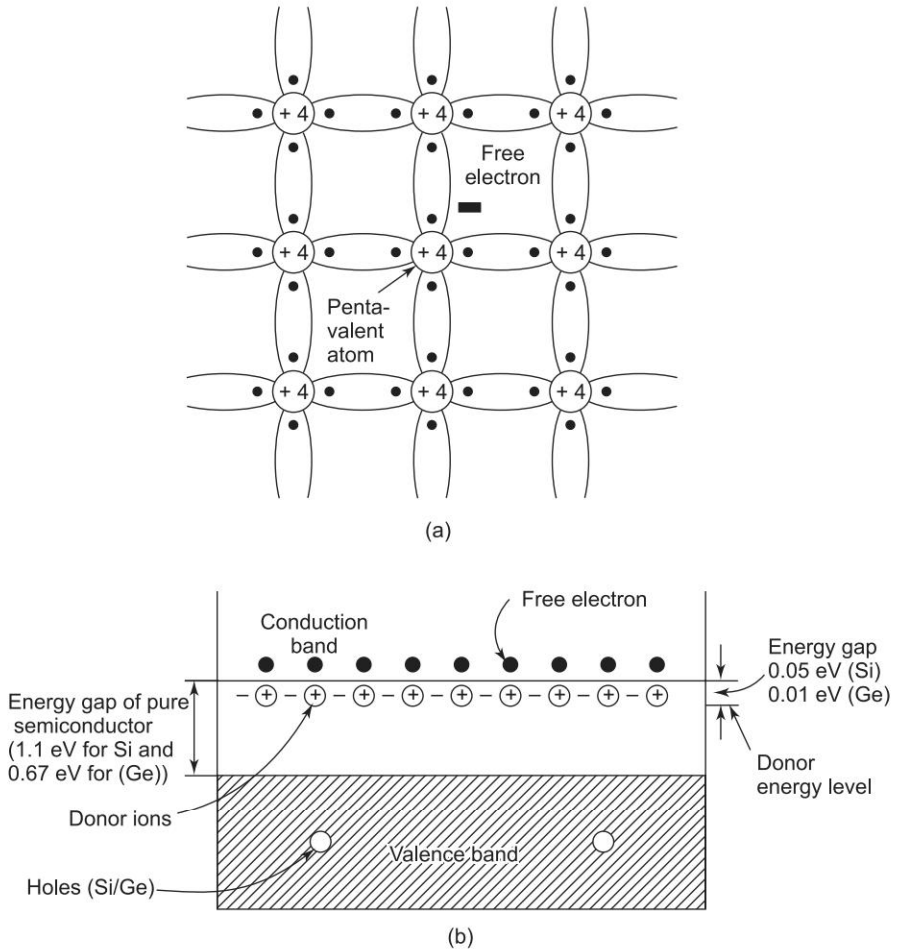


Fig. 13.6 *(a) Effect of n-type doping (b) Effect of donor impurity on energy-band structure of semiconductor*

The effect of donor impurity on energy-band structure of semiconductors is illustrated in Fig. 13.6(b). It is seen that the energy gap of donor atoms is significantly smaller than that of the intrinsic material. As a consequence, the fifth valence electrons from almost all the donor atoms become free above 300 K. At room temperature in intrinsic silicon there is about one free electron for every 10^{12} atoms (1 for 10^9 Ge atoms). If doping level is 1 donor atom in 10 million (10^7) silicon atoms, the free electrons in doped material rise by ($10^{12}/10^7 = 10^5$) times compared to the intrinsic material. Thus, there is great preponderance of electrons over holes in the extrinsic material with donor impurity atoms; the material being called *N*-type wherein electrons are the *majority charge carriers* and holes are the *minority charge carriers*.

Consider now the introduction of trivalent (impurity) atom into the silicon crystal as illustrated in Fig. 13.7(a). The three valence electrons of the trivalent atom form covalent bonds with the neighbouring silicon atoms while the fourth unfilled bond acts as a hole as it can accept an electron. Such impurity is called an *acceptor* or *P-type* impurity as it leads to generation of holes in the extrinsic material. As one such hole accepts an electron, the impurity atom behaves as a negatively charged immobile ion.

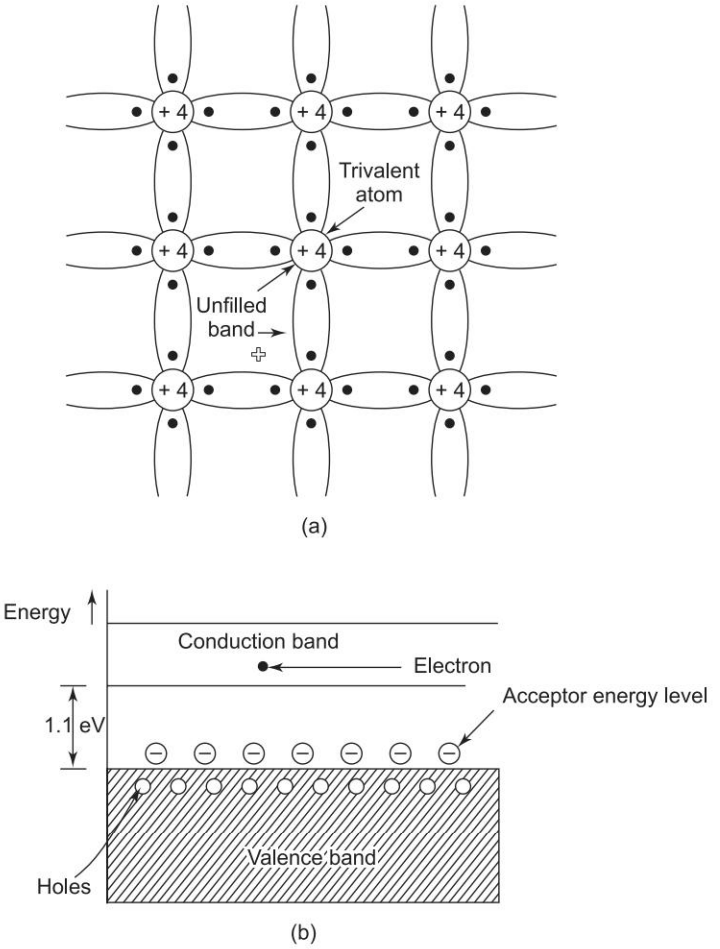


Fig. 13.7 *(a) Effect of p-type doping (b) Effect of acceptor impurity on energy-band structure of semiconductor*

Figure 13.7(b) shows the band structure of acceptor type (*P*-type) extrinsic material. In this also we find nearly as many extra holes as the number of acceptor atoms appear in the *P*-type material. Thus, in a *P*-type material, holes are the *majority carriers* and electrons are the *minority carriers*.

As an electron meets a hole, it is captured and the pair vanishes; the process is called *recombination*. The rate of recombination, R (electron-hole pairs/s. m^3) is proportional to all possible meetings of electron holes, i.e. np. Thus,

$$R = rnp;\ r = \text{constant}$$

Under thermal equilibrium conditions, the rate of generation equals the rate of recombination, i.e. $R = g$.

For intrinsic material,

$$g_i = R_i = rn_ip_i = rn_i^2 \text{ (as } p_i = n_i)$$

So long as the number of impurities atoms (donor/acceptor) in doping a semiconductor are small (1 in 10 million is a typical figure), thermal generation in extrinsic semiconductor is the same as intrinsic semiconductor or

$$g = g_i = rn_i^2$$

In equilibrium of extrinsic semiconductor,

$$g = R$$

or $$rn_i^2 = rnp$$

or $$np = n_i^2 \tag{13.4}$$

where n, p = carrier concentrations in extrinsic semiconductor.

This relationship is known as *mass-action law*.

According to Eq. (13.4), as the concentration of one type of carrier is increased by doping, the concentration of the other type of carrier goes down below the intrinsic value.

In normal doping, the concentration of donor/acceptor atoms is such that

$$N_d >> n_i \text{ or } N_a >> n_i$$

where N_d and N_a are concentrations of donor and acceptor atoms respectively.

$$n_n \approx N_d$$

It immediately follows that the conductivity of extrinsic material is determined mainly by the doping concentration.

Diffusion

All particles in random motion, because of their thermal energies, move from the region of high concentration to that of low concentration. It is because across any imaginary plane, the random motion of particles causes more particles per unit time to cross from the high to low concentration side compared to those crossing from the low to high side. This phenomenon is known as diffusion and is statistical in nature. It is easily observed in everyday life, for example, in the spread of fragrance upon opening a bottle of perfume. It may be noted that this movement is not on account of any external force acting on particles as in the case of drift or any repulsive forces among them but is purely due to random thermal motion of the particles and is related to the concentration gradient.

The phenomenon of the diffusion of electrons and holes in the semiconductors happens in a similar way and constitutes a flow of current known as the *diffusion current*. This current is proportional to the concentration gradient of electrons/holes and is in the direction opposite to that of the positive gradient q (particles flow down the gradient). For electron diffusion, current density can be expressed as

$$J = (-q)D_n(-dn/dx)$$

$$= qD_n dn/dx \tag{13.5a}$$

where D_n = diffusion constant of electrons (m^2/s) and dn/dx = concentration gradient of electrons with reference to the linear dimension in units of electrons/m^3/m.

It is assumed here that electrons are constrained by the geometrical configuration of the semiconductor so as to move in a linear dimension. Similarly, for hole diffusion current density

$$J = qD(-dp/dx)$$
$$= -qD(dp/dx) \quad (13.5b)$$

where D_n = diffusion constant of holes (m^2/s), and dp/dx = concentration gradient of holes with reference to the linear dimension x in units of electrons/m^3/m.

As mobility and diffusion are both statistical phenomena, it is not surprising that they obey the *Einstein equation*

$$\mu_n/D_n = \mu_p/D_p = q/kT \quad (13.6)$$

Summary

➢ Semiconductors are discussed in this chapter. They are useful in understanding electronic devices and integrated circuits.

Exercises

Review Questions

1. Define electric field intensity, potential energy, electron-volt, mobility and conductivity.
2. Distinguish between intensive and extrinsic semiconductors.
3. What is a hole and how does it contribute to conduction?
4. Show the two-dimensional picture of a silicon crystal containing: (a) donor impurity atoms, and (b) acceptor impurity atoms.
5. What type of semiconductor results when doped with (a) donor and (b) acceptor impurities?
6. State the law of mass action.
7. A semiconductor has donor and acceptor concentrations of N_D and N_A respectively. How will you determine the concentration of electrons n and holes p in each type of extrinsic semiconductor?
8. What is meant by recombination?
9. What is meant by diffusion of charge carriers? How is it different from drift? Are the two related? If so, how?
10. Does the resistivity of extrinsic semiconductor increase or decrease with temperature?

Problems

1. A Si bar is doped with 10^{17} boron atoms/cm^3. What is the electron concentration at 300 K? What is the resistivity?
   Given: $n_i = 14.5 \times 10^{10}/cm^3$, $\mu_n = 1350\ cm^2/V.s$, $\mu_p = 480\ cm^2/V.s$
2. A silicon bar, 0.1 cm long and 100 μm^2 in cross-sectional area, is doped with $10^{17}/cm^3$ antimony (*V*th gp.). Find the current at 300 K with 10 V applied. Repeat for 1 in long Si bar.
3. Phosphorous donor atoms with a concentration of $10^{16}/cm^3$ are added to a pure sample of silicon. Assume that the phosphorus atoms are distributed homogeneously throughout the silicon sample. What is the sample resistivity at 300 K?
4. An *N*-type sample of silicon has a uniform density of $N_d = 10^{16}$ atoms/cm^3 of arsenic and a *P*-type silicon sample has $N_a = 10^{15}$ atoms/cm^3 of boron. For each of the semiconductor materials, determine the equilibrium minority carrier concentration at 300 K.

5. The electron concentration in a piece of uniformly and lightly doped *N*-type silicon at room temperature varies linearly from $10^{17}/cm^3$ at $x = 0$ to $6 \times 10^{16}/cm^3$ at $x = 2$ cm. Electrons are supplied to keep this concentration constant with time. Calculate the current density in the silicon, if no electric field is present. Given: Diffusion constant = 35 cm^2/s (*Hint*: Use electron diffusion current density relation).

Multiple-Choice Questions

1. For silicon, the energy gap at 300 K is
   (a) 1.1 J (b) 1.1 eV (c) 1.1 F (d) all of these
2. *N*-Type semiconductors contains
   (a) trivalent impurity (b) tetravalent impurity
   (c) divalent impurity (d) pentevalent impurity
3. Energy gap for germanium at room temperature:
   (a) 0.67 eV (b) 0.12 eV (c) 1.1 eV (d) none of these
4. The electric charge on a hole is
   (a) 1.6×10^{8}C (b) 1.6×10^{-19}C
   (c) 1.6×10^{-11} (d) 1.6×10^{-12}
5. Hall-effects occurs only in
   (a) *P*-type semiconductor (b) *N*-type semiconductor
   (c) Metal (d) all of these
6. Energy gap for GaAS at room temperature is
   (a) 0.67 eV (b) 14.1 eV (c) 14.43 eV (d) 0.12 eV
7. The thermal voltage equation in diode is
   (a) $V_T = \frac{kT}{q}$ (b) $V_T = q\,k\,T$ (c) $V_T = \frac{q}{kT}$ (d) $V = \frac{k}{qT}$
8. The process of adding impurities to a pure semiconductor is called
   (a) doping (b) mixing (c) diffusing (d) filtering
9. The value of Boltzmann's constant *k* is
   (a) 1.38×10^{-24} J/K (b) 1.39×10^{-23} J/K
   (c) 1.38×10^{-23} J/K (d) 1.39×10^{23} J/K
10. The mobility of electrons in a material is expressed in units of
    (a) V/s^2 (b) m^2/s (c) J/K (d) $m^2/V\text{-}s$

Answers

Problems

1 2250/cm^3, 0.13 cm
2 2.16 mA, 2.16 A
3 0.463 cm
4 22500/cm^3, 225000/cm^3
5 1120 A/cm^2, in negative *x*-direction

Multiple-Choice Questions

1. (b) 2. (d) 3. (a) 4. (b) 5. (b)
6. (c) 7. (a) 8. (a) 9. (c) 10. (d)

Diodes and Applications

chapter 14

Goals & Objectives

- Discussion of various types of diodes
- Description of *PN*-junction diode and zener diode
- Types of rectifiers—half wave, full wave and bridge rectifier
- Rectifier with centre tapped (CT) transformer
- Different types of wave shaping
- Explanation of special purpose diodes—Schottky, barrier and photodiode

14.1 INTRODUCTION

A diode is a two-layer (*PN*) device which facilitates conduction in one direction and stops conduction in the other direction. It has a wide range of applications like rectification (converting ac to dc), voltage regulation, protection against high voltage and wave shaping. Then there are special purpose diodes, e.g. zener diode, light-emitting diode and several others.

14.2 *PN*-JUNCTION DIODE

As thin layers of *P*- and *N*-type semiconductors are joined to form a junction, as shown in Fig. 14.1, a certain phenomenon takes place immediately.

- The majority holes form *P*-side diffuse into *N*-side and vice versa.
- Recombination of electrons and holes in a narrow region on both sides of the junction results in uncovered fixed positive ions on *N*-side and fixed negative ions on *P*-side.
- This is the *depletion region* where no free electrons and holes are present.
- The electric field set up by the positive and negative ions prevents further flow of electrons and holes.
- The electric field causes the movement of minority carriers in opposite direction, a *drift* current.
- In steady-state, there is no net current flow across the junction.

The simplified diagram of an open-circuit *PN*-junction diode is drawn in Fig. 14.2 where V_0 = constant potential. The *P*-side terminal is called the *anode* and the *N*-side terminal is the *cathode*. The symbol of diode is shown in Fig. 14.3.

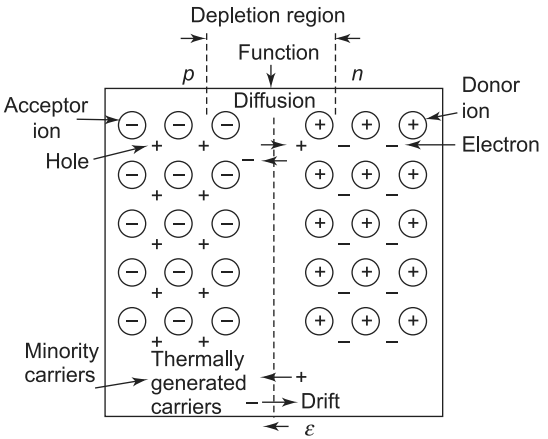


Fig. 14.1 *Phenomenon at PN-junction*

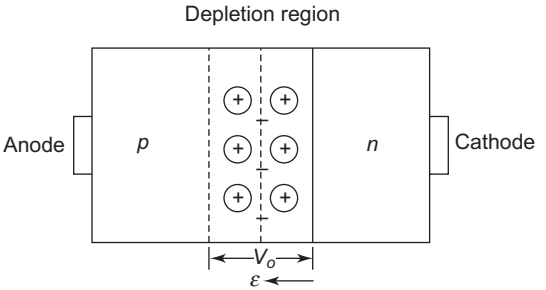


Fig. 14.2 *An open-circuited PN-junction diode*

14.2.1 Reverse Bias

The positive terminal of the battery is connected to *N*-side (cathode) and negative terminal of the battery is connected to *P*-side (anode) as shown in Fig. 14.3.

As a result of reverse biasing, the majority of holes and electrons are pulled away from the junction. This causes the width of the depletion region to increase. The majority carrier current cannot flow. However, the minority carrier drift current flows but stays at the saturation level I_s as the minority carrier concentrations

are very low. I_s is known as the *reverse saturation current*, which is almost of negligible order (nA for Si and μA for Ge).

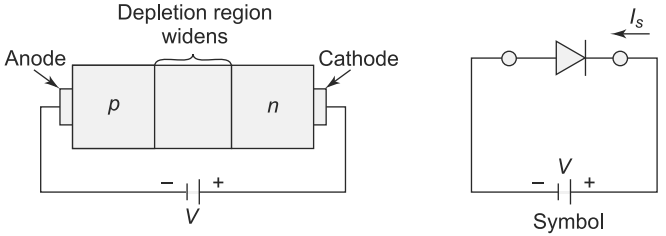


Fig. 14.3 *Reverse-biased diode*

14.2.2 Forward Bias

The positive terminal of the battery is connected to the anode (*P*-side) and negative terminal, to cathode (*N*-side). The holes from *P*-side and electrons from *N*-side get pushed towards the junction, thereby narrowing the depletion region. As a result, holes easily cross to *N*-side and electrons to *P*-side constituting the injunction current (I_i). The reverse saturation current I_s flows in the opposite direction. The net forward current $I_f = I_i - I_s$ increases sharply and is limited to a value determined by an external series resistance (load).

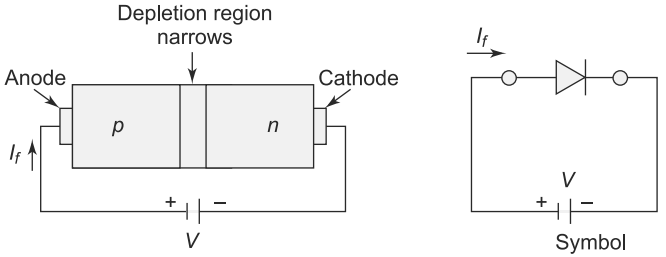


Fig. 14.4 *Forward-biased diode*

Diode Relationship

$$I_D = I_s(e^{kV_D/T_k} - 1) \tag{14.1}$$

where I_s = reverse saturation current
k = 11,600/η; η = 1 for Ge and η = 2 for Si for low current, below the knee of the curve and η = 1 for both Ge and Si for higher level of current beyond the knee (see Fig. 14.5).
$T_k = T_c + 273°$, and
T_c = operating temperature (25°C)

The plots of Eq. (14.1) for Ge and Si diodes are drawn to scale in Fig. 14.5. The sharply rising part of the curve extended downward meets the V_D axis, which is indicated as

V_T = offset, threshold or firing potential.

It is quite accurate to assume that $I_D = 0$ up to V_T and then increases almost linearly at a sharp slope. The values of V_T are

V_T = 0.7 V for Si diode
V_T = 0.3 V for Ge diode

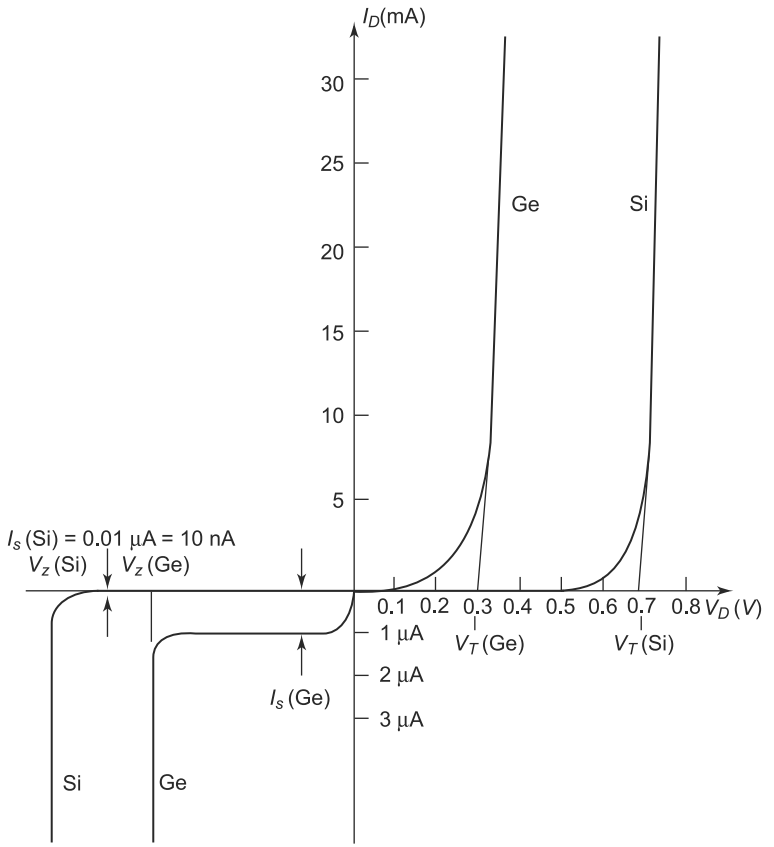


Fig. 14.5 *Diode characteristics*

Example 14.1

An Si diode has I_s = 10 nA operating at 25°C. Calculate I_D for a forward bias of 0.6 V.

Solution We take $\eta = 2$

$$T_k = 25° + 273° = 298°$$

$$k = \frac{11{,}600}{2} = 5{,}800$$

$$kV_D/T_k = \frac{5800 \times 0.6}{298} = 11.68$$

$$e^{11.68} = 117930$$

Then $$I_D = 10\,(117930 - 1) = 50 \times 0.117929 \times 10^6 \text{ nA}$$

$$= 0.586 \text{ mA, negligible.}$$

This justifies the choice of $\eta = 2$

Note: The diode is to conduct current much larger than this value.
So I_D = 0.586 mA may be approximated as zero.

❑ **Zener Region** As the reverse-bias voltage is raised, the diode breaks down at voltage V_z, by *avalanche phenomenon*. The maximum negative voltage that a diode can withstand is at Peak Inverse Voltage (PIV rating).

❑ **Zener Breakdown** By heavily doping the N and P-regions, the breakdown voltage V_z can be brought as low as –10 V, –5 V. This mechanism of breakdown is different from avalanche. This type of diode is called *zener diode*. When connected at a point in an electronic circuit, it does not allow the potential there to exceed the diode rated voltage.

14.2.3 Equivalent Circuit of Diode

Ideal Diode

It conducts when $V_D > 0$ as shown in Fig. 14.6(a).

Piecewise Linear Model

From the diode characteristic of Fig. 14.5, the piecewise linear characteristic follows and is drawn in Figs. 14.6(a), (b) and (c) along with its circuit model.

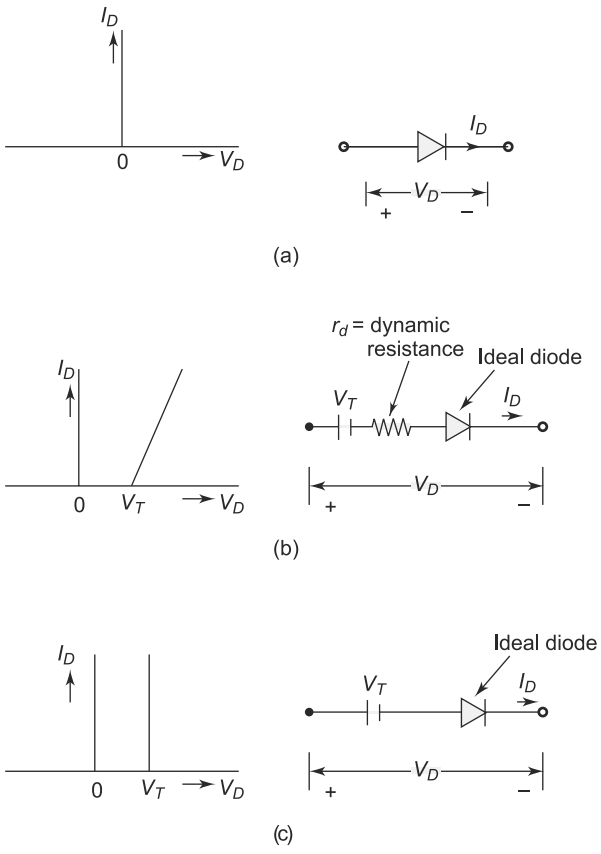


Fig. 14.6 *(a) Ideal diode (b) Piecewise linear model (c) Approximate model*

Dynamic Resistance

$$r_d = \frac{dV_D}{dI_D} \text{ (average)}$$

It can be proved that dynamic resistance on any point of the actual IV characteristic of a diode is given by

$$R_d = \frac{26 \text{ mV}}{I_D \text{(mA)}} \tag{14.2}$$

Dynamic resistance r_d is quite small, a few ohms

❑ **Approximate Model** Assuming r_d = 0, the model characteristic and circuit are drawn in Fig. 14.6(c). This equivalent circuit of diode is used most often.

Example 14.2

For the diode circuits of Fig. 14.7, find the value of *I*. Use approximate model of the diode.

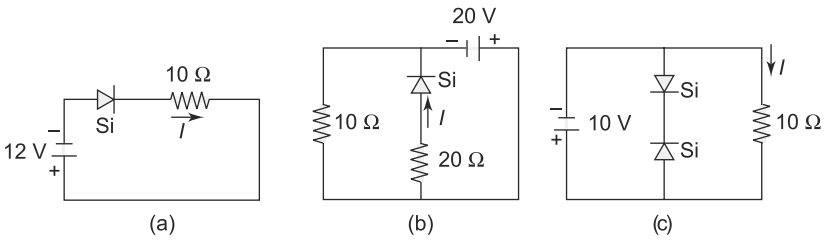


Fig. 14.7

Solution

(a) The Si diode is reverse biased by 12 V. So it does not conduct.

$$I = 0$$

(b) The voltage across diode the branch is 20 V independent of 10 Ω resistance. The diode conducts. As per equivalent circuit,

$$I = \frac{20 - 0.7}{20} = \frac{19.3}{20} = 0.965 \text{ A}$$

(c) The two diodes are in opposition and cannot conduct (open circuit).
Thus,

$$I = \frac{\Theta}{10} = -1\text{A}$$

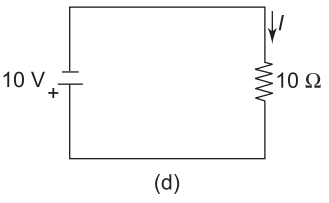


Fig. 14.7(d)

Example 14.3

For the diode circuits of Fig. 14.8, determine I_D and V_o using approximate model of the diode.

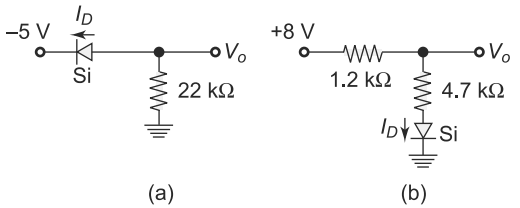


Fig. 14.8

Solution (a) The equivalent circuit is drawn in adjoining Fig. 14.9(a).

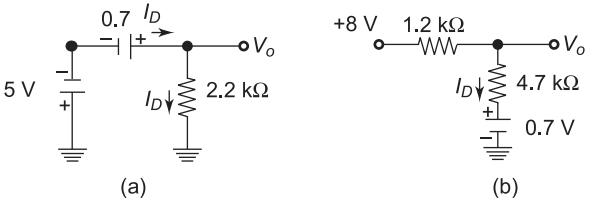


Fig. 14.9

$$I_D = \frac{5 - 0.7}{2.2} = \frac{4.3}{2.2} = 1.95 \text{ mA}$$

$$V_o = 2.2\, I_D = 2.2 \times \frac{4.3}{2.2} = 4.3 \text{ V}$$

or directly,

$$V_o = 5 - 0.7 = 4.3 \text{ V}$$

(b) The equivalent circuit is drawn in Fig. 14.9(b).

$$I_D = \frac{8 - 0.7}{1.2 + 4.7} = \frac{7.3}{5.9} = 1.237 \text{ mA}$$

$$V_o = 4.7 \times 1.237 + 0.7 = 6.51 \text{ V}$$

Example 14.4

For the diode circuits of Fig. 14.10(a), determine V_o and I_D.

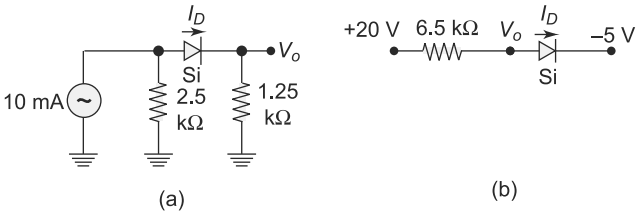


Fig. 14.10

(a) Converting current source to voltage source and diode by its circuit model, we get the circuit of the adjoining figure (Fig. 14.11).

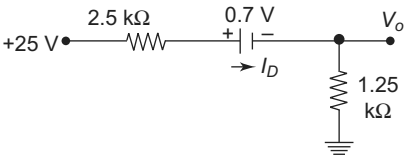


Fig. 14.11

$$I_D = \frac{25 - 0.7}{2.5 + 1.25} = 6.48 \text{ mA}$$

$$V_o = 1.25 \times 6.48 = 8.1 \text{ V}$$

(b) We can proceed directly.

$$I_D = \frac{20 - 0.7 + 5}{6.5} = 3.738 \text{ mA}$$

$$V_o = 20 - 3.738 \times 6.5 = -4.3 \text{ V}$$

or $V_o = -5 + 0.7 = -4.3$ V

Example 14.5

For the network of Fig. 14.12, determine V_{o1} and V_{o2}

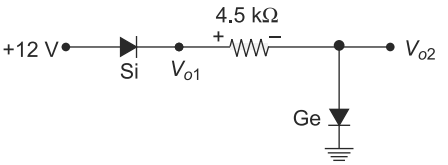


Fig. 14.12

Solution

$V_{o2} = 0.3$ V or V_T(Ge) = 0.3 V when conducting

$V_{o1} = 12 - 0.7 = 11.3$ V

Note the result does not depend on 4.5 kΩ.

Example 14.6

For the diode network of Fig. 14.13, determine V_o.

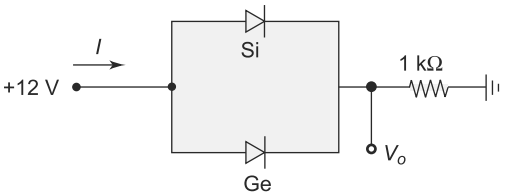


Fig. 14.13

Solution Diode Ge conducts, holding voltage at $V_T = 0.3$ V. Therefore, diode Si does not conduct as its $V_T = 0.7$ V

$$I = \frac{12 - 0.3}{1} = 11.7 \text{mA}$$

$$V_o = 1 \times 11.7 = 11.7 \text{ V}$$

Example 14.7

Determine V_o for the negative logic OR gate.

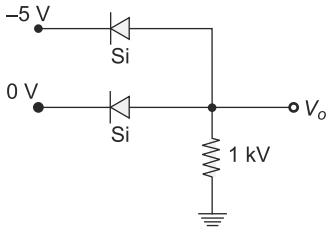


Fig. 14.14

Solution Top diode conducts

$$V_o = -5 + 0.7 = -4.3 \text{ V}$$

Lower diode is negatively biased, so does not conduct.

The output will be V_o = –4.3 V (high of negative logic) for input –5 V at any one or both terminals. The output will be zero (low) if both inputs are zero. This is presented in tabular form in Fig. 14.15.

In		Out
0	0	0
0	1	1
1	0	1
1	1	1

0 ~ Low (0 V)

1 ~ High (–4.3 V)

Fig. 14.15

Example 14.8

Determine V_o for negative logic AND gate of Fig. 14.16.

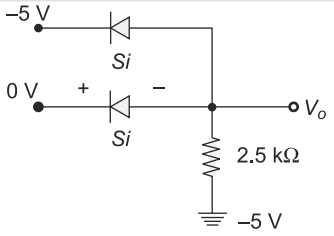


Fig. 14.16

Solution The lower diode will conduct.

$$V_o = -5 + 0.7 = -4.3 \text{ V (low, 0)}$$

If both inputs are 0 V, both diodes conduct. V_o = –4.3 V (low, 0). If both inputs are –5 V, both diodes do not conduct, V_o = –5 V (high, 1)

–5 V = high, 1 – 4.3 V – 0 V = low, 0

The result is presented in the table below.

In		Out
0	0	0
1	0	0
0	1	0
1	1	1

This is negative logic, AND.

14.3 ZENER DIODE

A zener diode has zener breakdown in reverse bias as shown in *IV* characteristic of Fig. 14.17(a). The symbol of the zener diode is drawn in Fig. 14.17(b). Its equivalent circuit is drawn in Fig. 14.17(c). It is connected in a circuit such that it is reverse biased. It conducts only if reverse bias exceeds V_z. For positive bias, it acts as short circuit.

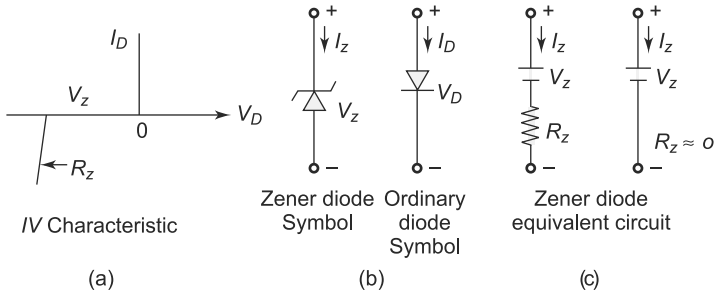


Fig. 14.17 *Zener diode*

❑ **Application** A zener diode when connected in reverse bias across two nodes does not permit the voltage to exceed V_z. It thus acts as voltage regulator.

Example 14.9

The circuit of Fig. 14.18 has a zener diode connected across the load.

(a) For R_L = 180 Ω, determine all currents and voltages.

(b) Repeat part (a) for R_L = 450 Ω.

(c) Find the value of R_L for the zener to draw maximum power.

(d) Find the minimum value of R_L for the zener to be just in on-state.

Solution

(a) As R_L is small, assume that the zener does not conduct,
i.e. $I_z = 0$.

Then, $$I_R = I_L = \frac{20}{200 + 180} = 52.6 \text{ mA}$$

$$V_z = V_L = 20 - 200 \times 52.6 \times 10^{-3} = 9.48 < 10 \text{ V}$$

So our assumption is correct.

(b) $$R_L = 450 \text{ V}$$

Assume that the zener conducts.

$$V_L = V_z = 10 \text{ V}$$

$$I_L = \frac{10}{450} \times 10^3 = 22.2 \text{ mA}$$

$$I_R = \frac{20 - 10}{200} \times 10^3 = 50 \text{ mA}$$

$$I_z = 50 - 22.2 = 27.8 \text{ mA}$$

$$P_z = 27.8 \times 10 = 278 \text{ mW} < 350 \text{ mW (rating)}$$

(c) When the zener draws maximum power,

$$I_z = \frac{350}{10} = 35 \text{ mA}$$

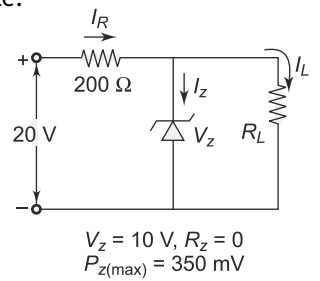


Fig. 14.18

Then $$I_R = \frac{20-10}{200}\times 10^3 = 50 \text{ mA}$$

$$I_L = I_R - I_z = 50 - 3.5 = 15 \text{ mA}$$

$$R_L = \frac{10}{15}\times 10^{-3} = 667\ \Omega$$

(d) $I_z = 0$ (just on state)

$$I_R = 50 \text{ mA} = I_L$$

$$V_L = V_z = 10 \text{ V}$$

$$R_L \text{ (min)} = \frac{10}{50}\times 10^{-3} = 200\ \Omega$$

Example 14.10

Determine the range of V_i in which the zener diode of Fig. 14.19 conducts.

Solution

(a) V_z just in conducting state

$$V_z = 20 \text{ V}, I_z = 0$$

$$I_R = I_L = \frac{20}{1.25} = 16 \text{ mA}$$

$$V_i = 20 + 220 \times 16 \times 10^{-3} = 23.52 \text{ V}$$

(b) $$I_z = I_z(\text{max}) = \frac{1200}{20} = 60 \text{ mA}$$

$$I_L = 16 \text{ mA}$$

$$I_R = 60 + 16 = 76 \text{ mA}$$

$$V_i = 20 + 220 \times 76 \times 10^{-3} = 36.72 \text{ V}$$

For input voltage from 23.52 V to 36.72 V, V_L will remain constant at 20 V.

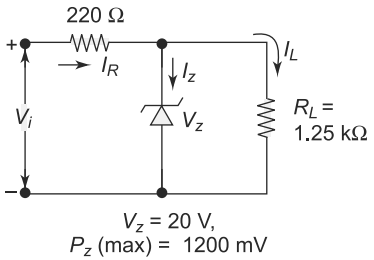


Fig. 14.19

14.4 RECTIFICATION

The diode is an ideal and simple device to convert ac to dc. The process is called rectification. We shall focus our attention on some performance measures of a rectifier: dc voltage, ripple factor, power conversion efficiency, PIV, and voltage regulation.

14.4.1 Half-wave Rectification (Sinusoidal Input)

The half-wave rectification is carried out by the simple circuit of Fig. 14.20 with a single diode. The diode conducts during positive half-cycles of input voltage and cuts off during negative half-cycle. The input and output waveforms are shown in the Fig. 14.20.

The *dc output voltage* is found as

$$V_{\text{dc}} = \frac{1}{2\pi}\left[V_m \int_0^{\pi} \sin \omega t \, d\omega + 0\right] = \frac{V_m}{\pi} = 0.318\, V_m \tag{14.3}$$

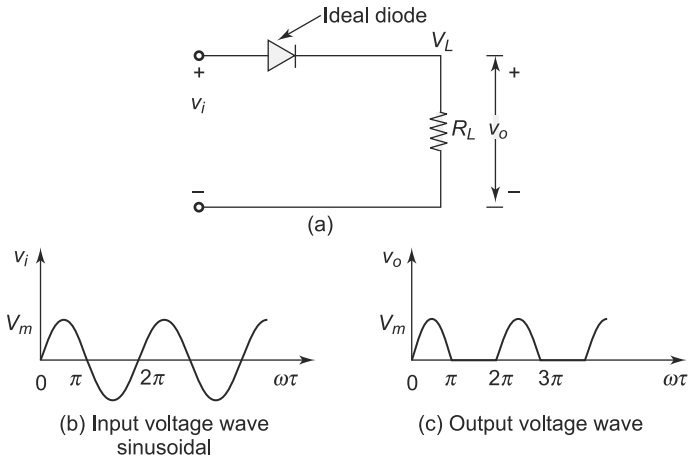


Fig. 14.20 *Input/output waveforms of half-wave rectification*

Then
$$I_{\text{dc}} = \frac{V_m}{\pi} \cdot \frac{1}{R_L} = \frac{I_m}{\pi} = 0.318\, I_m \tag{14.4}$$

PIV—During negative half, the input voltage reverse biases the diode. So PIV = V_m

Ripple Factor

Ripple is the variation of output voltage about dc, which is quite large in a half-rectified wave. It has frequency twice the frequency of the input voltage wave.

Ripple factor is defined as

$$\gamma = \frac{\text{rms value of the ac component of load (output) voltage}}{\text{dc component of load voltage}} \tag{14.5}$$

We can write the equality

$$V_{L\,\text{rms}} = \left[V^2_{L\,\text{ac rms}} + V^2_{L\text{dc}} \right]^{1/2}$$

or
$$\gamma = \left[\frac{V^2_{L\text{rms}}}{V^2_{L\text{dc}}} - 1 \right]^{1/2} \tag{14.6}$$

$V_{L\,\text{rms}}$ = rms of half sine wave $(0 - \pi)$ over $(0 - 2\pi)$

$$V_{L\,\text{rms}} = \sqrt{\left(\frac{V_m}{\sqrt{2}} \right)^2 \times \frac{1}{2}} = \frac{V_m}{2}$$

Then
$$\gamma = \left[\frac{(V_m/2)^2}{(V_m/\pi)^2} - 1 \right]^{1/2} = \left[\left(\frac{\pi}{2} \right)^2 - 1 \right]^{1/2} = 1.21 \tag{14.7}$$

We find that ripple factor of a half-wave rectifier is quite high, which is unacceptable.

The value of V_{dc} can be adjusted by providing V_i from a transformer of appropriate turn ratio.

For small values of V_m, we need to replace V_m by $(V_m - V_T)$ in all the above relationships.

Power Conversion Efficiency

It is defined as

$$\eta = \frac{\text{dc power input}}{\text{ac power input}}$$

Assuming the diode to be ideal in a half-wave rectifier,

$$\text{dc output} = I_{\text{dc}}^2 R_L$$

$$\text{ac input} = I_{\text{rms}}^2 R_L$$

$$I_{\text{rms}} = \sqrt{\left(\frac{I_m}{\sqrt{2}}\right)^2 \div 2} = \frac{I_m}{2}$$

$$\eta = \left(\frac{I_{\text{dc}}}{I_{\text{rms}}}\right)^2 = \left(\frac{I_m/\pi}{I_m/2}\right)^2 = \left(\frac{2}{\pi}\right)^2 = 0.405 \text{ or } 40.5\% \text{ (ideal)} \tag{14.8}$$

14.4.2 Full-wave Rectification

In order to reduce the ripple factor and raise the dc voltage level, we switch to full-wave rectification in which the phase of the second half of the wave is reversed. The full-wave rectified waveform is drawn in Fig. 14.21.

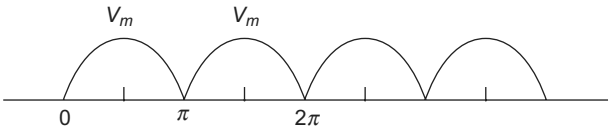


Fig. 14.21 *Full-wave rectified waveform*

Obviously,

$$V_{\text{dc}} = \frac{2V_m}{\pi} = 0.638\, V_m \text{ (double of half-wave)} \tag{14.9}$$

$$I_{\text{dc}} = \frac{2I_m}{\pi};\ I_m = \frac{V_m}{R_L}$$

Ripple Factor

$$V_{i\,\text{rms}} = \frac{V_m}{\sqrt{2}}$$

Substituting in Eq. (14.7),

$$\gamma = \left[\left(\frac{V_m/\sqrt{2}}{2V_m/\pi}\right)^2 - 1\right] = \left[\left(\frac{\pi^2}{8}\right) - 1\right]^{1/2} = 0.482 \tag{14.10}$$

The ripple factor is reduced from 1.21 to 0.482; consider also improvement.

Power Conversion Efficiency

$$\text{dc output} = I_{\text{dc}}^2 R_L$$

$$I_{\text{rms}} = \frac{I_m}{\sqrt{2}}$$

$$\text{ac input} = I^2_{\text{rms}} R_L$$

$$\eta = \left(\frac{I_{\text{dc}}}{I_{\text{rms}}}\right)^2 = \left(\frac{I_m/\pi}{I_m/\sqrt{2}}\right)^2 = \left(\frac{2\sqrt{2}}{\pi}\right)^2 = 0.81 \text{ or } 81\% \text{ (ideal)} \tag{14.11}$$

We shall now take up two full-wave rectification circuits.

14.4.3 Bridge Rectifier

It is a bridge of four diodes as shown in Fig. 14.22. In positive half-cycle of input v_i, diodes D_2 and D_3 conduct through the load R_L. The conduction path is shown by a solid line. During negative half-cycle, the polarity of v_i reverses; diodes D_4 and D_1 conduct through R_L in the same direction. The conduction path is shown by a dotted line. Thus, in both half-cycles, the current flows in the same direction through R_L. The voltage across R_L is, therefore, rectified voltage; see the output waveforms shown in Fig. 14.21.

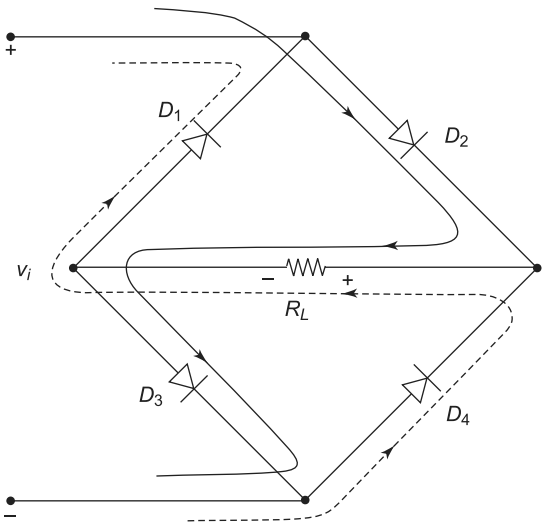


Fig. 14.22 *Bridge rectifier*

PIV

When D_2, D_3 are conducting reverse voltage across D_1, which in off position, is equal to the voltage across R_L, its peak value is V_m. The same applies when D_1, D_4 conduct. Therefore,

$$\text{PIV} > V_m$$

A bridge rectifier can provide high dc voltages. It is commonly used in electronic circuits.

14.4.4 Rectifier with Centre-Tapped (CT) Transformer

The circuit diagram of a CT transformer with diodes connected at each end and load connected to the central tap is drawn in Fig. 14.23. During positive half-cycle of $v_i(u)$, the diode D_1 conducts feeding the load with polarities shown in the figure. During negative half-cycle, the polarities of $v_i(u)$ and $v_i(l)$ reverse. D_2 conducts feeding the load as shown by dotted lines. The polarity of the load remains the same (rectification) while v_i is sinusoidal (ac), and v_o is rectified sine wave (see Fig. 14.23). All the relationships apply with V_m = peak value of half-secondary.

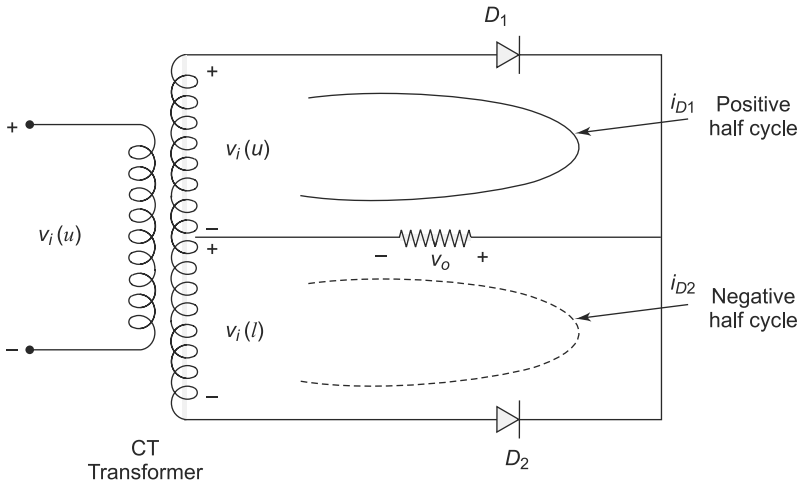


Fig. 14.23 *Rectifier with CT transformer*

PIV

When D_1 is conducting, D_2 is 'off', and the reverse voltage across D_2 is $v_i(l) + v_o$. At peak value, $v_d(l) + v_o = 2V_m$. Hence,

$$\text{PIV} > 2V_m$$

Filtering

Even in full-wave rectification the ripple factor is quite high (0.482). Therefore, the rectified output is filtered to reduce its ac content. This is achieved by connecting a capacitor (large size) across the load as shown in Fig. 14.24. Under steady conditions when v_i is less than v_o, the capacitor feeds the load (at time constant $1/R_LC$). When v_i increases above v_o, the diode conducts till $v_o = v_c$ during which period the source charges the capacitor. The output waveform is shown in Fig. 14.25, which has very much reduced ripple voltage (more smooth dc).

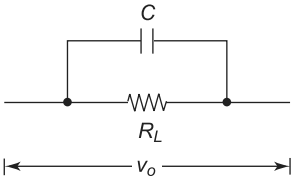
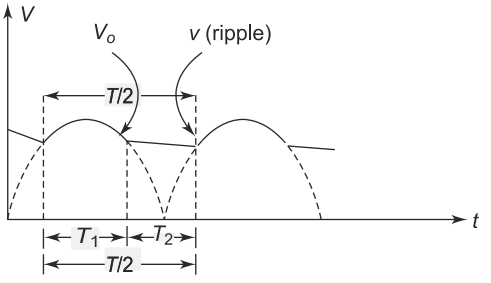


Fig. 14.24 *Capacitor across load*



T1—diode conducts
T2—capacitor conducts
v (ripple) = peak-to-peak;
ripple voltage considerably reduced

Fig. 14.25 *Filtered waveform*

14.4.5 Choke-capacitor Filter

The choke-capacitor filter of Fig. 14.26 is much more effective and is used for large dc power. The ripple factor can be made almost negligible because of the nonlinearity of choke not being used in low power electronic circuits.

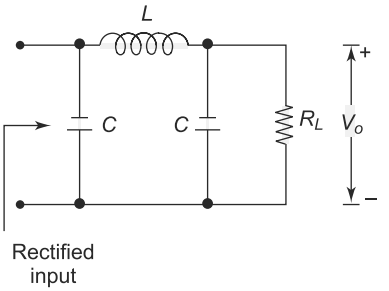


Fig. 14.26 *Choke-capacitor filter*

Example 14.11

For the diode network of Fig. 14.27, sketch v_i, v_d and i_d if the input is sinusoidal of 50 Hz.

Solution

$$V_{\text{dc}} = \frac{V_m}{\pi} = 2\,\text{V}$$

$$v_i \text{ peak} = V_m = 2\pi\,\text{V}$$

$$i_d \text{ peak} = I_m = \frac{2\pi}{2.5} = 2.51\,\text{mA}$$

$v_d = 0$, diode is ideal

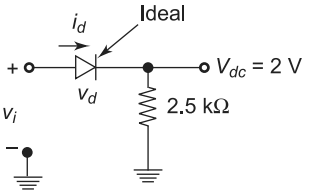


Fig. 14.27

The waveform sketches are drawn in Fig. 14.28.

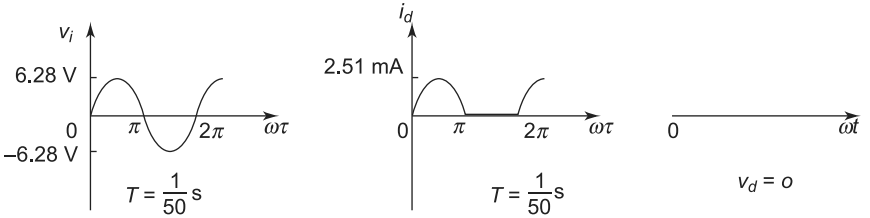


Fig. 14.28

Example 14.12

Repeat Example 14.11 if the diode has V_T = 0.7 V.

Solution

$$v_d = \frac{V_m - V_T}{\pi} = 2\,\text{V}, \text{ it is an approximation as output voltage is not exactly sinusoidal.}$$

$$v_i \text{ peak} = V_m = 2\pi + 0.7 = 6.98\,\text{V}$$

For $v_i < V_T = 0.7$ V, $i_d = 0$ at time t_1,

$$6.98 \sin 2\pi f t_1 = 0.7 \text{ V},$$

$$t_1 = 0.0011 \text{ s}$$

$$i_d \text{ peak, } I_m = \frac{V_m - V_T}{2.5} = \frac{2\pi}{2.5} = 2.51 \text{ mA}$$

v_i in sinusoidal with peak 6.98 V, $f = 50$ Hz

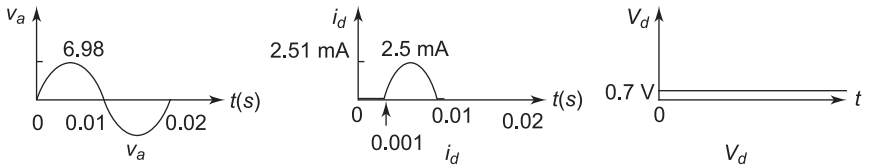


Fig. 14.29

Example 14.13

For the network of Fig. 14.30, sketch v_o and determine V_{dc}.

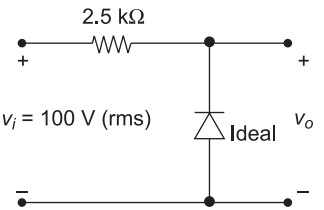


Fig. 14.30

Solution

$$\text{Input } V_m = 100\sqrt{2} = 141.4 \text{ V}$$

$$V_{dc} = \frac{V_m}{\pi} = \frac{141.4}{\pi} = 45 \text{ V}$$

During positive half-cycle of v_i, the diode does not conduct, $v_o = v_i$. During negative half-cycle of v_i, the diode conducts, causing short circuit at output terminals; $v_o = 0$. See Fig. 14.31.

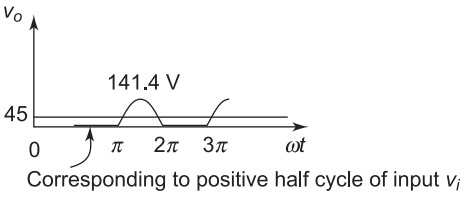


Fig. 14.31

Example 14.14

For a sinusoidal input of 10 V peak, sketch i_R and v_o in the network of Fig. 14.32.

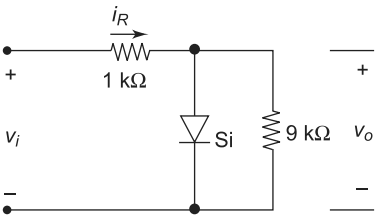


Fig. 14.32

Solution

For Si, $V_T = 0.7$ V

During positive half-cycle, the diode does not conduct up to 0.7 V.

$$v_i \Rightarrow 0 - 0.7 \text{ V}$$

$$v_o = \left(\frac{9}{10}\right) v_i$$

$$= 0.9\, v_i \text{ up to } 0.7 \text{ V}$$

$$i_R = 0.1\, v_i \text{ up to } 0.07 \text{ mA}$$

For $v_i \geq 0.7$ V, diode voltage remains constant on both halves of the cycle.

$$v_o = 0.7 \text{ V},$$

$$i_R = \frac{v_i - 0.7}{1}$$

$$= (v_i - 0.7) \text{ mA}$$

i_R (peak) = (10 – 0.7) = 9.3 mA

During negative half-cycle, the diode open circuits

$$i_R \text{ (peak)} = \frac{10}{1} = 10 \text{ mA}$$

$$v_o = 0.9\, v_i \text{ peak} = 9 \text{ V}$$

v_o and i_R are sketched in Fig. 14.33.

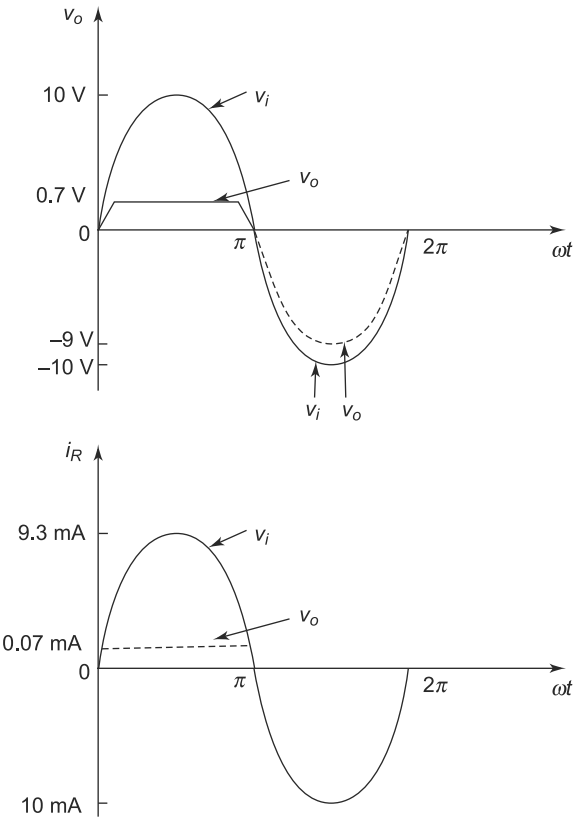


Fig. 14.33

Example 14.15

A full-wave bridge rectifier with an input of 100 V (rms) feeds a load of 1 kΩ. V_T = 0.7 V

(a) If the diodes employed are of silicon, what is the dc voltage across the load?

(b) Determine the maximum current that each diode conducts and the diode power rating.

(c) Determine the PIV rating of each diode.

Solution

(a) Peak values of input, $V_m = 100\sqrt{2} = 141.4$ V

$$V_{dc} = \frac{2(V_m - 2V_T)}{\pi}, \text{ conduction path is through two diodes.}$$

or

$$V_{\text{dc}} = \frac{2(141.4 - 2 \times 0.7)}{\pi} = 44.56 \text{ V}$$

(b)

$$I_m = \frac{V_m - 2V_T}{1} = 140 \text{ mA}$$

$$I\text{(rms) (each diode)} = \frac{140}{\sqrt{2}} \text{ mA}$$

Diode power rating $P_0 = \frac{140}{\sqrt{2}} \times 0.7 = 69 \text{ mW}$

(c) PIV > V_m = 141.4 V

14.5 WAVE SHAPING

Diodes find several applications in wave shaping, some of which are discussed here.

14.5.1 Clamping

A clamping circuit fixes the dc level of a signal to a new value. Also, when feeding the signal to an amplifier, a dc component, if present, must be removed. In a TV signal, the dc level need to be clamped to build the peak value of a complex TV signal.

A clamping circuit requires a diode, a capacitor and a resistor. It may also need an independent source. The circuit is so constructed that during charging, there is no series resistance and so the *capacitor charges instantaneously*. While discharging, the time constant $RC >> T = 2\pi f/\omega$ (signal time period). During this period, the capacitor *practically holds charge*, after which begins the next charging cycle.

Consider the diode circuit of Fig. 14.34(a) in which C and R fulfill the conditions mentioned above. The input voltage wave is drawn in Fig. 14.34(b). During the negative half cycle of input, the diode conducts and the capacitor gets charged to a polarity indicated in Fig. 14.34(b), beyond which the diode open circuits. The output voltage is

$$v_o = A + A \sin \omega t$$

which is sketched in Fig. 14.34 (c). The output is clamped at the minimum value of 0. Any small loss of charge is made up when the output touches zero and the diode conducts momentarily.

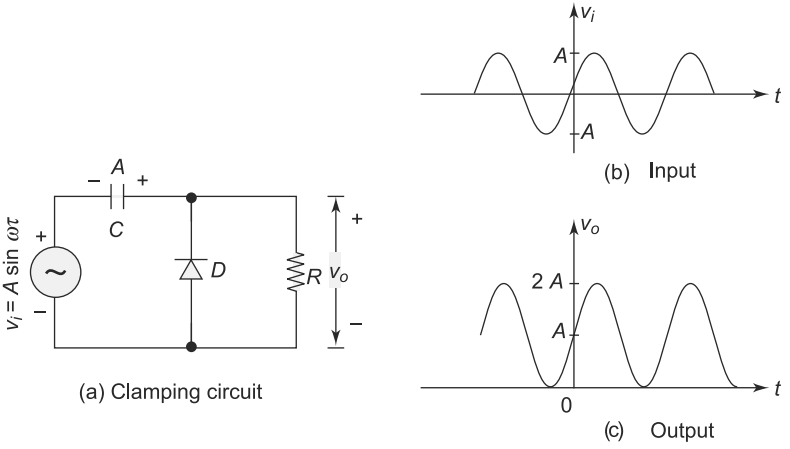


Fig. 14.34 *Clamping*

Observation

In clamping, the peak-to-peak value of the signal at output is same as of input (2 A). The signal has shifted up by +Δ.

14.5.2 Clamping Circuit Diode with Negative Bias (Fig. 14.35)

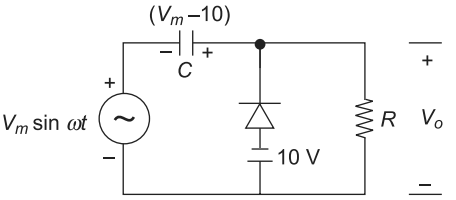


Fig. 14.35 *Clamper diode with negative bias*

During negative half cycle, the diode conducts and the capacitor charges to $(V_m - 10)$, polarity indicated. The output:

Positive peak

$$V_m + (V_m - 10) = 2\,V_m - 10$$

Negative peak

$$-V_m + (V_m - 10) = 10 \text{ V}$$

The output waveform in sketched in Fig. 14.36. The minimum values is clamped at –10 V.

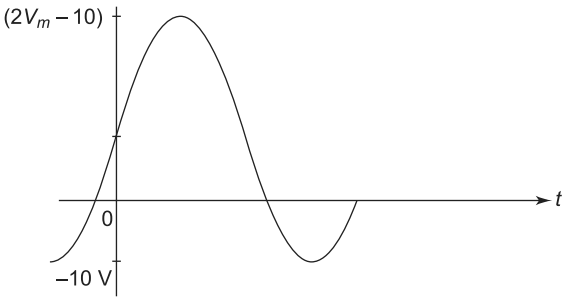


Fig. 14.36 *Output waveform*

14.5.3 Clamping Circuit with Pulse Input

For the clamping circuit of Fig. 14.37, determine the output for a rectangular pulse train of Fig. 14.38.

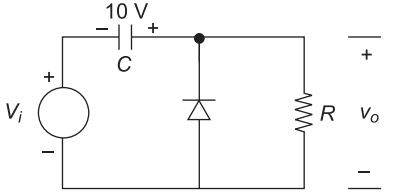


Fig. 14.37

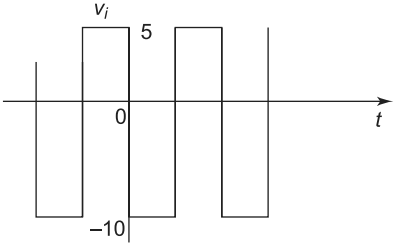


Fig. 14.38

When v_i = 10 V, the diode conducts and the capacitor charges to 10 V, polarity shown in Fig. 14.38. Then

$$v_o = v_i + 10 \text{ V}$$

Thus, the pulse train moves up by 10 V. The pulse varies from (5 + 10) = +15 V to (–10 + 10) = 0 V. The reader may sketch the wave.

14.5.4 Clipping

A part of the input signal is cut off or dipped while the remaining part is intact. A half-wave rectifier is a clipper. For clipping, a diode is used in series or shunt. In a rectifier, the diode is used in series. We will take up the circuit with the diode in shunt.

14.5.5 Shunt Diode

A clipping circuit with shunt diode and voltage source is drawn in Fig. 14.39(a). The diode conducts, when $v_i > V_1$ and so the output becomes zero; This part of the signal is clipped. The part of the signal $v_i < V_1$ appears as such at the output as the diode is open circuited. For a sine wave having $V_m > V_1$, the output wave shape is drawn in Fig. 14.39(b).

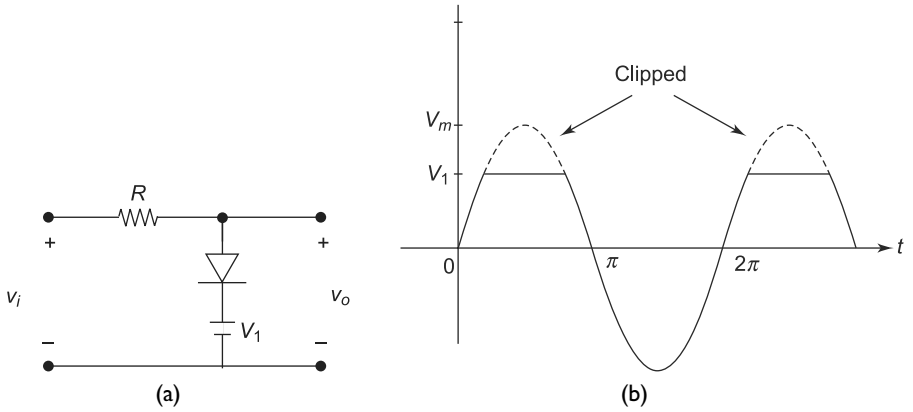


Fig. 14.39 *(a) Clipping circuit with shunt diode and voltage source (b) Output wave shape*

14.5.6 Voltage Doubler

Half-wave

The voltage doubler circuit is drawn in Fig. 14.40.

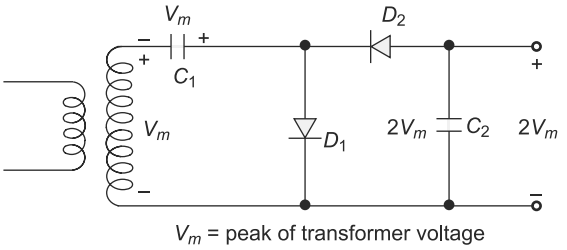


Fig. 14.40 *Half-wave voltage doubler circuit*

- During the positive half-cycle, D_1 conducts and C_1 gets charged to V_m. D_2 does not conduct and C_2 is uncharged.
- During negative half-cycle, the transformer voltage sign reverses. D_2 conducts through C_2 so that C_2 gets charged to $V_m + V_m = 2\ V_m$, output.

Full-wave

The circuit is drawn in Fig. 14.41

- During positive half-cycle, D_1 conducts and C_1 charges to V_m.
- During negative half-cycle, D_2 conducts and C_2 charges to V_m
- Output $V_m + V_m = 2\ V_m$

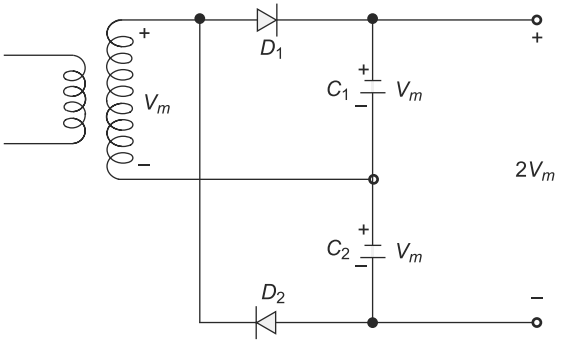


Fig. 14.41 *Full-wave voltage doubler*

14.5.7 Peak Detector

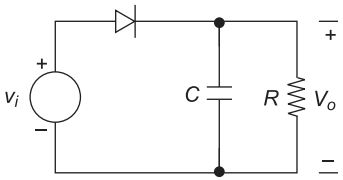


Fig. 14.42 *Peak detector*

The circuit of a peak detector is shown in Fig. 14.42. It is indeed a half-wave rectifier with an *RC* filter. Consider the input to be sinusoidal as shown in Fig. 14.43. During positive half-cycle, the diode conductors and *C* charges to *A* volts, the diode now stops conducting. If $RC >> T = 2\pi/\omega$, v_o decays exponentially till slightly less than $5\pi/\omega$. The diode again conducts and charges to *A*; the process thereon repeats.

The input has a small ripple voltage and its average value is close to the peak value *A*.

This circuit is employed in *envelop detection* of Amplitude Modulated (AM) wave.

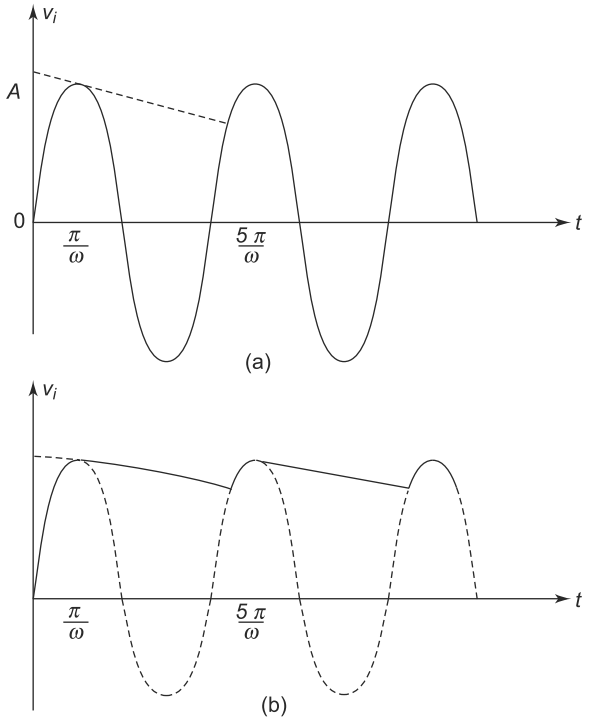


Fig. 14.43 *(a) Sinusoidal input (b) Output*

14.6 SPECIAL-PURPOSE DIODES

The *IV* characteristics of a *PN*-junction can be considerably modified from that of a normal diode by control of doping level and choice of material. These are other two-terminal devices which are highly sensitive (or produce light). These belong to the general category of photoelectric devices. All these will be briefly introduced here.

14.6.1 Schottky Barrier Diode

It is formed by metal-semiconductor junction, which provides rectifying action. The constructional details are shown in the cross-sectional view of Fig. 14.44(a). The metal (Al) contact with the n^+ semiconductor forms a rectifying junction. The majority electrons from the semiconductor flow in large number into the metal, which has its own pre-electrons by smaller energy. The semiconductor gets somewhat deflected by electrons. The barrier potential so formed prevents any further flow of electrons. The Al metal forms the *anode* and the n^+ region is the *cathode*.

When a forward bias is applied, the conduction is solely by electrons as there are no holes in the metal. The threshold voltage V_T = 0.3 V is less than 0.7 V for a silicon ordinary diode. This means less power dissipation in a Schottky diode. Further, the recovery time upon switch-off is very small, about 10–20 ns, as there is no recombination of electron-holes.

The symbol of Schottky diode and equivalent circuit are shown in Fig. 14.44(b) and (c).

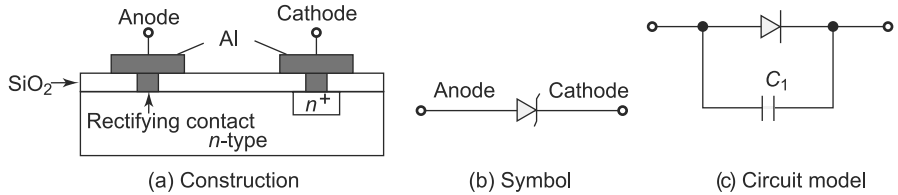


Fig. 14.44 *Schottky diode*

14.6.2 Tunnel Diode

As the doping levels of *N*- and *P*-sides of a diode are heavily increased, the depletion region becomes very narrow. When the depletion layer width becomes 1 nm or less, low-energy electrons are able to cross the barrier by a process called *tunnelling*. So the conduction begins at much lower values of bias voltage, where there is no injunction current.

The *IV* characteristic of a tunnel diode is sketched in Fig. 14.45.

As the bias voltage increases, the current reaches its maximum value I_p at V_p, beyond which no more electrons are available and holes have decreased. The current now begins to reduce reaching the minimum value of I_v and V_v. In this region, the diode offers negative resistance; beyond V_v the diode behaves like a normal diode.

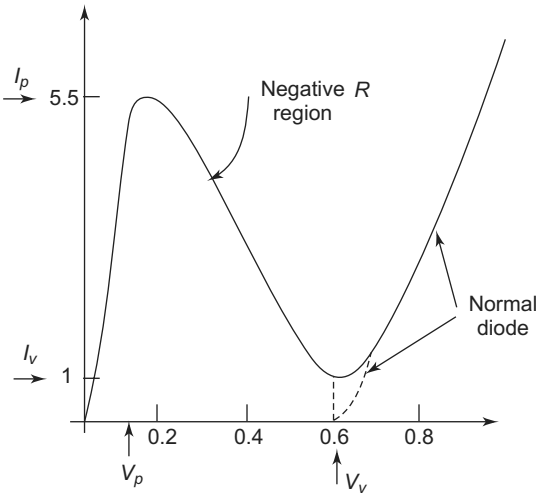


Fig. 14.45 *Characteristic of tunnel diode*

Application

In a high-frequency *LC* oscillator circuit, tunnel diode is included whose negative portion makes up the loss in *LC* circuit resistance.

The figure of merit of a tunnel diode is the ratio (I_p/I_v). Its value is 10 for germanium and 20 for gallium arsenide.

14.6.3 Varactor (Varicap) Diode

A diode with reverse bias has wide depletion region and positive and negative charges on each side. Therefore, it possesses a capacitance.

$$C_T = \in \frac{A}{W_d};$$

A = area of depletion region , W_d = its width , $\in$ = permittivity of semiconductor material C_T is called *transition capacitance*. As the width of the depletion region varies with reverse voltage (V_R), the transition capacitance varies accordingly. The transition capacitance can be approximated as

$$C_T = \frac{K}{(V_T + V_R)^n} \tag{14.12}$$

where V_T = threshold voltage
V_R = reverse bias (magnitude), can be a maximum of 20 V
K = constant of semiconductor material
n = ½ for alloyed junction and 1/3 for differed junction

A typical plot of C_T vs V_R is shown in Fig. 14.46(a) where $C(0)$ is the capacitance at $V_R = 0$. Equation (14.12) can be expressed as

$$C_T = \frac{C(0)}{\left[1 + \left(\left|V_T/V_R\right|\right)^n\right]} \tag{14.13}$$

The equivalent circuit and symbol of a varicap are drawn in Fig. 14.46(b) and (c).

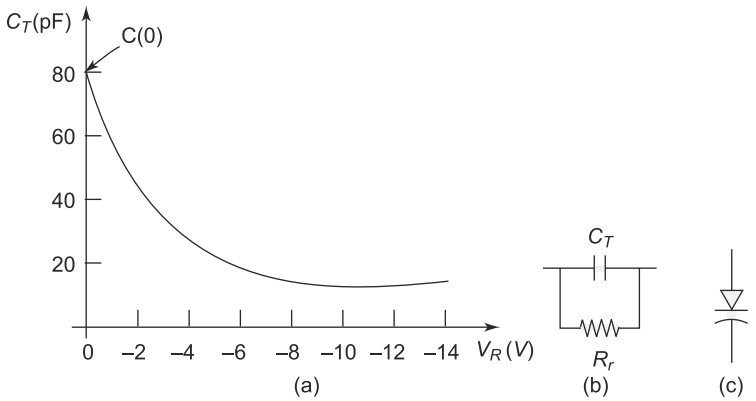


Fig. 14.46 *(a) Plot of C_T vs V_R (b) Equivalent circuit (c) Symbol*

R_r = reverse resistance of diode, very large (more than 1 MΩ)

Change in temperature affects the thermally generated carriers and therefore, the transition capacitance. The temperature coefficient of $C(0)$ is provided by manufacturers.

Application

A varactor is employed as variable capacitance of tank-circuit high-frequency oscillation for changing the oscillation frequency.

14.6.4 Photodiode

The field of photoelectrons has quite a variety of applications and has been attracting deep research interest. Here, we will study two kinds of devices—one in which light controls diode current and the other in which diode emits light when carrying current.

Light Definition and Units

As per the quantum theory of light, light is in the form of photons and each photon delivers an energy packet to the surface on which it falls.

$$W = hf \text{ joules}$$

where h = Planck's constant (6.624×10^{-34} joule seconds)
f = frequency of light waves in Hz.

Note that light also behaves as a travelling wave.

The frequency of light is directly related to its wavelength (distance between successive peaks) as

$$f = \frac{v}{\lambda}$$

where v = velocity of light (3×10^8 m/s)
λ = wavelength in metres

Units of wavelength are angstrom (Å) or micrometer (μm).

1 Å = 10^{-10} m, 1 μm = 10^{-6} m

Intensity of light is measured in units of luminous flux incident on unit area. Units of luminous flux are lumens where

$$1 \text{ lm} = 1.496 \times 10^{-10} \text{ W}$$

Practical unit of intensity of light is

1 lm/ft^2, called foot-candle (fc) = 1.609×10^{-9} W/m^2

A *photodiode* is a *PN*-junction (silicon/germanium) operated in reverse-bias region as shown in Fig. 14.47. The reverse saturation current I_λ (μA) flows limited by the availability of thermally generated minority carrier. As light is made to impinge on the junction, the light photons impart energy to the valence electrons causing more electron-hole pairs to be released. As a result, the concentration of minority carriers increases and so does the current I_λ. The symbol of a photodiode is drawn in Fig. 14.47(b).

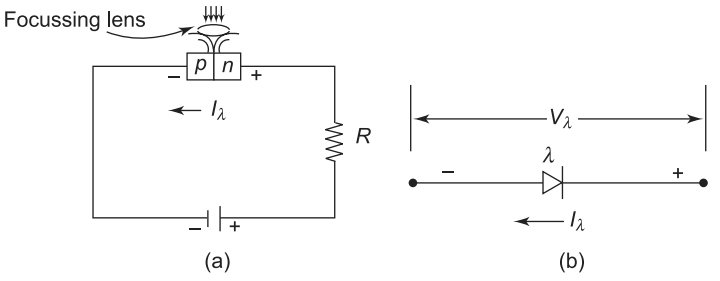


Fig. 14.47 *(a) Photodiode in reverse bias (b) Symbol*

The *IV* characteristics for various values of light intensity (*fc*) are drawn in Fig. 14.48. The dark current characteristic corresponding to no-light impingement (($I_\lambda = I_s$). By examining the characteristics it is found that at a certain V_λ (say 20 V), I_λ increases almost linearly with f_{cs}.

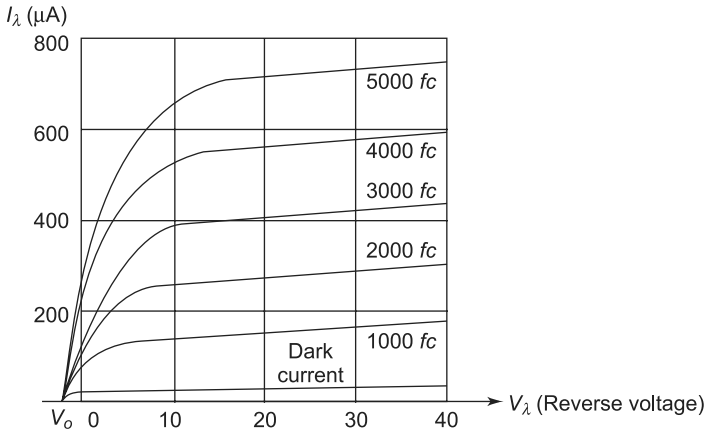


Fig. 14.48 *IV characteristics of photodiode*

It has been found that Ge photodiode has more overlaps compared to Si, which is in the range of light frequencies to which the human eye is sensitive. Ge is, therefore, more suitable for infra-red (IR) light sources like laser.

14.6.5 Light-Emitting Diode (LED)

In a forward biased *PN*-junction, diode recombination of electrons and holes takes place at the junction and within the body of the crystal, particularly at the location of a crystal defect. Upon capture of a free electron by a hole, the electron goes into a new state and its kinetic energy is given off as heat and as light photons. In a silicon diode, most of this energy is given off as heat but in other materials such as gallium arsenide (GaAs) or gallium phosphide (GaP), sufficient number of photons (light) are generated so as to create a visible source. This process of light emission in *PN*-junctions of such materials is illustrated in Fig. 14.49 and is known as *electroluminescence*. The metal contact of *P*-material is made much small to permit the emergence of maximum number of photons so that in an LED, the light lumens generated per watt of electric power is quite high. Intensity of light increases almost linearly with forward current, depending on the material used.

The voltage levels of LEDs are 1.7 V to 3.3 V which is compatible with the solid-state circuits. The response time is short (only a few nanoseconds) and light contrast is good.

LEDs emit light red, green, orange or blue.

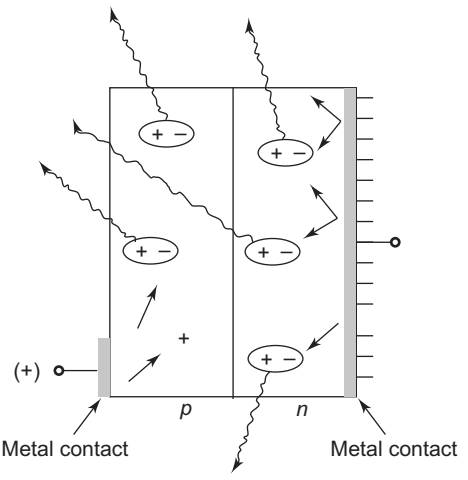


Fig. 14.49 *Light emission in PN-junction*

Applications

LEDs find several display applications, particularly in 8-segment display of numbers 0 to 9. These are now being used in LED TV's.

14.6.6 Photocoupler

It is a package of an LED and photodiode whereas circuits are electrically isolated as shown in Fig. 14.50. The LED is forward biased and the photodiode is reverse biased. The output is available across R_2.

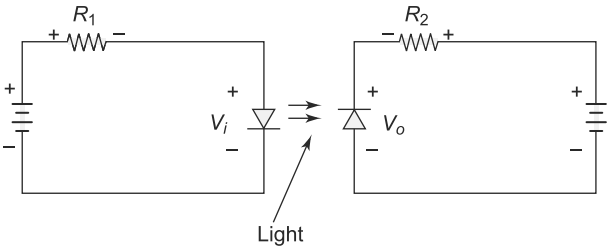


Fig. 14.50 *Photocoupler*

The key advantage of the photocoupler is the electrical isolation between two circuits. It is employed to couple circuits whose voltage level may differ by several thousand volts.

Example 14.16

Determine the transistor capacitance of diffused junction varactor at a reverse potential of 4.5 V, if $C(0) = 85$ pF and $V_T = 0.7$ V. Also determine the values of K in Eq. (14.12).

Solution

$$C_T = \frac{C(10)}{1 + \left(\left|V_T / V_R\right|\right)^n} = \frac{85}{1 + \left(\frac{0.7}{4.5}\right)^{2/3}} = 55.3 \text{ pF}$$

$$C_T = \frac{K}{(V_T + V_R)^n}$$

$$55.3 = \frac{k}{(0.7 + 4.5)^{1/3}}, \text{ k} = 95.8 \text{ pF} - \text{V}^{1/3}$$

Example 14.17

For a photodiode, determine I_λ if V_λ = 30 V and intensity of light is 3.22×10^{-6} W/m^2. Read from Fig. 14.48.

Solution Light intensity in *fc*

$$fc = \frac{3.22 \times 10^{-6}}{1.609 \times 10^{-9}} = 2000$$

Reading from Fig. 14.48 we find

$$I_\lambda \approx 300 \text{ μA}$$

Summary

➢ Various types of diodes, rectifiers have been described in this chapter along with their characteristics and applications.

Exercises

Review Questions

1. Explain what is depletion region in a *PN*-junction diode?
2. What is reverse saturation current in a diode? Does it exist in both reverse-biased and forward-biased diodes.
3. What is threshold voltage of a diode? What is its value for Si and Gi diodes?
4. Write the diode conduction equation. Explain the meaning of each symbol.
5. Draw the circuit equivalent of a forward-biased diode.
6. Explain the operation of a zener diode and draw its circuit equivalent.
7. A zener diode acts as a voltage regulator. Explain the meaning of the statement.
8. Draw the circuit of a bridge rectifier. What is the input and output waveform?
9. Write the expression of dc voltage of half-wave and full-wave rectifiers.
10. What is the ripple factor of a diode rectifier? Derive its expression for a full-wave rectifier. Will the ripple factor be more or less than this value for a half-wave rectifier?
11. What is the conversion efficiency of a rectifier circuit? Derive its expression for a full-wave rectifier. Will the value be more or less than this in a half-wave rectifier?

Problems

1. For the diode circuit of Fig. 14.51, determine I, V_1, V_2, V_0.

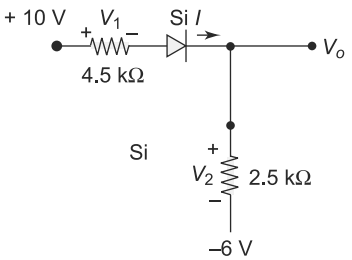


Fig. 14.51

2 For the diode circuit of Fig. 14.52, determine I_1, I_2, I_{D2}.

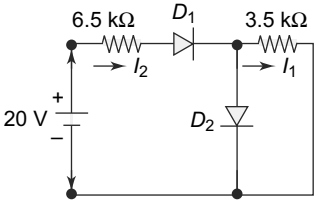


Fig. 14.52

3. For the diode OR gate logic of Fig. 14.53, prepare a table of inputs and corresponding outputs.
4. For the diode AND logic of Fig. 14.54, prepare a table of inputs and corresponding output.

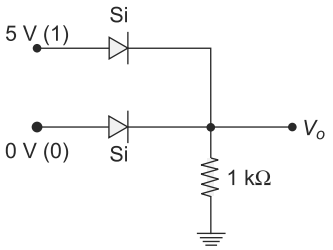


Fig. 14.53 *OR gate*

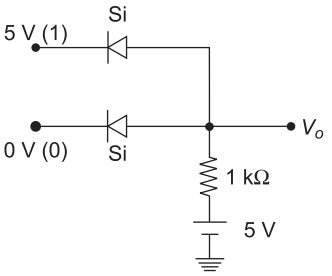


Fig. 14.54 *AND gate*

5. In the zener diode circuit of Fig. 14.55, V_L is to be maintained constant at 12 V, while I_L varies from 0 to 250 mA. Calculate the values of V_z, R_S and power rating of the zener.
6. For the circuit with zener diode (Fig. 14.56), determine the output for $V_i = 50$ V and $V_i = 5$ V.

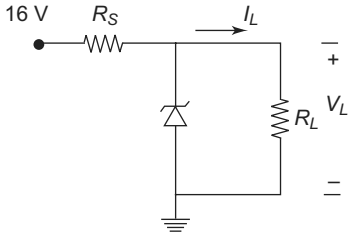


Fig. 14.55

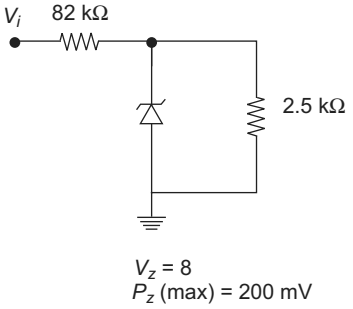


Fig. 14.56 P_z(max) = 200 mW

7. For the diode bridge of Fig. 14.57, V is sinusoidal with $V_m = 100$ V. Sketch v_o. Find V_o(dc) and PIV of each diode.

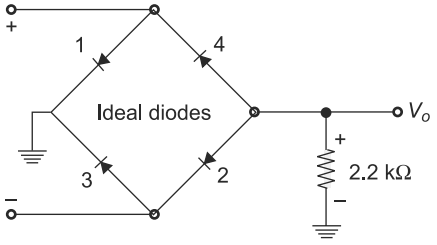


Fig. 14.57

8. For the diode network of Fig. 14.58, which is sinusoidal input with V_m = 170 V, determine V_o(dc).

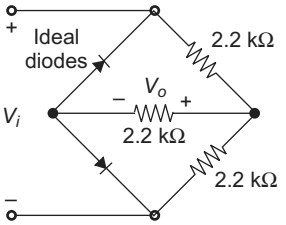


Fig. 14.58

9. A CT transformer full-wave rectifier has ac voltage of each half-secondary of 20 V(rms). The resistance of each half is 1 Ω. Diodes are Si–V_T = 0.7 V, r_d = 0.5 Ω. The load resistance is 15.5 Ω. Determine V_{dc} and I_{dc} of the load.
10. A bridge rectifier has four identical diodes of forward resistance of 5 Ω each. It is supplied from a transformer with output voltage of 20 V(rms) and secondary winding resistance of 10 Ω. Calculate the
    (a) dc output voltage at a dc load current of 100 mA
    (b) rms value of output voltage at a dc load current of 200 mA
    (c) rms value of the ac component of the voltage in part (b).
11. For the circuit of Fig. 14.59 and the given input signal, determine v_i and the output signal.

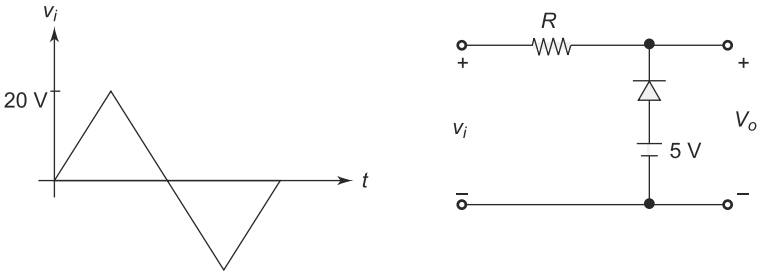


Fig. 14.59

12. Draw the output of the direction of the diode of Fig. 14.35 when reversed. A clamping circuit diode with negative bias is shown in Fig. 14.35.
13. In Fig. 14.36, reverse the direction of diode and bias voltage; sketch v_o.

Multiple-Choice Questions

1. The cut in (knee voltage) of a germanium diode is
   (a) 0.2 V (b) 0.3 V (c) 0.7 V (d) 0.8 V
2. Junction breakdown of a *PN*-junction diode occurs
   (a) with forward bias (b) with reverse bias
   (c) because of improper design (d) All of these
3. A zener diode
   (a) is useful as an amplifier
   (b) has a negative resistance
   (c) has a high forward voltage
   (d) has a sharp breakdown at low reverse voltage
4. Which of the following diodes is best suited as a switching diode for very high frequencies?
   (a) PIN diode (b) Zener diode
   (c) LED (d) Step recovery diode

5. The ripple factor of a half-wave rectifier is
   (a) 0.482 (b) 0.812 (c) 1.21 (d) 1.11
6. The ac resistance for a Ge semiconductor diode having a forward bias of 200 mV and reverse situation current of 1 μA at
   (a) 10.52 W (b) 11.86 W (c) 12.37 W (d) 15.49 W
7. Which of the following is a type of clipping circuit?
   (a) Positive clippers (b) Negative clippers
   (c) Biased clippers (d) All of these
8. Level shifter circuits are also known as
   (a) clipper circuits (b) clamper circuits (c) diodes (d) transistors
9. In a zener diode, the value of I_{zm}, if power dissipation rating is 500 mW and zener voltage rating is 6.8 V,
   (a) 78.6 mA (b) 80.2 mA (c) 82.5 mA (d) 73.5 mA
10. In an LED, light emission occurs because
    (a) light gets reflected due to lens action
    (b) light falling on the diode gets amplified
    (c) diode gets heated up
    (d) recombination of charge carriers takes place

Answers

Problems

1. 2.186 mA, 9.84 V, 5.46 V, −0.535 V
2. 0.2 mA, 2.86 mA, 2.66 mA
3. Input: High (1) = 5 V, Low (0) = 0 V
   Output: High (1) = 4.3 V, Low (0) = 0 V
4. Input: High (1) = 5 V, Low (0) = 0 V
   Output: High (1) = 5 V, Low (0) = 0.7 V
5. V_z = 12 V, R_S = 16 Ω, 3 W
6. 8 V, 0.15 V
7. 27.05 V
8. 16.57 V, 0.663 A
9. (a) 16 V (b) 15.5 V (c) 6.65 V
10.

Multiple-Choice Questions

1. b	2. b	3. d	4. a	5. a
6. b	7. d	8. b	9. d	10. d

Bipolar Junction Transistor (BJT) and Other Devices

chapter 15

Goals & Objectives

- Introduction and constructional details of bipolar junction transistor (BJT)
- Operational characteristics of BJT and configurations
- Description of silicon-controlled rectifier (SCR)
- Construction and characteristics of unijunction transistor (UJT)
- Types of dc biasing—self, voltage divider and voltage feedback bias.

15.1 INTRODUCTION

In Chapter 14, we understood how a two-layer, one-junction semiconductor device acts as a diode, which conducts current in a particular direction and whose magnitude is controlled by the external circuit supply. Basically, a transistor is a combination of two back-to-back diodes, provided crystal continuity is maintained. Addition of another layer results in a three-layer two junctions device which has *npn* or *pnp* form and is called a transistor. With a terminal connected to each layer, it acts as a *two-port device* (input/output ports) wherein one of the terminals is common between the two ports. Such a transistor is known as *Bipolar Junction Transistor* (BJT) which acts as a *current-controlled device* with the output current being controlled by the input current, such that the input-current waveform is replicated at the output. This is the amplifying action of a transistor commonly applied in various types of audio/video *amplifiers*. A BJT can also be made to act as a switch wherein the input current level controls the ON/OFF state of the output current. This mode of operation of a BJT finds wide applications in high-speed digital electronics.

15.2 BJT CONSTRUCTION AND OPERATION

The constructional details and order of dimension for the two types of BJT are shown in Fig. 15.1. In a *pnp* transistor, a thin *N*-type layer is sandwiched between two *P*-type layers, while in an *npn* transistor, a thin layer of *P*-type is sandwiched between two *N*-type layers.

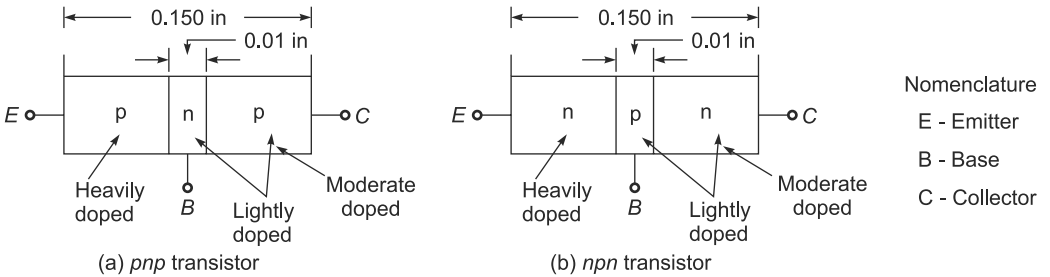


Fig. 15.1 *BJT Transistor—construction and order of dimensions*

Biasing

There are two junctions: *EB* junction and *CB* junction. A transistor is like two diodes.

EB junction: Forward-biased diode

CB junction: Reverse-biased diode

Voltage biasing of transistors is shown in Fig. 15.2.

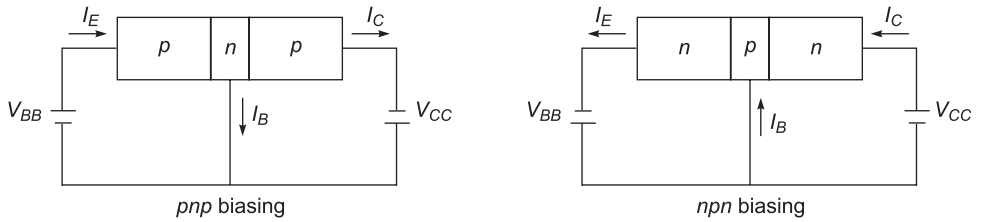


Fig. 15.2(a) *Direction of current is conventional (hole current)*

Transistor Symbols

Fig. 15.2(b) *Transistor symbols*

The type of transistor can be recognised from the direction of arrow of *E* (emitter).

Operation

An enlarged cross-sectional view of a *pnp* transistor is drawn in Fig. 15.3(a); not to scale.

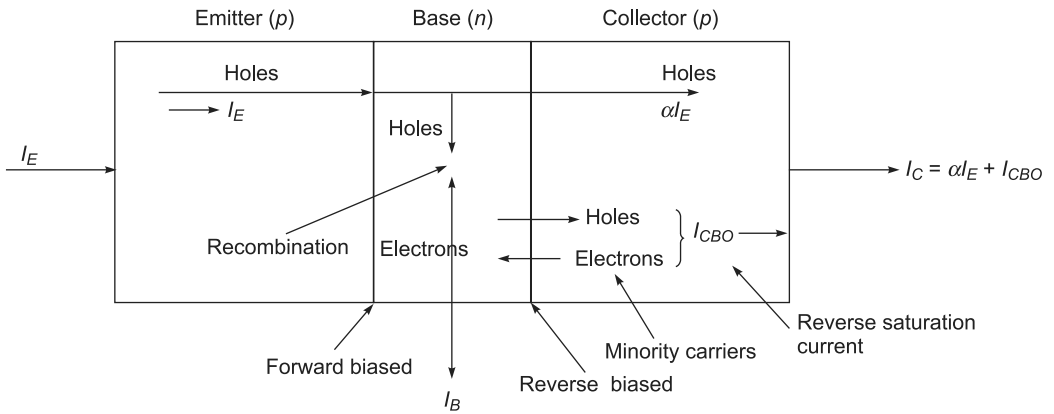


Fig. 15.3(a) *Carrier flow in a pnp transistor*

- Emitter holes (majority carriers) cross the forward-biased *EB* junction into the base. These constitute the emitter current I_E.
- The major portion of these holes cross over the reverse-biased CB junction constituting current αI_E; $\alpha = 0.98$ to 0.99. This is why the base width is kept very small.
- The reverse saturation current I_{CBO} flows across the *CB* junction. The controller current $I_C = \alpha I_E + I_{CBO}$ of order nA for Si.
- A small number of holes coming from the emitter recombine with electrons in the base. Recombination rate is small as electron concentration is very light in the base. To replenish the recombining electrons, a small electron current I_B flows out of the base. Note that direction of I_B is that of conventional current.
- Very few electrons from the base cross over to the emitter as the base is lightly doped. This current flow can be ignored [not shown in the figure]. As both electrons and holes participate in conduction, hence the name Bipolar Junction Transistor (BJT).

The following fundamental dc relationships emerge.

$$I_C = \alpha I_E + I_{CBO} \tag{15.1}$$

As per KCL $$I_E = I_C + I_B \tag{15.2}$$

Substituting I_E from Eq. (15.2) in Eq. (15.1),

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$

Or $$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO} \tag{15.3}$$

We define $$\beta = \frac{\alpha}{1-\alpha}; \quad \alpha = \frac{\beta}{1+\beta}$$

Then $$I_C = \beta I_B + (1 + \beta) I_{CBO} \tag{15.4}$$

I_{CBO}

If we make $I_E = 0$, open emitter

$I_{CBO} = I_{CO}$, reverse saturation current

as shown in Fig. 15.3(b).

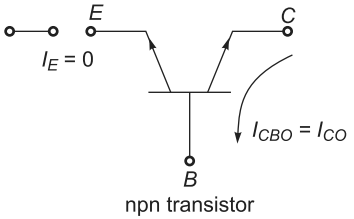


Fig. 15.3(b) *Open emitter*

Order of β

Let $\alpha = 0.988$

$$\beta = \frac{0.988}{1-0.988} = 82.3$$

Range of $\beta = 50 - 400$

Approximations

As I_{CBO} is the reverse saturation current (nA for Si), it can be neglected in Eq. (15.4) even though it is multiplied by $(1 + \beta)$

Thus, we can write

$I_C \approx \beta I_B$, we shall use this approximation most often (15.5)

Also, from Eq. (15.1),

$$I_C = \alpha I_E$$

or $I_C \approx I_E$ as $\alpha \approx 1$ (15.6)

Thus, we have from Eqs (15.5) and (15.6),

$$\alpha \approx \frac{I_C}{I_E}, \ \beta \approx \frac{I_C}{I_B} \tag{15.7}$$

15.2.1 Early Effect

Refer Fig. 15.4. At the *CB* junction, there is a depletion region as the *CB* junction is reversed biased, while there is no such region at the *EB* junction as it is forward biased. As V_{CB} increases, the depletion region, and so effective base width, reduces. This base-width modulation is known as *early effect*. Its consequences are the following:

- Reduction of base width results in hole crossover to the collector faster, which mean α increases.
- Concentration of electrons in base increases, which crossover to the emitter thereby increasing I_E.
- At extremely large values of V_{CB}, the base width reduces to zero causing BJT breakdown. This phenomenon is known as *punch through*.

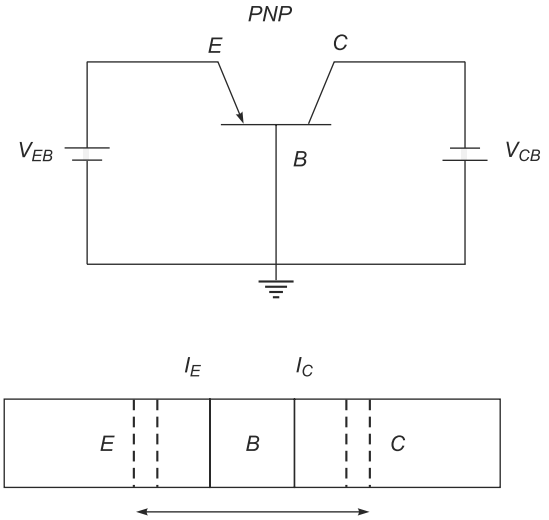


Fig. 15.4 *Basewidth modulation due to* V_{CB}

15.2.2 Ebers—Moll Model (Two-Diode Model)

It has been seen above that *BJT* has two junctions, *EB* and *CB,* which act as diodes. The *EB* diode is forward biased and the *CB* diode is reverse biased. It can, therefore, be modelled as two diodes shown in Fig. 15.5.

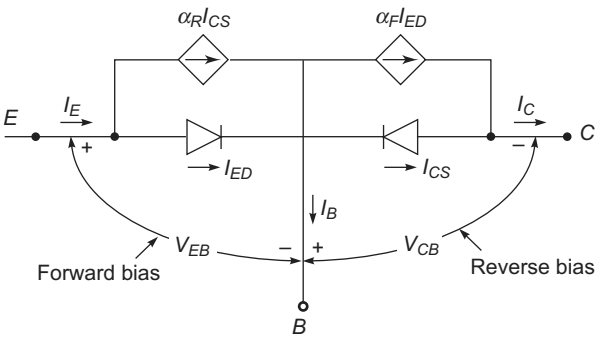


Fig. 15.5 *Two-diode model*

I_{CS} = reverse saturation current = I_{CBO} (in nA)

Range of α's

$$0.98 \le \alpha_F \le 0.998$$

$$0.4 \le \alpha_R \le 0.8$$

We can, therefore, ignore the dependent current $\alpha_R I_{CS}$. This will result in equations already presented.

15.3 BJT CONFIGURATIONS AND CHARACTERISTICS

As BJT is a three-terminal device, it can be connected in three possible configurations. For circuit operations, we require two terminals for input as well as output. So, one terminal of the transistor is grounded.

1. Common base
2. Common emitter
3. Common collector

To describe the behaviour of any configuration, two characteristics are required.

(i) Driving point or input

(ii) Output

15.3.1 Common Base Configuration

The circuit is drawn in Fig. 15.6. Unless otherwise mentioned the transistor is NPN.

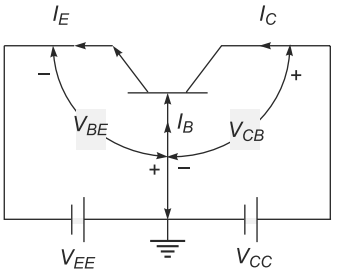


Fig. 15.6 *Common base configuration (NPN)*

Input (Driving-Point) Characteristic (I_E vs V_{BE})

The *EB* junction is a forward-biased diode. A typical characteristic to scale is presented Fig. 15.7. It is found that it is practically independent of V_{CB}. It can be approximated as a diode characteristic. Conduction begins for V_{BE} = 0.7 V as shown in Fig. 15.7(b).

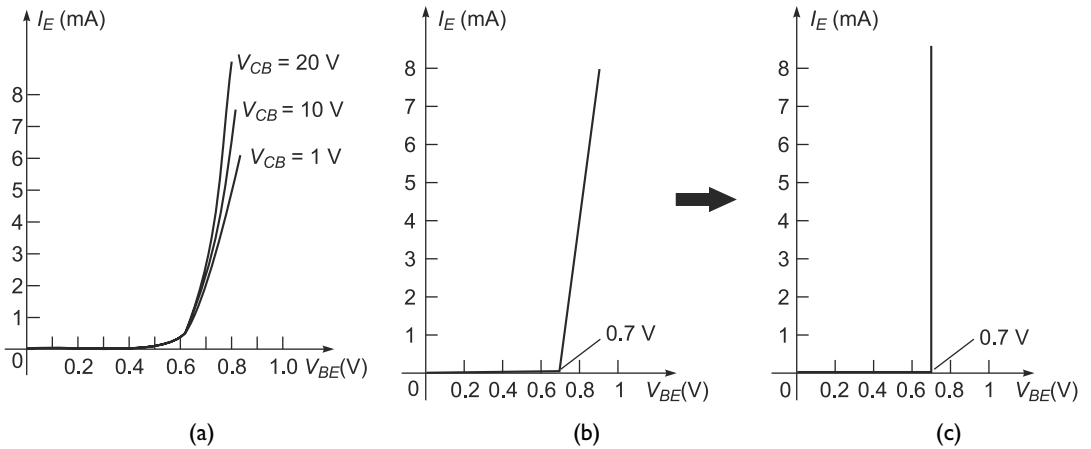


Fig. 15.7 *Driving point characteristic*

The current I_E is controlled by adding a resistance in series with V_{EE}, while it will be assumed that

$$V_{BE} = 0.7 \text{ V}$$

At any value of I_E, once the transistor starts conducting, ON state is shown in Fig. 15.7(c).

Output (Collector) Characteristics

These relate output current (I_C) with output voltage (V_{CB}) for varying values of input current (I_E). Typical output or collector characteristics are drawn in Fig. 15.8.

The characteristics can be divided into three regions.

Active Region

The base-emitter junction is forward biased, while the collector-base junction is reverse biased. All the carriers that are injected into the emitter are swept away through the base to the collector. As a result, as already shown that

$I_C = \alpha I_E$ or $I_C \approx I_E$ as $\alpha \approx 1$

α is the common-base forward current gain.

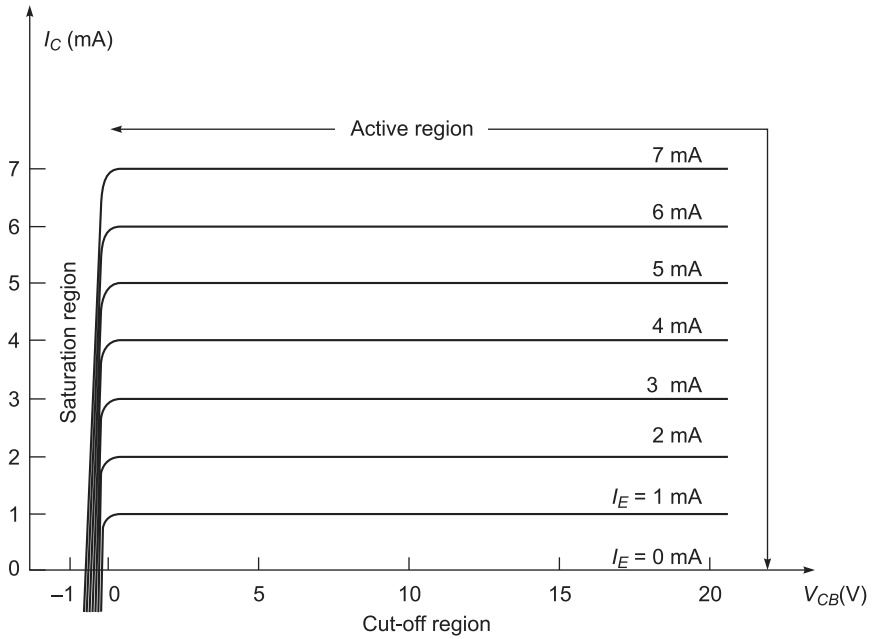


Fig. 15.8 *Collector characteristics*

This is easily seen from Fig. 15.8. Also, I_E is not affected by reverse bias V_{CB}. This is the linear region in which amplifying action of the circuit takes place.

Cut-off Region

In this region, both base-emitter and collector-base junctions are both reverse biased. As a result, $I_E = 0$ and so $I_C = 0$.

Saturation Region

In this region, both base-emitter and collector-base junctions are forward biased. This region is to the left of $V_{CB} = 0$. In this region, the collector current rises exponentially to the I_E value set by V_{BE} circuit as V_{CB} increases towards reverse bias.

Amplifying Action

Current amplification ≈ 1. The input current is transferred by the transistor to output.

Voltage amplification will result from low driving-point resistance (10 – 100 Ω) [see Fig. 15.7(b)] and high output resistance.

The configuration is not used for amplification but serves certain special purposes.

15.3.2 Common-Emitter (CE) Configuration

It is the most frequently used configuration. Its circuit is drawn in Fig. 15.9.

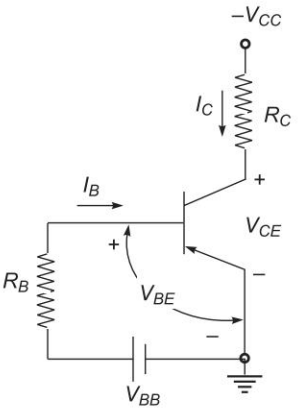


Fig. 15.9 *CE configuration*

Input (Base) Characteristics

I_B vs V_{BE} for varying V_{CE} is drawn in Fig. 15.10(b).

Output (Collector) Characteristics

I_C vs V_{CE} for various values of I_B is drawn in Fig. 15.10(a).

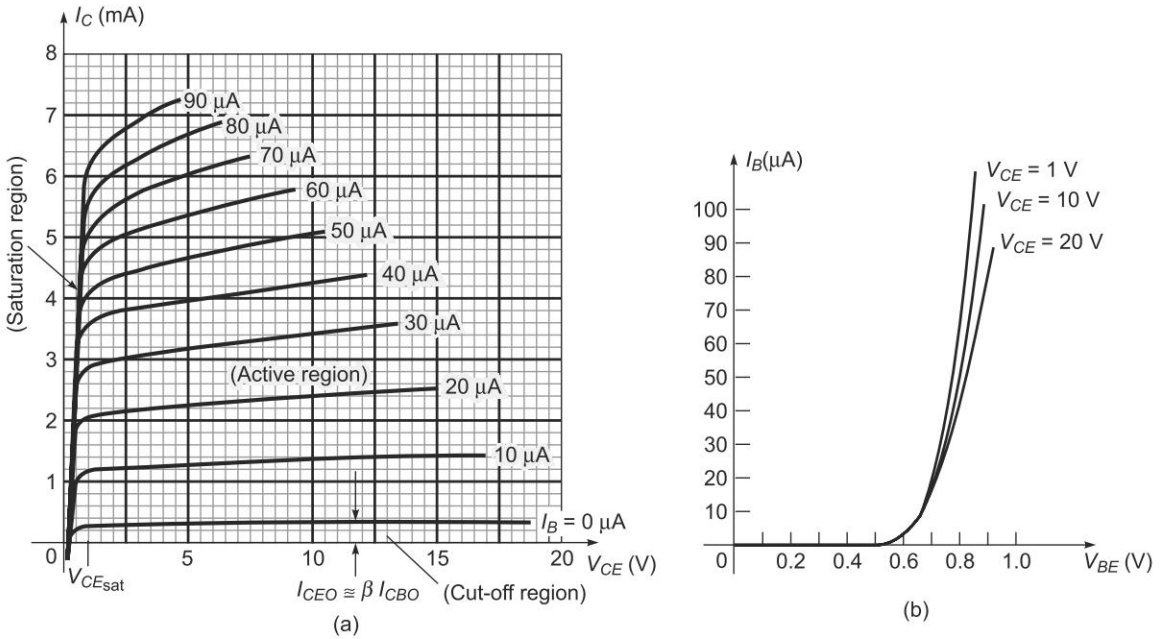


Fig. 15.10 *(a) Collector characteristics (b) Basic characteristics*

It is seen from the base characteristics that I_B is practically independent of V_{BE}. The base-emitter junction goes 'on' at V_{BE} = 0.7 V and then stays there, while I_B is adjusted by the external resistance R_B.

Active Region

Base-emitter is forward biased and collector-base is reverse biased. The collector characteristics are drawn in Fig. 15.10(a). It is seen that I_B is in μA and I_C in mA. These are related by β. The middle of this region is linear w.r.t. I_B and V_{CE}.

Cut-off Region

It is below $I_B = 0$; the *EB* junction becomes reverse biased but the corresponding $I_C \neq 0$. From Eq. (15.4),

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

or $$I_C = (1 + \beta) I_{CBO} \approx \beta I_{CBO}; \text{ for } I_B = 0$$

$$\beta I_{CBO} = I_{CEO} \tag{15.8}$$

If $I_{CBO} = 1$ μA, resulting from $I_B = 0$, then

$$I_{CEO} = 250 \times 1 \times 10^{-2} = 0.25 \text{ mA at } \beta = 250$$

Saturation Region

It is to the left of $V_{CE(\text{sat})} = 0.2$ V. In this region, the *CB* junction becomes forward biased and I_B no longer controls I_C.

β_{dc} and β_{ac} lie in the middle region of Fig. 15.10(a), at any point corresponding to a certain V_{CE} say 10 V.

$$\beta = \beta_{\text{dc}} = \frac{I_C}{I_B}, \text{ large signal gain} \tag{15.9}$$

For variation about this point along $V_{CE} = 10$ V,

$$\beta_{\text{ac}} = \frac{\Delta I_C}{\Delta I_B} \tag{15.10}$$

Study on typical collector characteristics shows that

$$\beta_{\text{ac}} \approx \beta_{\text{dc}}$$

We will use the symbol β for β_{dc} or β_{ac} which will be obvious from the study under investigation.

We observe here that β *is the common-emitter forward-current gain*.

15.3.3 Common Collector (CC) Configuration

This connection is similar to common emitter, except that output is taken from the emitter. This causes, the output to be in phase with input (signal). It offers a high input resistance and low output resistance. It is, therefore, employed for impedance matching.

In this configuration, α_R factor will exist which shows the amplification of input at output.

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \tag{15.11}$$

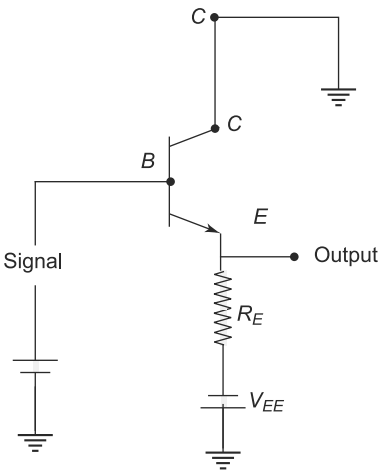


Fig. 15.11 *Configuration*

Limits of Operation

For each transistor, there are limits of operation which identify the region on its characteristics within which the signal exhibits least distortion. As shown in Fig. 15.12, the region is bounded by cut-off region, saturation region $I_{C(\max)}$, maximum power dissipation $P_{D(\max)} = V_{CE}\, I_C$, an inverse hyperbola and $V_{CE(\max)}$.

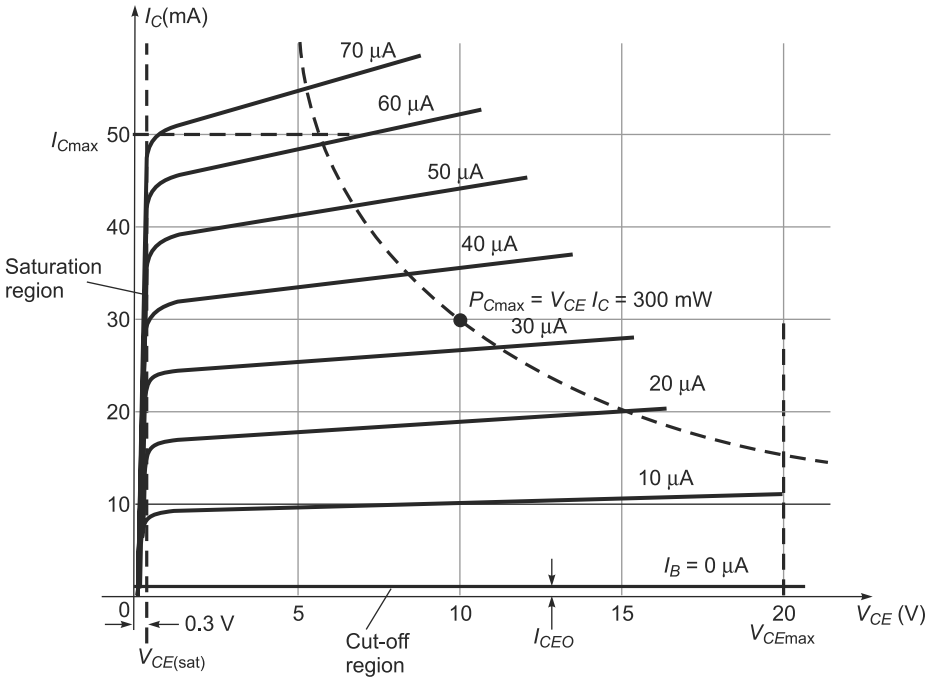


Fig. 15.12 *Limits of operation*

15.4 SILICON-CONTROLLED RECTIFIER (SCR)

It is a four-layer device which along with its associated circuitry has a very wide range of applications—rectifiers, regulated power supplies, dc to ac conversion (inverters), relay control, time-delay circuits and many more.

SCRs are now available to control power as high as 10 MW with individual rating of 2 kA and 1.8 kV. The frequency range has now been extended to 50 kHz, which are employed in high-frequency applications like induction heating and ultrasonic cleaning.

15.4.1 Basic Operation and Symbols

The material used for SCR is silicon because of high-temperature requirement of handling large current and power. Its four layers are arranged as *pnpn* shown in Fig. 15.13. The outer layers are connected to terminals to form **anode** (positive terminal) and **cathode** (negative terminal). The *P*-layer closer to the cathode is connected to the **gate** terminal. The SCR symbol is drawn in 15.13(b). It is similar to that of a diode, the difference being the indication of the gate terminal.

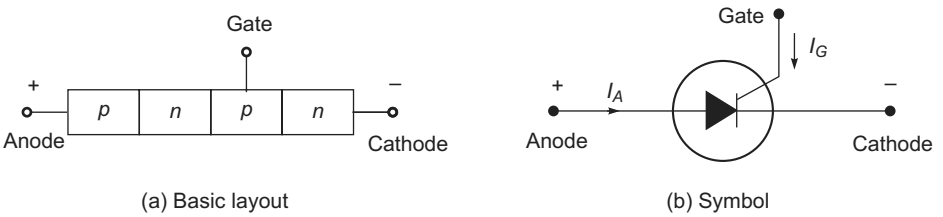


Fig. 15.13 *Silicon Controlled Rectifier (SCR)*

As a forward voltage is applied across the anode (+) and cathode (–), no conduction takes place as the middle *np*-junction is reverse biased. If a positive pulse is applied at the gate, such that a current of magnitude equal to more than I_G (turn-on) flows into the gate, the processes in the device cause it to go into conduction. The forward current (anode to cathode) is offered a resistance as low as 0.01 to 0.1 Ω. However, because of regenerative action, removing the gate current does not cause the device to turn off.

The dynamic reverse resistance of an SCR is as high as 100 kΩ or more.

15.4.2 Two-transistor Model

The cross-sectional view of an SCR with its four layers is drawn in Fig. 15.14(a). The middle *n* and *p* layers can be imagined to be subdivided into two halves, as shown by the dotted line. It is now immediately recognised that the device comprises one *PNP* and one *NPN* transistor. As there is an electrical continuity between the two halves of each of these layers, the base of *PNP* is connected to the collector of *NPN*; and the collector of *PNP* is connected to the base of *NPN*, while the gate is connected to the base of *NPN*.

The corresponding two-transistor equivalent circuit is drawn in Fig. 15.14(b); observe that the connections are consistent with Fig. 15.14(a). This circuit will now be used to explain the action of the gate pulse I_G.

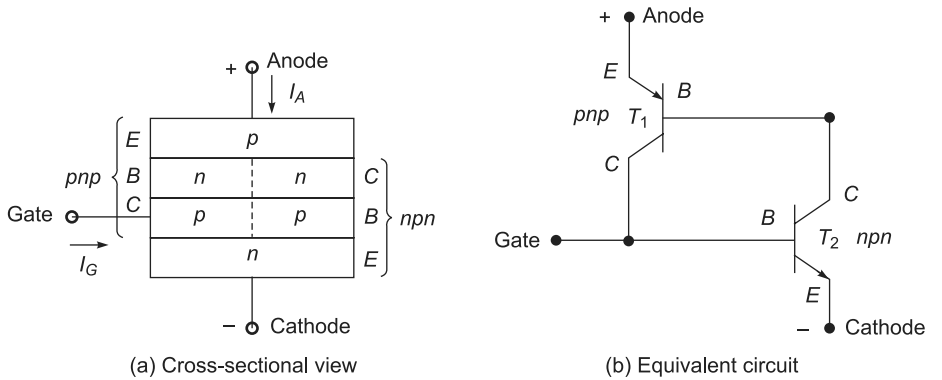


Fig. 15.14 *Two-transistor model of SCR*

15.4.3 Switching Action

Let a positive voltage *V* be applied to the anode (E_1), and the cathode (E_2) and gate (G) be both grounded as shown in Fig. 15.15(a). As $V_G = V_{BE2} = 0$, the transistor T_2 is in 'off' state. It means that *CB*-junction of T_2, through *EB*-junction of T_1, is reverse biased. Therefore, $I_{B1} = I_{CO}$ (minority carrier current) is too small to 'turn-on' T_1. Thus both T_1 and T_2 are 'off' and so anode current

$$I_A = I_{B1} = I_{CO}$$

is of negligible order. It means that SCR is in 'turn-off' state, that the switch between anode (E_1) and cathode (E_2) is open.

Now, let a voltage $+V_G$ be applied at the gate as shown in Fig. 15.15(b). As $V_{BE2} = V_G$, on making V_G sufficiently large, I_{B2} will cause T_2 to turn on and the collector current I_{C2} becomes large. As $I_{B1} = I_{C2}$, T_2 turns on causing a large collector current I_{C1} ($I_A = I_{C1}$) to flow. This in turn, increases I_{B2} causing a regenerative action to set in (this is indeed a positive internal feedback). The result is that the SCR is turned on, that is, the switch between the anode (E_1) and cathode (E_2) is closed (*turn-on*). The current I_A must be limited by the external circuit, say a series resistance between the source and E_1.

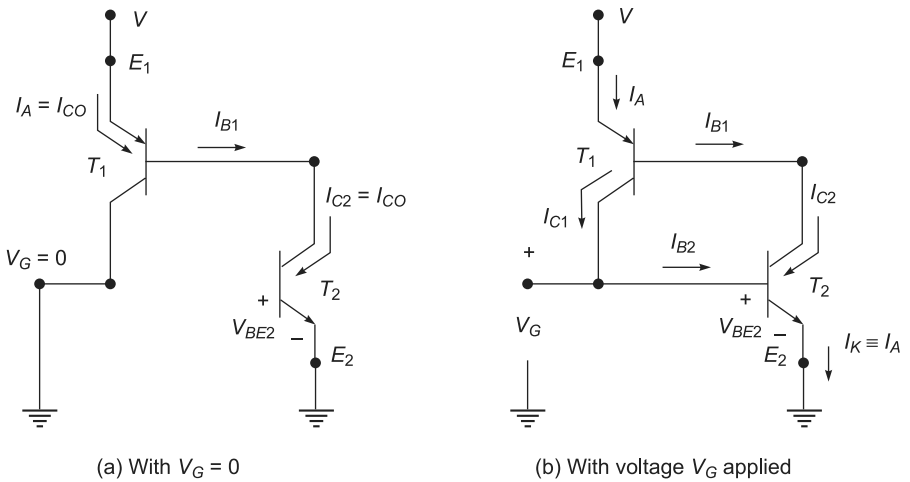


Fig. 15.15 *Switching action of a two-transistor SCR*

The turn-on time of an SCR is typically 0.1 to 1 μs. However, for high-power devices in the range of 100–400 A, turn-on time may be 10–25 μs.

Turn-off

As has been shown earlier, when the SCR is in conduction mode, the gate is ineffective in turning it off. The turn-off mechanism is called *commutation* and it can be achieved in two ways explained below.

❑ **Natural Commutation** When the source that feeds the current to anode of SCR is such that it naturally passes through zero, the SCR turns off at the current zero. This is the case when the SCR is fed from the ac source. In this situation, the commutation is also known as *line commutation*.

❑ **Forced Commutation** In this method of commutation, the current through the SCR is forced to become zero by passing a current through it in opposite direction from an independent circuit. A variety of SCR turn-off circuits are available in books and in manufacturer's manuals.

One basic turn-off circuit which illustrates the principle is drawn in Fig. 15.16. A transistor and dc battery source in series are connected to the SCR. When the SCR is in conduction mode (on), $I_B = 0$ and when the transistor is off, it is almost an open circuit. To turn off the SCR, a positive I_B pulse of magnitude large enough to drive the transistor into saturation is applied at the transistor base. The transistor acts almost like a short circuit. This causes flow of very large I_{off} through the SCR in the opposite direction to its conduction current. The total SCR current reduces to zero in a very short time causing it to turn off. The transistor has to withstand a large current but for a very short time.

Turn-off time of an SCR is typically 5–30 μs.

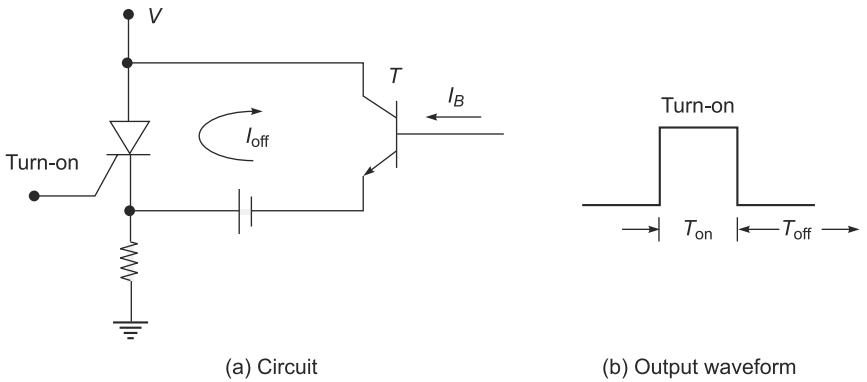


Fig. 15.16 *Turn-off circuit using SCR*

15.4.4 SCR Characteristics

The symbol and *I-V* characteristics of an SCR are given in Fig. 15.17. Various voltages and currents which provide important information for SCR applications are described below.

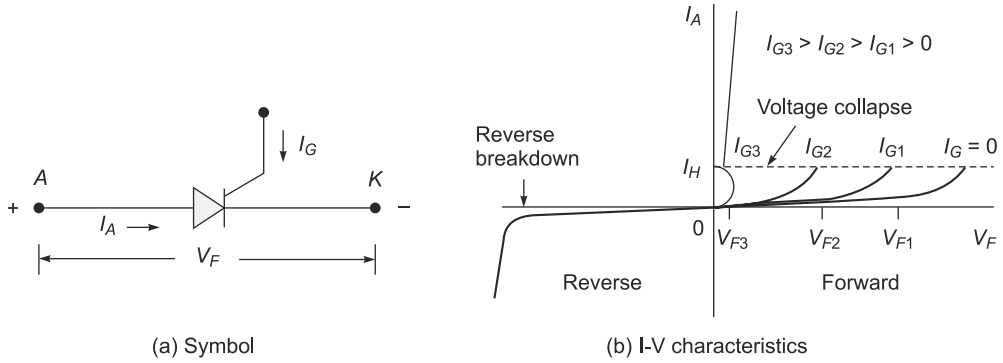


Fig. 15.17 *SCR characteristics*

1. *Forward Breakover Voltage* V_F (BR) is the voltage at which for a given I_G, the SCR enters into conduction mode. As is seen from Fig. 15.17, that this voltage reduces as I_G increases. V_F(BR) has dependence on the circuit connection between *G* and *K* terminals.
2. *Holding current* I_H is the value of the current below SCR switches from conduction state to forward blocking regions of specified conditions.
3. Forward and reverse blocking regions are those regions in which the SCR is open circuited and no current flows from anode to cathode.
4. Reverse breakdown voltage corresponds to Zener or avalanche region of a diode.

Other specifications of interest in designing SCR circuitry and systems are the grid voltage, current and power, their maximum permitted values symbolised as

$$P_{GFM}, I_{GFM}, V_{GFM}$$

The manufacturer's manual, apart from indicating these, identified the preferred region of operation.

15.4.5 Applications of SCR

The range of applications of SCRs given in the beginning of this section is by no means exhaustive. As for applications in power and drives, these form the subject matter of a separate course for which several excellent books are available. We shall give here a single application for illustrative purpose.

Variable Resistance Phase Control

On triggering, an SCR permits flow of only forward current but blocks the current in reverse direction. This action is the same as that of a diode. On application of alternating voltage, it causes rectified ac to flow but it needs to be triggerd for each positive half cycle of ac. It then produces constant dc (average value) current through load and dc voltage across load. Adjusting the triggering time on positive half cycle of ac voltage would yield variable dc output. This method is known as phase control.

A variable-resistance phase-control circuit is provided in Fig. 15.18(a). The SCR gate current is controlled through R and the variable R_1. Let R_G be adjusted to high value so that even at the peak value v_i (positive), $I_G < I_{G(\text{turn-on})}$ and no conduction takes place. As R_1 is reduced, I_G rises to turn-on value at a particular angle (time) of v_i. The conduction then begins and continues till v_i reaches zero (180°). Varying R_1 allows the adjust of SCR firing angle from 0° to 90° as shown in Fig. 15.17(b).

At R_1, corresponding to the firing angle of 90°, $v_i = v_i$ (max). If R_1 is adjusted for firing at α [see Fig. 15.17(b)], the firing will take place at angle $\alpha < 90°$ but not at angle $\beta = (180° - \alpha) > 90°$ as the angle α is reached earlier in time on the v_i-wave. So the operation of this circuit is known as *half-wave, variable-resistance phase control*.

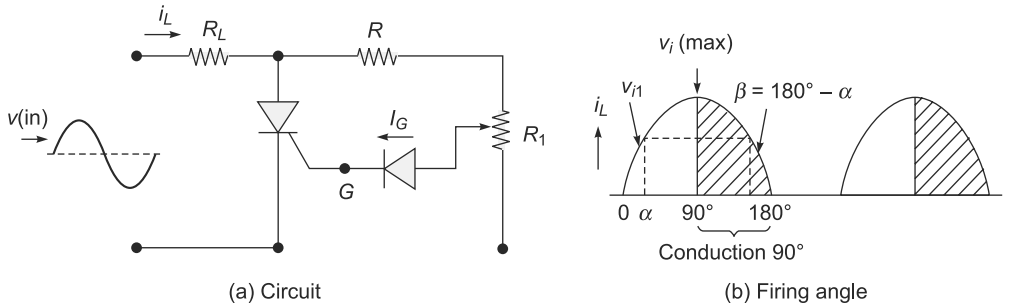


Fig. 15.18 *Variable resistance phase control*

Thus, i_L(dc) can be adjusted to the maximum value at 0° to the minimum value at 90°.

It may be noted that a diode is provided in the firing circuit to prevent the flow of reverse gate current.

15.4.6 DIAC

The DIAC is basically a two-terminal, parallel-inverse combination of semiconductor layers that permits triggering in either direction. The characteristics of the device, presented in Fig. 15.19(a), clearly demonstrate that there is a breakover voltage in either direction. This possibility of an on condition in either direction can be used to its fullest advantage in ac applications.

The basic arrangement of the semiconductor layers of the DIAC is shown in Fig. 15.19(b), along with its graphical symbol. Note that neither terminal is referred to as the cathode. Instead, there is an anode 1 (or electrode 1) and an anode 2 (or electrode 2). When the anode 1 is positive with respect to the anode 2, the semiconductor layers of particular interest are $p_1n_2p_2$ and n_3. For the anode 2 to be positive with respect to the anode 1, the applicable layers are $p_2n_2p_1$ and n_1.

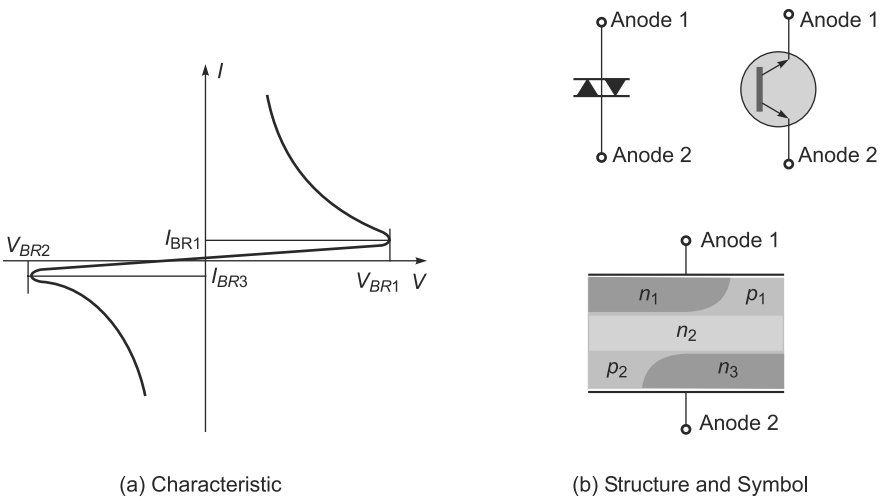


Fig. 15.19 *DIAC*

15.4.7 TRIAC

The TRIAC is fundamentally a DIAC with a gate terminal for controlling the turn-on conditions of the bilateral device in either direction. In other words, for either direction, the gate current can control the action of the device in a manner very similar to that demonstrated for an SCR. The characteristics, however, of the TRIAC in the first and third quadrants are somewhat different from those of the DIAC, as shown in Fig. 15.20. Note the holding current in each direction not present in the characteristics of the DIAC.

The graphical symbol for the device and the distribution of the semiconductor layers are provided in Fig. 15.20 with photographs of the device. For each possible direction of conduction, there is a combination of semiconductor layers whose state will be controlled by the signal applied to the gate terminal.

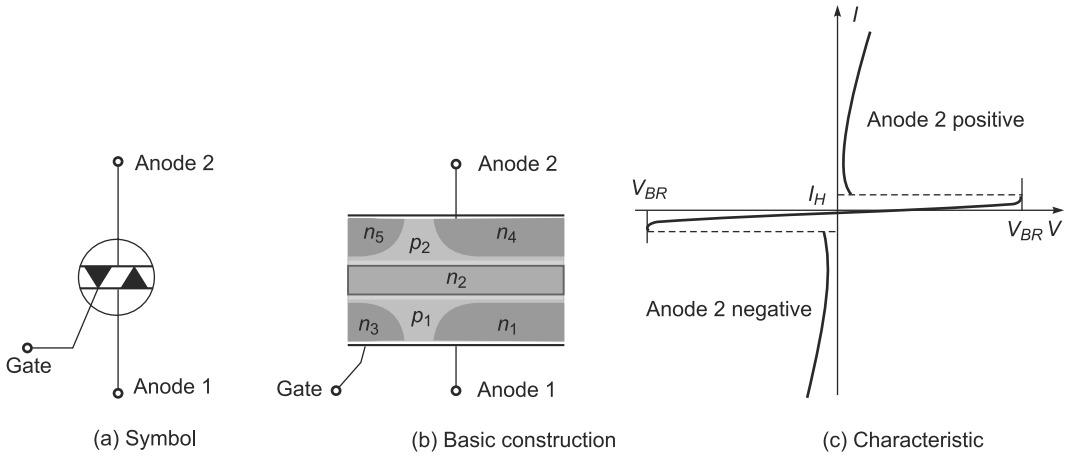


Fig. 15.20 *TRIAC*

15.5 UNIJUNCTION TRANSISTOR (UJT)

It is a low-cost device, which, because of its excellent characteristic and low power loss (in it), is commonly employed in a wide variety of applications like oscillators, trigger circuits, sawtooth generators, phase control, timing circuits, bistable networks and regulated supplies.

A UJT is a three-terminal device (basic construction shown in Fig. 15.21(a)) formed from a lightly doped slab on *N*-type material having high resistance characteristics. Two base contacts are made at each end of one side of the slab, while an aluminium rod is fused on the other side to form a single *pn*-junction, and hence the name unijunction. The rod is located closer to the base terminal 2 which is made positive with respect to the base terminal 1 by V_{BB}. The symbol and biasing of a UJT is shown in Fig. 15.21(b).

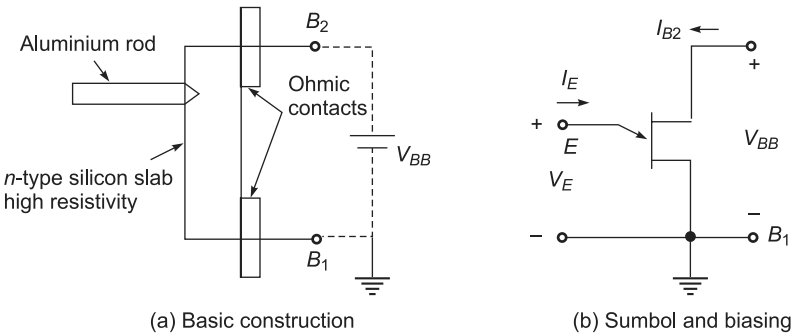


Fig. 15.21 *Unijunction transistor (UJT)*

The circuit equivalent to the UJT is drawn in Fig. 15.22. Here the input diode represents the *pn*-junction operation; R_{B2} is a fixed resistance and R_{B1} is a variable resistance, which reduces with increase in emitter current I_E. The range of variation of R_{B1} may be 50 kΩ to 50 Ω as I_E increases from 0 to 50 mA. The interbase resistance is defined as

$$R_{BB} = (R_{B1} + R_{B2})\big|_{I_E = 0} \tag{15.12}$$

The range of this resistance is typically 4–10 kΩ. At $I_E = 0$, the voltage

$$V(R_{B1}) = \frac{R_{B1} V_{BB}}{R_{B1} + R_{B2}}\bigg|_{I_E = 0} = \eta V_{BB} \tag{15.13}$$

where η, called *intrinsic stand-off ratio*, is given as

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}\bigg|_{I_E = 0} \tag{15.14}$$

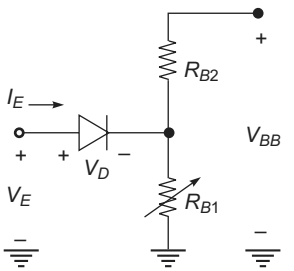


Fig. 15.22 *Circuit equivalent of UJT*

This ratio (η) is controlled by the location of the aluminium rod (Fig. 15.21). The emitter firing potential is given by

$$V_P = \eta V_{BB} + V_D \tag{15.15}$$

The static characteristic of a typical UJT is shown in Fig. 15.23 for V_{BB} = 10 V, wherein the various regions are indicated. As V_E crosses V_P, the emitter fires and holes are injected into the slab from the *P*-type aluminium rod. This causes increase in the hole content of the *N*-type slab with consequent increase in the number of free electrons in it, and so, increased conductivity. Thus, V_E drops off while I_E increases. This is

the negative resistance region of the *UJT*, which passes through the valley point (I_V, V_V), while the devices get saturated.

Three important parameters of a UJT are I_P, V_V and I_V. As V_{BB} increases, it causes V_P to increase [as per Eq. 15.15].

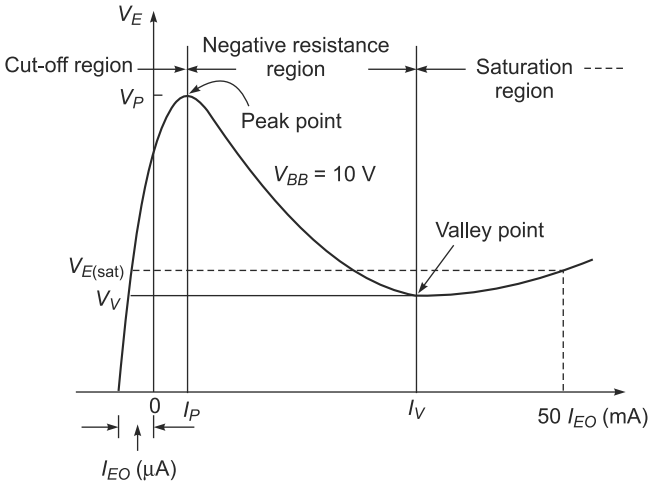


Fig. 15.23 *UJT static emitter characteristic*

15.6 DC BIASING

It has been seen above that for BJT operation, certain dc levels must be set by dc sources (batteries). This process is called biasing the BJT. The biasing locates an operating point, also called *quiescent point* (*Q*), on the characteristics, about which signal-caused variation takes place [ac input causing ac output suitably modified (amplified)]; dc biasing and ac analysing can be carried out separately (results superimposed if necessary). In order to isolate the ac signals from dc sources, isolating capacitors are used, which act as short circuits for ac signals. From the signal point of view, these are coupling capacitors. We shall now proceed to analyse and design the dc biasing which determines the location of the *Q*-point appropriately.

An important requirement of the biasing circuit is its insensitivity to BJT's parameter changes due to temperature, i.e. a stable *Q*-point.

Fixed Bias

The fixed bias circuit is drawn in Fig. 15.24 with a single battery source. The collector characteristics are drawn in Fig. 15.25. The *Q*-point is to be located on the characteristic

$$I_B = I_{BQ} \text{ as shown in Fig. 15.25.}$$

KVL equation for *BE* loop

$$V_{CC} - R_B I_{BQ} - 0.7 \text{ V} = 0;\ V_{BE} = 0.7 \text{ V} \tag{15.16}$$

$$I_{BQ} = \frac{V_{CC} - 0.7}{R_B} \tag{15.17}$$

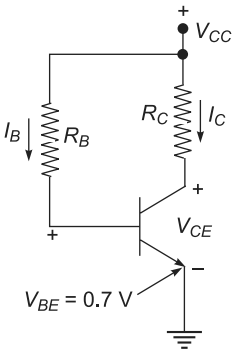


Fig. 15.24 *Fixed bias*

Load Line

KVL equation for the collector loop is

$$V_{CC} - R_C I_C - V_{CE} = 0 \qquad (15.18)$$

or $$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

It is a straight line in $I_C - V_{CE}$ coordinates.

Along V_{CE} axis. $I_C = 0$; intercept on V_{CE} – axis is

$$V_{CE} = V_{CC}$$

Along I_C axis, $V_{CE} = 0$, intercept on I_C – axis

$$I_C = \frac{V_{CC}}{R_C}$$

The line joining these two intercepts is the *load line* drawn on the collector characteristics. It intersects the characteristics for I_{BQ} at the operating point Q.

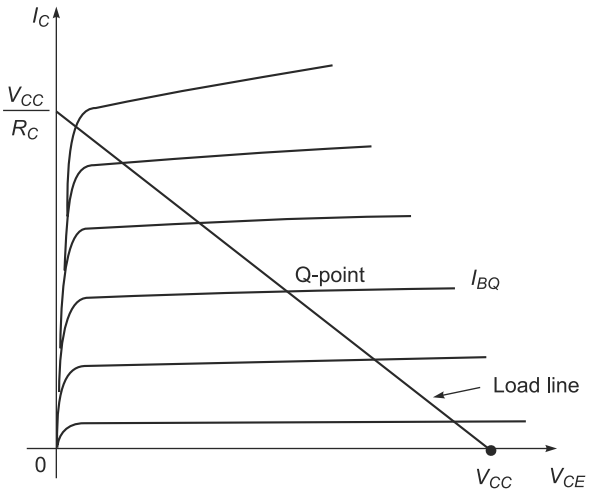


Fig. 15.25 *Location of Q-point*

By adjusting I_B (by R_B) and R_E, the Q-point can be located anywhere. If I_B is increased, the Q-point moves up along the load line. If R_C is increased, the load line slope, starting from V_{CC}, decreases and the Q-point moves on I_{BQ} characteristic to the left side.

The fixed bias cannot counter the thermal effect on the BJT characteristics. As β rises with temperature, collector characteristics shift upwards as $I_C \approx \beta I_B$. Correspondingly, the Q-point moves up on the load line.

This deteriorates the BJT's performance.

15.6.1 Bias Stabilisation by Emitter Resistance (Self-Bias)

The fixed-bias circuit of Fig. 15.24 is modified to include a small resistance R_E in the emitter by as shown in Fig. 15.26. The circuit also shows coupling capacitors (C_c) which are open circuit for dc.

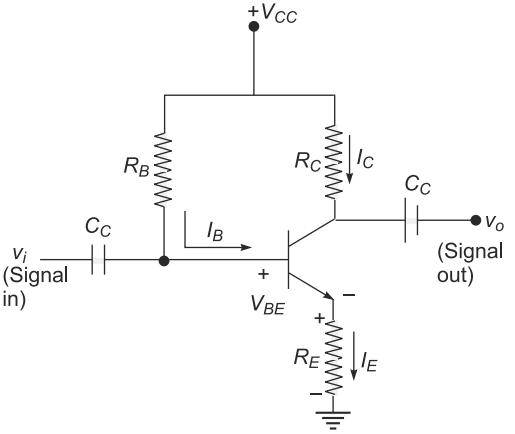


Fig. 15.26 *Fixed-bias circuit*

The emitter includes voltage drop $R_E J_{E,}$ which acts as negative feed to stabilise the bias (Q-point).

$$I_E = I_B + I_C = I_B + \beta I_B = (1 + \beta) I_B$$

Base-emitter loop

$$V_{CC} - R_B I_B - 0.7 - [(1 + \beta)R_E] I_B = 0 \tag{15.19}$$

$$I_B = \frac{V_{CC} - 0.7}{R_B + (1+\beta) R_E} \tag{15.20}$$

Any increase in β reduces I_B slightly as $R_B >> R_E$.

Corresponding $I_C = \beta I_B$ increases to compensate the shift in Q-point. So there is no significant shift in Q-point, which has been stabilised by inclusion of R_E.

15.6.2 Voltage-Divider Bias

The voltage-divider bias circuit is drawn in Fig. 15.27(a) wherein bias voltage is applied to the base from the voltage-divider resistances R_1. R_2 and self-bias emitter resistance is also included.

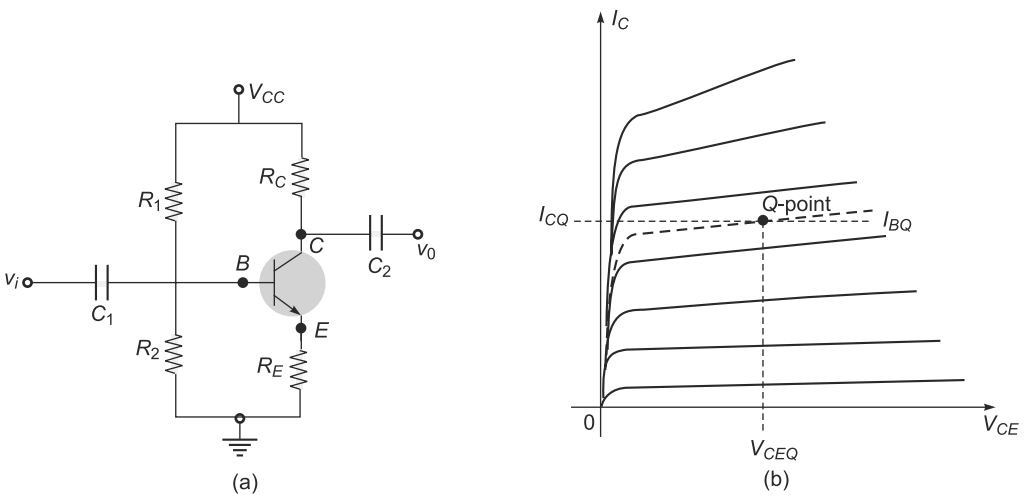


Fig. 15.27 *(a) Voltage-divider bias circuit (b) Q-point remains almost unchanged*

It can be shown by exact analysis that the sensitivity of the Q-point to changes in β is quite small by proper design of circuit parameters. If β changes, the level of I_{BQ} will change because of the negative feedback effect of R_E but the collector characteristics also change accordingly. As a result, the operating point defined by I_{CQ} and V_{CEQ} remains changed.

15.6.3 Analysis Equations

The Thevenin equivalent seen at B

$$V_{\text{th}} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} \tag{15.21}$$

Thevenin resistance

$$R = R_1 \| R_2 \tag{15.22}$$

The biasing circuit is redrawn in Fig. 15.28.

As $$I_E = (1 + \beta)\, I_B \tag{15.23}$$

we find from the *BE* loop

$$I_B = \frac{V_{\text{th}} - 0.7}{R_{\text{th}} + (1+\beta)R_E} \tag{15.24}$$

From the emitter bias KVL, we have

$$V_{CE} = V_{CC} - (R_C + R_E)\, I_C;\ I_E \approx I_C \tag{15.25}$$

These equations are sufficient to determine all voltages and currents after the choice of V_{CC} and I_{CQ} and V_{CEQ} from the collector characteristics by locating a *Q*-point.

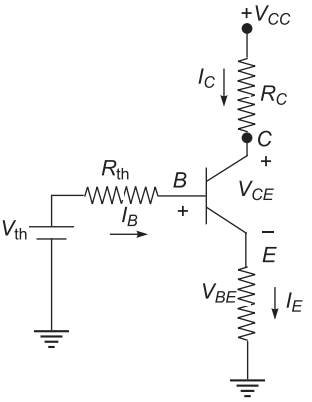


Fig. 15.28 *Biasing circuit*

15.6.4 Voltage Feedback Bias

The emitter self-bias circuit of Fig. 15.26 is modified by voltage feedback to base from V_C collector voltage instead of V_{CC} as drawn in Fig. 15.28.

Writing the KVL equations for *BE* and *CE* loops and recognising $I_B = I_E - I_C$, we can obtain the following result $(1 + \beta \approx \beta)$

$$I_B = \frac{(V_{CC} - 0.7) = V'}{R_B + \beta(R_C + R_E)} \tag{15.26}$$

It is further found that

$$I_{CQ} = \frac{\beta V'}{R_B + \beta R'};\ R' = R_C + R_E \tag{15.27}$$

As $\beta R' >> R_B$,

$$I_{CQ} = \frac{V'}{R'}, \text{ Independent of } \beta \tag{15.28}$$

In fact, Eq. (15.26) is the general form of the I_B equation for the biasing circuits presented. Voltage feedback bias is somewhat better than emitter self-bias because of additional voltage feedback. *But the voltage-divider bias is the best of all the schemes of BJT bias and is universally adopted.*

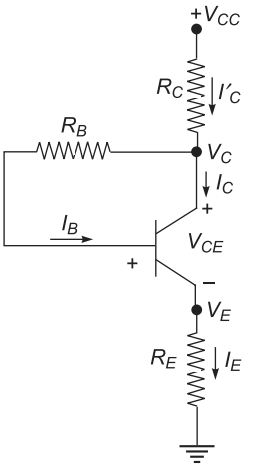


Fig. 15.29 *Voltage feedback bias*

***Remark*:** In order that emitter resistance R_E does not affect the ac performance, it should be shunted by a capacitor called *bypass capacitor*.

***I*$_C$(sat):** To gauge how far the *Q*-point is from saturation, we need to find I_C(sat). BJT saturates at $V_{CE} = 0.2$ V, see Fig. 15.10. It can be assumed that in saturation $V_{CE} = 0$, with $R_E = 0$,

$$I_C(\text{sat}) = \frac{V_{CC}}{R_C} \tag{15.29}$$

Example 15.1

In a BJT, the emitter current is 8 mA and $I_B = I_C/100$. Determine I_C and I_B.

Solution

$$I_E = I_C + I_B$$

$$I_E = I_C + \frac{1}{100} I_C = \frac{101}{100} I_C$$

$$I_C = 8 \times \frac{1}{101} = 7.92 \text{ mA}$$

$$I_B = \frac{1}{100} I_C = 0.0792 \text{ mA}$$

Example 15.2

Given $\alpha_{dc} = 0.997$, (a) determine I_C if $I_E = 5$ mA, (b) determine α_{dc} if $I_E = 2.8$ mA and $I_B = 20$ μs, and (c) find I_E if $I_B = 40$ μA and $\alpha_{dc} = 0.98$.

Solution

(a) $I_C = \alpha_{dc} I_E$; I_{CBO} neglected

$$I_C = 0.997 \times 5 = 4.985 \text{ mA}$$

(b) $$I_E = I_C + I_B$$

$$(1 - \alpha_{dc}) I_E = I_B$$

$$1 - \alpha_{dc} = \frac{20 \times 10^{-3}}{2.8}$$

$$\alpha_{dc} = 0.993$$

(c) $$I_B = (1 - \alpha_{dc}) I_E$$

$$I_E = \frac{40 \times 10^{-3}}{(1 - 0.98)} = 2 \text{ mA}$$

Example 15.3

Refer characteristics of Fig. 15.10.

(a) Find I_C corresponding to $V_{BE} = +750$ mV, $V_{CE} = +5$ V.

(b) Find V_{CE} and V_{BE} corresponding to $I_C = 3$ mA and $I_B = 30$ μA.

Solution

From Fig. 15.10(b), at $V_{BE} = 0.75 \text{ V} \times I_B = 40$ μA
From Fig. 15.10(a) at $I_B = 40$ μA, $V_{CE} = 5$ V, $\times I_C = 4$ mA

Example 15.4

Using the collector characteristics of Fig. 15.10(a), determine

(a) β_{dc} at $I_B = 80$ μA and $V_{CE} = 5$ V

(b) Repeat part (a) at $I_B = 30$ mA and $V_{CE} = 10$ V

Solution

(a) We find from Fig. 15.10(a) at $I_B = 80$ mA, $V_{CE} = 5$ A

$$I_C = 6.7 \text{ mA}$$

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{6.7}{80 \times 10^{-3}} = 83.75$$

(b) $I_B = 30\ \mu A.\ V_{CE} = 10\ V$

$$\beta_{dc} = \frac{3.4}{30 \times 10^{-3}} = 113.3$$

***Remark*:** $\beta_{dc} = 113.3$ is the proper value for use as it lies in the linear part of active region.

Example 15.5

On the common-emitter collector characteristics of Fig. 15.10(a), locate the operating point at $V_{CE} = 10$ V and $I_C = 2$ mA.

(a) Find the value of α for this operating point.

(b) Find the value of β for this operating point.

(c) At $V_{CE} = 10$ V read the corresponding V_{CEO}.

(d) Calculate the corresponding value of V_{CBO}.

Solution

(a) The operating point is located at Q in Fig. 15.10(a)

$$I_C = 2\ mA,\ I_B = 16\ \mu A$$

$$I_E = I_C + I_B$$

$$\frac{1}{\alpha} I_C = I_C + I_B$$

$$\left(\frac{1}{\alpha} - 1\right) I_C = I_B \text{ or } \left(\frac{1}{\alpha} - 1\right) = \frac{I_B}{I_C} = \frac{16 \times 10^{-3}}{2}$$

$$\alpha = 0.992$$

(b) $$\beta = \frac{I_C}{I_B} = \frac{2}{16 \times 10^{-3}} = 125$$

(c) At $V_{CE} = 10$ V, $I_{CEO} = 0.4$ mA

(d) $$I_{CEO} \approx \beta . T_{CBO}$$

$$I_{CBO} = \frac{0.4}{125} \times 10^3 = 3.2\ \mu A$$

Example 15.6

For the transistor circuit of Fig. 15.30,

$V_{BB} = V_{CC} = 10$ V. $\beta = 100$

Calculate (a) I_B, (b) I_C, (c) V_{CE}, and (d) V_{CB}.

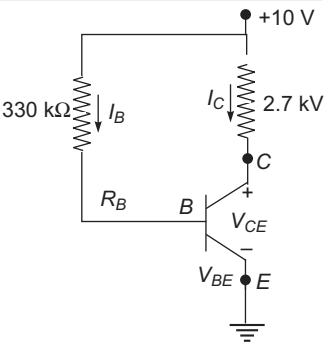


Fig. 15.30

Solution

Assume active mode.

BE conducts with $V_{BE} = 0.7$ (remains constant)

(a) $$I_B = \frac{10 - 0.7}{330} = 0.028\ mA$$

(b) $I_C = \beta I_B = 2.8$ mA

(c) $V_{CE} = 10 - 2.7 \times 2.8 = 2.44\ V > 0.2\ V = V_{CE(sat)}$, active mode

(d) $V_{CB} = V_{CE} - V_{BE} = 2.44 - 0.7 = +1.74$ V, reverse bias; active mode

Remark: $V_{CB} > 0.5$ V (cut-in voltage) for active mode

Correspondingly,

$V_{CE} = V_{CB} + V_{BE} = -0.5 + 0.7 = 0.2 \text{ V} = V_{CE(\text{sat})}$

Example 15.7

For the fixed-bias configuration of Fig. 15.31, determine the following at quiscent point: (a) I_B, I_C, V_{CE} (b) V_C, V_B, V_E (c) V_{CB}

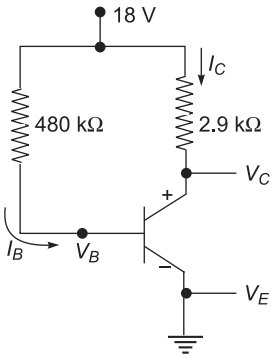


Fig. 15.31 $\beta = 95$

Solution

(a) $$I_B = \frac{18 - 0.7}{480} = 36 \text{ μA}$$

$$I_C = 95 \times 36 = 3.42 \text{ mA}$$

$$V_{CE} = 18 - 2.9 \times 3.42 = 8.08 \text{ V}$$

(b) $$V_C = 8.08 \text{ V},$$

$$V_B = 0.7 \text{ V},$$

$$V_E = 0$$

(c) $$V_{CB} = 8.08 - 0.7 = 7.38 \text{ V, reverse biased (OK)}$$

Example 15.8

For the emitter-stabilised BJT bias circuit of Fig. 15.32, determine I_{BQ}. I_{CQ}, V_{CEQ}, V_B, V_C, V_E.

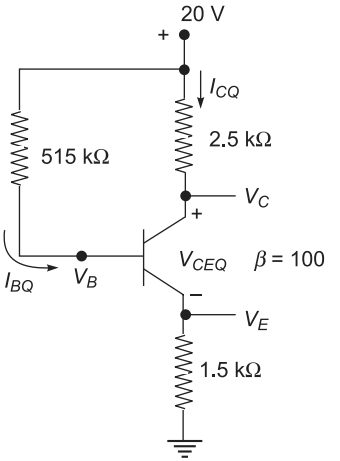


Fig. 15.32

Solution

$$I_{BQ} = \frac{(20 - 0.7) \times 10^3}{515 + (1 + 100) \times 1.5}$$

$$= 29 \text{ μA}$$

$$I_{CQ} = 100 \times 29 \times 10^{-3}$$

$$= 2.9 \text{ mA}$$

$$V_{CEQ} = 20 - 2.9 \times 2.5 - 2.9 \times 1.5 \qquad (I_E \approx I_{CQ})$$

$$= 8.4 \text{ V}$$

$$V_C = 20 - 2.9 \times 2.5$$

$$= 12.75 \text{ V}$$

$$V_E = 2.9 \times 1.5$$

$$= 4.35 \text{ V}$$

Example 15.9

For the voltage-divider bias circuit of Fig. 15.33, determine I_{RQ}, I_{CQ}, V_{CEQ}, V_C, V_E, V_B.

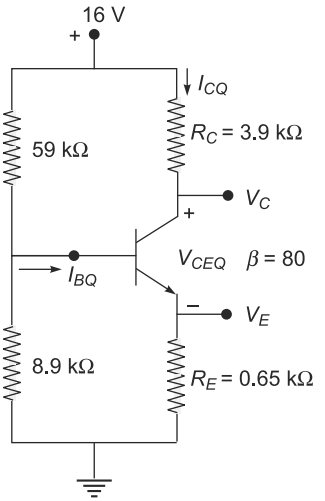


Fig. 15.33 $\beta = 80$

Solution

Thevenin equivalent as seen from the base

$$V_{th} = \left(\frac{8.9}{59 + 8.9}\right) \times 16 = 2.1 \text{ V}$$

$$R_{th} = \frac{59 \times 8.9}{59 \times 8.9} = 7.73 \text{ k}\Omega$$

The circuit is now drawn in Fig. 15.34.

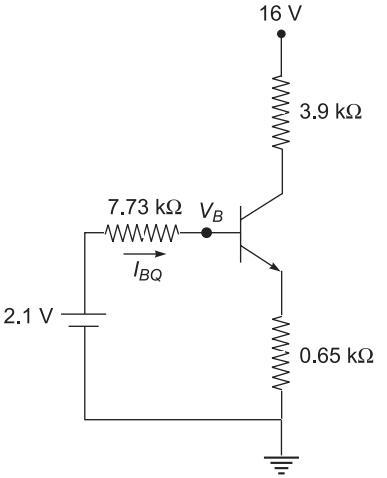


Fig. 15.34

$$I_{BQ} = \frac{(2.1 - 0.7) \times 10^3}{7.73 + (1 + 80) \times 0.65} = 23.2\ \mu A$$

$$I_{CQ} = 80 \times 23.3 \times 10^{-3} = 1.856\ mA$$

CE loop KVL equation

$$16 - 3.9\ I_{CQ} - V_{CEQ} - 0.65\ I_{EQ} = 0$$

$$16 - 3.9 \times 1.805 - V_{CEQ} - 0.65 \times 1.865 = 0$$

$$V_{CEQ} = 7.51\ V$$

$$V_C = 16 - 3.9 \times 1.856 = 8.76\ V$$

$$V_E = 8.76 - 7.51 = 1.25\ V$$

$$V_B = 1.25 + 0.7 = 1.95$$

Check

$$V_B = 2.1 - 7.73 \times 23.2 \times 10^{-3} = 1.92\ V\ (OK)$$

Example 15.10

For the voltage feedback circuit of Fig. 15.35, determine I_B, I_C, V_C.

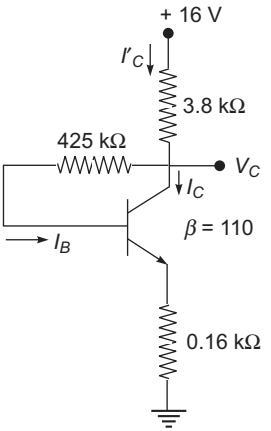


Fig. 15.35

Solution

$$I'C = \frac{16 - V_C}{3.8} = I_B + I_C$$

or $$16 - V_C = 3.8\ I_B + 3.8\beta\ I_B$$

or $$V_C = 16 - 3.8\ (8 + 110)\ I_B \quad \text{(i)}$$

$$V_C = 16 - 421.8\ I_B \quad \text{(ii)}$$

BE loop KVL

$$V_C = 425\ I_B - 0.7 - 0.61\ (1 + 110)\ I_B = 0$$

$$V_C = (425 + 67.7)\ I_B - 0.7 \quad \text{(i)}$$

$$V_C = 492.7\ I_B - 0.7 \quad \text{(ii)}$$

From Eqs (i) and (ii)

$$16 - 421.8\ I_B = 492.7\ I_B - 0.7$$

$$914.5\ I_B = 16.7$$

$$I_B = 18.26\ mA$$

$$I_C = \beta I_B = 110 \times 18.26 \times 10^{-3} = 2\ mA$$

From Eq (ii),

$$V_C = 492.7 \times 18.26 \times 10^{-3} - 0.7 = 8.3\ V$$

Check

$$I'_C = I_C + I_B = 111\ I_B = 111 \times 18.26 \times 10^{-3} = 2.027\ mA$$

$$V_C = 16 - 3.8 \times 2.027 = 8.29\ V\ (OK)$$

Example 15.11

The collector characteristics of a BJT are drawn in Fig. 15.36.

(a) Locate an operating point midway between the active region.

(b) What are the values of I_{CQ} and V_{CEQ}?

(c) Determine the value of R_B to establish this operating point for fixed-bias configuration. Calculate P_{CQ}, given V_{CC} = 20 V.

(d) Calculate the value of β and α at the operating point.

(e) What is the value of the saturation current , $I_{C(sat)}$.

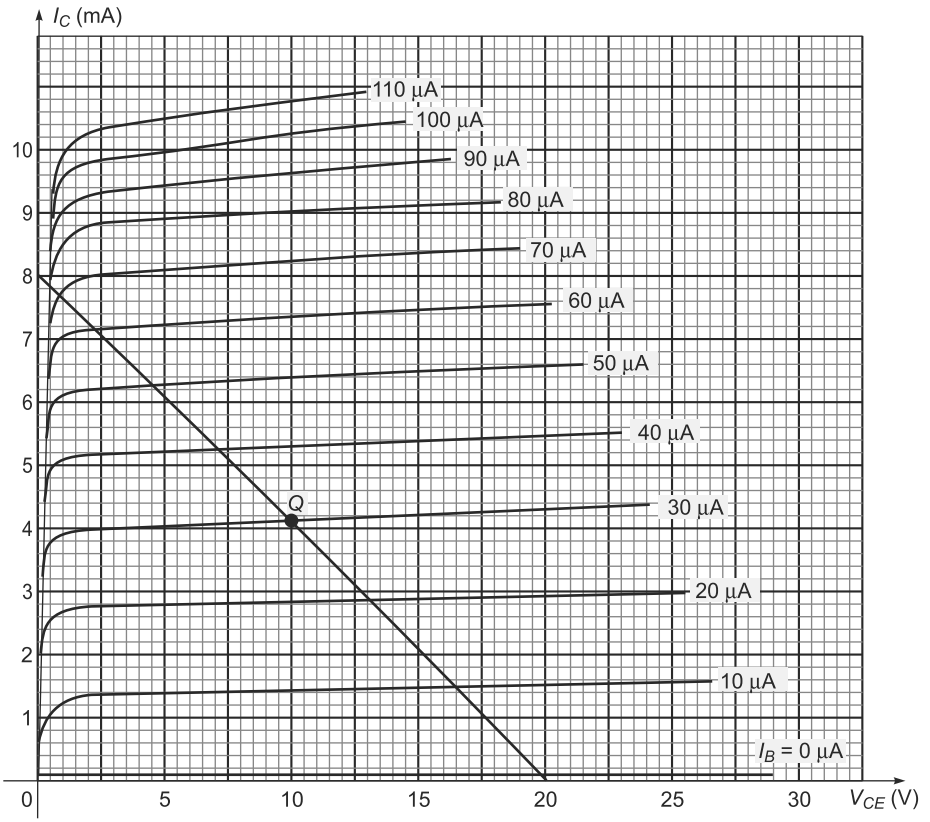


Fig. 15.36

Solution

(a) and (b) Q-point is located on Fig. 15.36 where

$$I_{CQ} = 4.1 \text{ mA}, V_{CEQ} = 10 \text{ V}, I_{BQ} = 30 \text{ μA}$$

(c) From $V_{CE} = V_{CC} = 20$ V, draw a line through Q which intersect

I_C = axis at $I_C = 8$ mA

$$\frac{V_{CC}}{R_C} = 8 \text{ mA} \rightarrow R_C = \frac{20}{8} = 2.5 \text{ k}\Omega$$

(d) $$R_B = \frac{20 - 0.7}{30 \text{ μA}} = 643 \text{ k}\Omega$$

(e) $I_{C\,(\text{sat})} \approx 10$ mA

Summary

➢ BJT is introduced with constructional details its operational characteristics and configurations explained. SCR and UJT introduced with their characteristics and biasings.

Exercises

Review Questions

1. Comment on the doping levels of the three components of a BJT.
2. Why is the base layer of a BJT made very thin compared to emitter and collector layer?
3. What are the three regions of operation of a BJT. Explain with help of *CE* configuration collector characteristics.
4. In the three regions of operation how are the BJT junctions biased?
5. Define α of a BJT.
6. Define β of a BJT.
7. How are α and β related?
8. Distinguish between α_{dc} and α_{ac}
9. Distinguish between β_{dc} and β_{ac}.
10. What is reverse saturation current in a BJT? How can this be observed independently?
11. Draw the symbols for *pnp* and *npn* BJT. What distinguishes one from the other?
12. How are I_{CBQ} and I_{CEO} related?
13. What is meant by biasing a transistor?
14. What is self-bias? How does it help in stabilising the *Q*-point?
15. Draw the circuit of a voltage-divider bias.
16. What is voltage feedback bias? Draw the circuit. Is this type of bias almost independent of β?
17. What is meant by β insensitive bias?

Problems

1. For common-base configuration for $V_{BE} = 0.7$ V, I_E is adjusted to 5 mA. What is I_C? Does it depend on V_{CB} in the active region. The collector characteristics are drawn in Fig. 15.8.
2. For the common emitter configuration, $I_B = 30$ mA, $V_{CE} = 7.5$ V.
   (a) Calculate β_{dc} and β_{ac}.
   (b) Find the value of I_E.
   (c) Find the change in I_E for $\Delta I_B = +5$ μA.
   The collector characteristics are drawn in Fig. 15.10 (a).
3. From the collector characteristics of Fig. 15.10(a), the operating point is at $I_B = 20$ μA and $V_{CE} = 10$ V. Calculate α_{dc} and the corresponding I_E.

4. A BJT is connected in *CE* configuration as in Fig. 15.37; *BJT* $\beta = 100$.

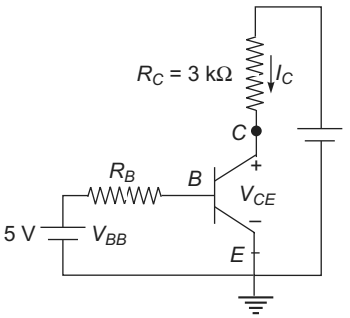


Fig. 15.37

Determine
(a) I_B (b) I_C (c) V_{CE} (d) V_{CB} assuming the transistor to be in active region. Check from the value of V_{CB} if it is so.
Hint: *CB* junction should be reverse biased.

5. For the fixed-bias configuration of Fig. 15.38, determine R_B, R_C, I_C, V_{CE}.
6. For the emitter-stabilised bias circuit of Fig. 15.39, determine R_B, R_C, R_E and V_B.

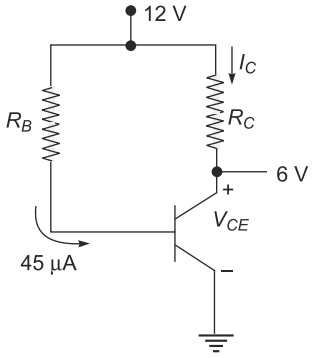


Fig. 15.38 $\beta = 100$

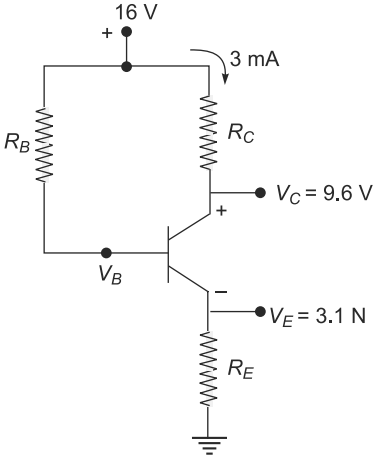


Fig. 15.39 $\beta = 80$

7. For the voltage-divider bias circuit of Fig. 15.40, determine I_C, V_E, V_{CC}, V_B, R_1.
8. For the voltage feedback network of Fig. 15.41, determine V_E, I_C, V_C, V_{CE}, I_B, β.

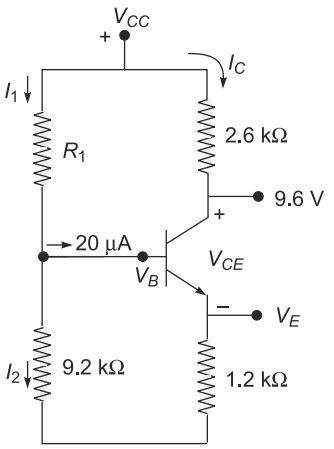


Fig. 15.40 $\beta = 101$

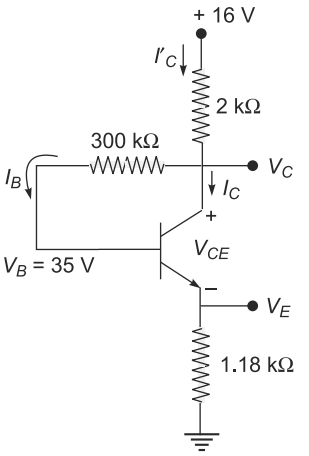


Fig. 15.41

9. For the network of Fig. 15.42, determine
I_E, V_C, V_{CE}

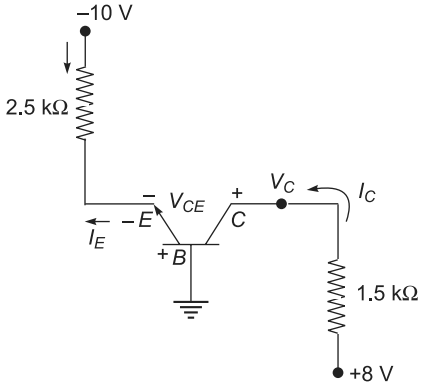


Fig. 15.42

Multiple-Choice Questions

1. Current gain of BJT in common base is
   (a) α (b) β (c) γ (d) none of these
2. An SCR device has
   (a) four layers (b) three layers (c) two layers (d) one layer
3. A UJT device has
   (a) four layers (b) three layers (c) two layers (d) none of these
4. The value of total collector current in a *CB* circuit is
   (a) $I_C = \alpha I_E + I_{CO}$ (b) $I_C = \alpha I_E$ (c) $I_C = \beta I_E$ (d) $I_C = \alpha I_{CO} - I_E$

5. When the collector junction in transistors is biased in the reverse direction and the emitter junction in forward directions, the transistor is said to be in the
   (a) cut-off region (b) saturation region (c) active region (d) none of these
6. Which of the following acts like a diode and two transistors?
   (a) UJT (b) SCR (c) TRIAC (d) DIAC
7. Early effect in BJT refers to
   (a) avalanche breakdown (b) zener breakdown
   (c) base narrowing (d) none of these
8. In a BJT, largest current flows
   (a) in the base (b) in the emitter (c) in the base and emitter (d) in the collector
9. The "cut-in" voltage of a silicon small-signal transistor is
   (a) 0.5 V (b) 0.3 V (c) 1.0 V (d) 0.9 V
10. An SCR consists of
   (a) five *PN* junctions (b) two *PN* junctions (c) four *PN* junctions (d) three *PN* junctions

Answers

Problems

1. $I_C \approx 5$ mA, no
2. $\beta_{dc} = 113$ $\beta_{ac} \approx 100$
3. $\alpha_{dc} = 0.992$, $I_E = 2.4$ mA
4. (a) 21.5 μA (b) 2.15 mA (c) +2.85 V
5. $R_B = 251$ kΩ, $I_c = 4.5$ mA, $R_c = 1.33$ kΩ, $V_{CE} = 6$ V
6. $R_C = 2.13$ kΩ, $R_E = 1.03$ kΩ, $R_B = 324.6$ kΩ, $V_b = 3.83$ V
7. $I_C = 2$ mA, $V_{CC} = 14.8$ V, $V_E = 2.4$ V, $V_B = 3.1$ V, $R_1 = 32.8$ kΩ
8. $V_E = 2.74$ V, $I_C = 2.32$ mA, $V_c = 12.3$ V, $V_{CE} = 9.56$ V, $I_B = 4$ μA
9. $I_E = 3.72$ mA, $V_C = 2.42$ V, $V_{CE} = 3.12$ V

Multiple-Choice Questions

1. (a) 2. (a) 3. (b) 4. (a) 5. (c)
6. (a) 7. (c) 8. (b) 9. (a) 10. (d)

Field Effect Transistors (FETs)

chapter 16

Goals & Objectives

- Introduction of field effect transistors(FETs)
- Construction and characteristics of JFETs
- Constructional features and analysis of metal oxide field effect transistors(MOSFET)
- Explanation of FET circuit configurations, CMOS circuits and FET biasing

16.1 INTRODUCTION

Like BJTs, FETs are three-terminal devices. These differ from BJTs in two respects.

- While BJT is a current-controlled device (input I_B controls output I_C), FET is voltage-controlled device (input voltage controls output current)
- BJT is bilateral while FET is unilateral, which means that only one type of carrier participates in conduction.

FETs are of two types: Junction Field Effect Transistor (JFET) and Metal Oxide Semiconductor Field-Effect Transistor (MOSFET).

16.2 JFETs

16.2.1 Construction and Characteristics

An *N*-type material channel forms the major part of the structure. It is embedded on both sides with *P*-type material as shown in Fig. 16.1 (*N* and *P* could be interchanged). The two *P*-type materials through ohmic contacts are joined together and connected to the terminal gate (*G*).

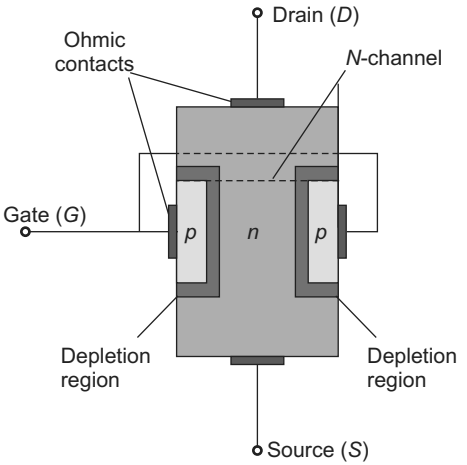


Fig. 16.1 *Junction Field Effect Transistor (JFET) N-channel*

The *N* and *P* materials form *PN*-junctions on the two sides of the channel. The top of the *N*-channel makes ohmic contact with the terminal. Drain (*D*) and the lower end of the channel makes ohmic contact with the terminal source (*S*). Around both the *PN*-junctions there is the depletion region (like in a diode).

Operation with $V_{GS} = 0$ and $V_{DS} > 0$ (variable)

Connection Diagram

In Fig. 16.2, voltage $V_{DS} > 0$ is applied across the *DS* terminals, V_{DS} can be varied by the source V_{DD}. The gate terminal *G* is connected to the source terminal *S* so that $V_{GS} = 0$. V_{DS} causes the channel electrons to flow from *S* to *D*, the conventional current I_D flows into *D* and I_S flows out of *S*; obviously, $I_D = I_S$.

16.2.2 Operation

The voltage V_{DS} reverse biases both the *PN*-junctions. The reverse biasing reduces towards the *S* terminal because of voltage drop in the channel from *D* to *S*. As a result, the depletion region widens at the *D*-end

of the channel. The width of depletion region reduces along the channel towards the *S*-end. The depletion region is therefore non-uniform as shown in Fig. 16.2. As V_{DS} is increased from zero, I_D increases. As the channel width is decreasing with increase of V_{DS}, I_D begins to level off as shown in Fig. 16.3. At $V_{DS} = V_p$ (called pinch-off voltage), I_D becomes constant and I_{DSS}, the saturation level, becomes independent of V_{DS}. The initial behaviour of the channel is that of voltage-controlled resistance.

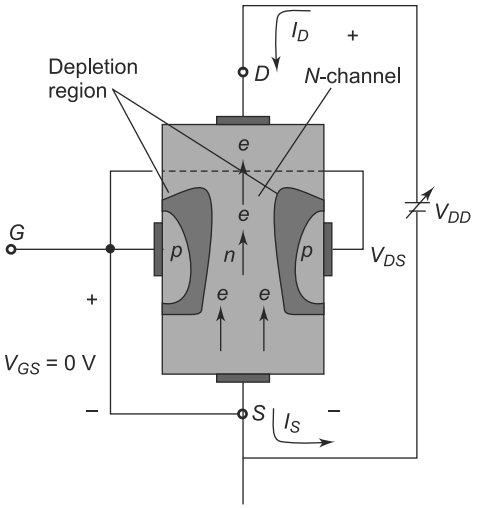


Fig. 16.2 *Connection diagram of JFET, $V_{GS} = 0$, $V_{DS} > 0$*

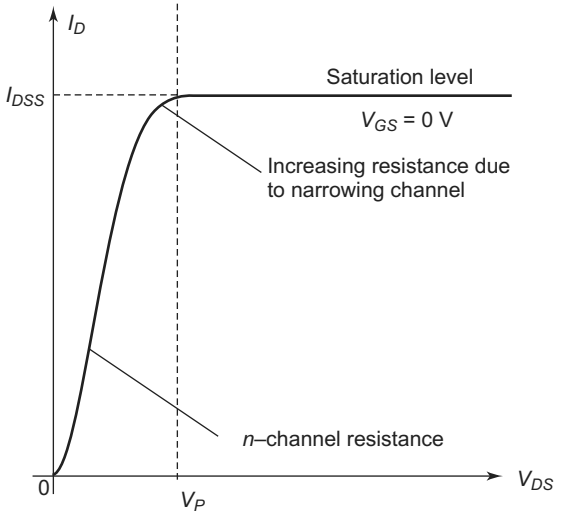


Fig. 16.3 *JFET characteristic; $V_{GS} = 0$, V_{DS} increasing*

Operation $V_{GS} < 0$, $V_{DS} > 0$, Both Variable

A voltage source is connected between the gate *G* and source *S* terminals causing V_{GS} to be negative as shown in Fig. 16.4. This negative V_{GS} reverse biases both the junctions uniformly reducing the channel

width throughout. This is over and above the effect of V_{DS}. The channel therefore pinches off at value $V_{DS} < V_P$ for $V_{GS} = 0$ as shown in Fig. 16.5. The pinch-off values of V_{DS} continue to decrease as V_{GS} is made more negative. At a value of $V_{GS} = V_P$(–4 V in Fig. 16.5), the channel completely closes and so $I_D = 0$ irrespective of the value of V_{DS}. Then pinch-off is caused by negative V_{GS} (= V_P).

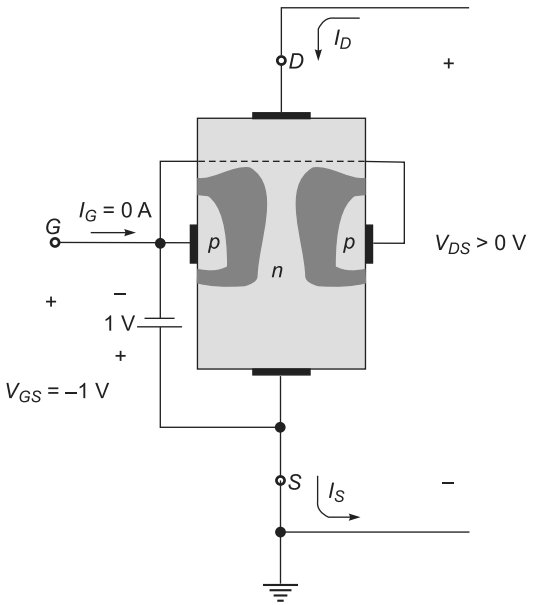


Fig. 16.4 *$V_{GS} < 0$, $V_{DS} > 0$, both variable*

The complete characteristics (typical) are drawn in Fig. 16.5. It is to be noted that as the two junctions are reverse biased, $I_G \approx 0$.

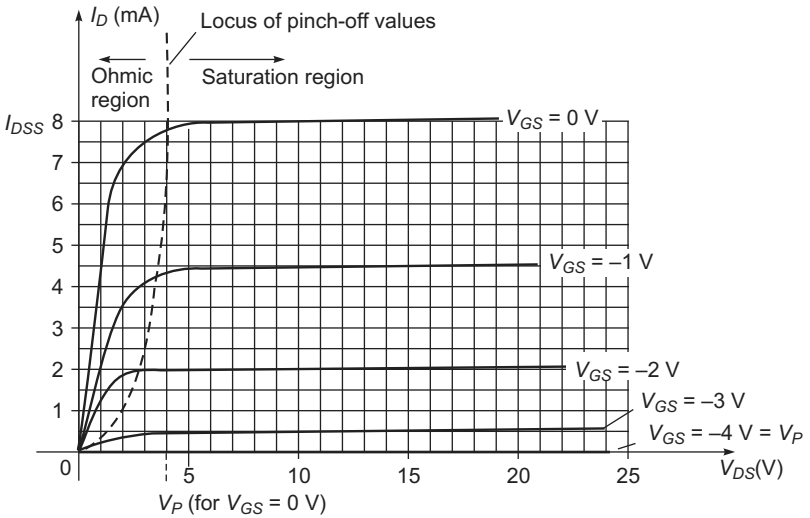


Fig. 16.5 *N-Channel JFET characteristics with I_{DSS} = 8 mA and V_P = –4 V*

Symbols

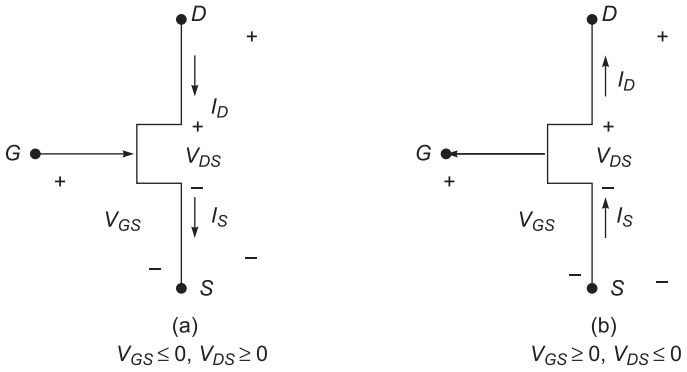


Fig. 16.6 *(a) n-channel JFET (b) p-channel JFET*

16.2.3 Voltage-controlled Resistance

It is observed from the characteristics of Fig. 16.5 that the characteristics are linear (almost) to lie left of the V_P locus. It is further observed that the slope decreases as V_{GS} increases. It means that the JFET acts as voltage-controlled resistance; and resistance increases with V_{GS}. To a good approximation, the resistance offered by JFET in the ohmic region can be expressed as

$$r_d = \frac{r_0}{(1 - V_{GS}/V_P)^2} \tag{16.1}$$

where r_0 = resistance with $V_{GS} = 0$
r_d = drain resistance

16.2.4 Transfer Characteristic

It is observed from the characteristics of Fig. 16.5 that the characteristics to the right of V_P locus, the saturation region (the major part of the characteristics), that I_D is dependent on V_{GS} but is independent of V_{DS}. For any value of V_{DS}, (preferably in the middle), we can read I_D for various values of V_{GS} (from zero to V_P) and plot I_D vs V_{GS} as shown in Fig. 16.7. This plot is known as the transfer characteristic [it transfers V_{GS} (input) to I_D (output)]. That is why JFET is a voltage-controlled device in which input voltage controls the output current.

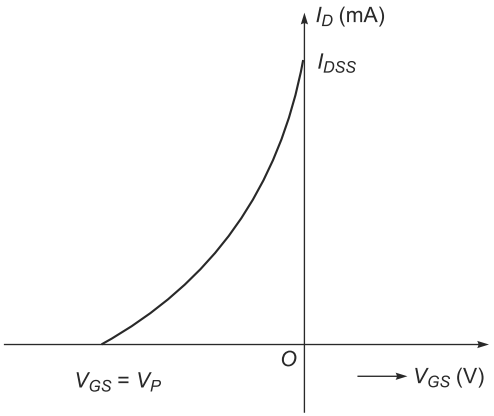


Fig. 16.7 *Transfer characteristics*

16.2.5 Shockley's Equation

The transfer characteristic can be expressed analytically as

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \tag{16.2}$$

At $V_{GS} = 0$, $I_D = I_{DSS}$ and at $V_{GS} = V_P$. $I_D = 0$

Equation (16.2) can be written in the form to determine V_{GS} for given I_D as

$$V_{GS} = V_P\sqrt{1-\frac{I_D}{I_{DSS}}} \tag{16.3}$$

Example 16.1

From the drain characteristics of JFET (*N*-channel) of Fig. 16.5, read I_{DSS}, V_P. Using Shockley's equation, check the values of I_D for $V_{GS} = -1$ and $V_{GS} = -2$.

Solution From the figure, $I_{DSS} = 8$ mA, $V_P = -4$ V

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

At $V_{GS} = -1$ V,

$$I_D = 8\left(1-\frac{-1}{-4}\right)^1 = 8\times\left(\frac{3}{4}\right)^2 = \frac{9}{2} = 4.5 \text{ mA (checks)}$$

At $V_{GS} = -2$ V,

$$I_D = 8\left(1-\frac{2}{4}\right)^2 = 8\times\frac{1}{4} = 2 \text{ mA (checks)}$$

Example 16.2

From the drain characteristics of Fig. 16.5, write down the progressive difference in I_D against the difference $n\ V_{GS}$. What is the nature of their relationship?

Solution

ΔV_{GS} (V)	ΔI_D(A)
–1	0.5
–1	1.5
–1	2.5
–1	3.5

The relationship in nonlinear.

Example 16.3

At a *Q*-point of JFET, $I_{OQ} = 3.5$ mA and $V_{GS} = -3$ V; determine I_{DSS} if $V_P = -6$ V.

Solution

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$3.5 = I_{DSS}\left(1 - \frac{-3}{-6}\right)^2 = \frac{1}{4} I_{DSS}$$

or $$I_{DSS} = 3.5 \times 4 = 14 \text{ mA}$$

Example 16.4

For JFET, I_{DSS} = 6 mA, V_P = −4.5 V

Determine

(a) I_D at V_{GS} = −2 and −4 V

(b) V_{GS} at I_D = 3 and 5.5 mA

Solution

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

(a) (i) $$I_D = 6\left(1 - \frac{-2}{-4.5}\right)^2 = 1.85 \text{ mA}$$

(ii) $$I_D = 6\left(1 - \frac{-4}{-4.5}\right)^2 = 0.074 \text{ mA}$$

(b) (i) $$3 = 6\left(1 - \frac{V_{GS}}{-4.5}\right)^2$$

$$0.5 = (1 + 0.222\ V_{GS})^2$$

$$1 + 0.222\ V_{GS} = \pm 0.707$$

$$0.222\ V_{GS} = -1.707, -0.293$$

$$V_{GS} = -1.32 \text{ V}, -7.73 > V_P \text{ rejected}$$

(ii) $$5.5 = 6(1 + 0.222\ V_{GS})^2$$

$$0.917 = (1 + 0.222\ V_{GS})^2$$

$$1 + 0.222\ V_{GS} = \pm 0.957$$

$$0.222\ V_{GS} = -0.043, -1.957$$

$$V_{GS} = -0.194 \text{ V}$$

Example 16.5

For the JFET drain characteristics of Fig. 16.8, determine the difference in I_D for V_{GS} = −2 V and −1 V. Check the result using Shockley's equation.

Solution From the characteristics, ΔI_D for $V_{GS} = -2$ V, −1 V, $\Delta I_D = 7 - 4.5 = 2.5$ mA
Further,

$$I_{DSS} = 10 \text{ mA}, V_P = -6 \text{ V}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

At $V_{GS} = -2$ V,

$$I_D = 10\left(1 - \frac{2}{6}\right)^2 = 4.46 \text{ mA}$$

At $V_{GS} = -1$ V,

$$I_D = 10\left(1 - \frac{1}{6}\right)^2 = 6.94 \text{ mA}$$

$$\Delta I_D = 6.94 - 4.44 = 2.5 \text{ mA}$$

From characteristics, $\Delta J_D = 2.6$ mA

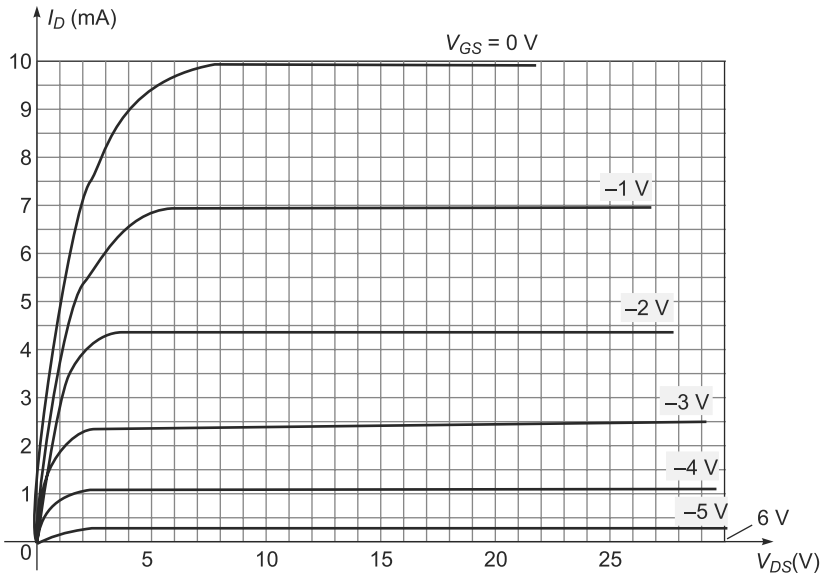


Fig. 16.8 *Drain characteristic*

16.3 METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

The MOSFET transistor has become the most important device for construction of integrated circuits for digital computers. Its thermal stability and other general features make it very suitable for IC design and construction because of smaller silicon-chip space needed.

Depletion-Type MOSFET Constructional Features

Refer Fig. 16.9. On a *p*-type substrate, an *n*-channel is formed which is connected to *D* and *S* terminals through heavily doped *n*-regions.

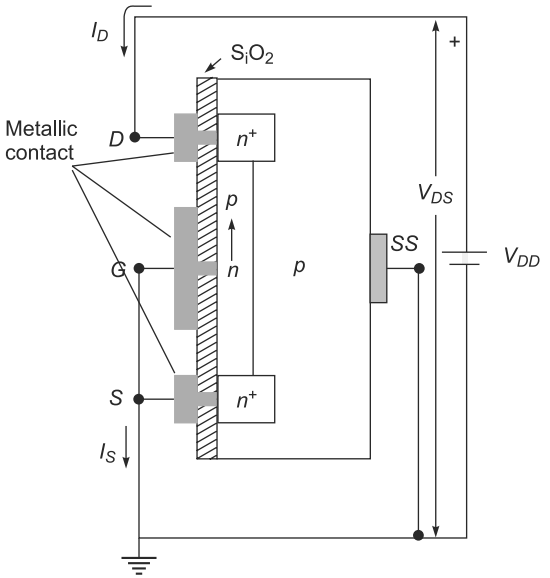


Fig. 16.9 *MOSFET—n-channel depletion type $V_{GS} = 0$, $V_{DS} > 0$*

The *N*-channel is insulated from the gate *G* terminal by an SiO_2 layer, which extends over the complete device. The great quality of the insulated gate is $I_G = 0$ irrespective of any gate voltage which means, extremely high input resistance. This is not so in JFET where I_G is the reverse saturation current though very small (nA).

Operation

When $V_{GS} = 0$ (i.e. positive V_{DS}), saturation current $I_D = I_S = I_{DSS}$ will flow.

When a negative voltage is applied to the gate, say $V_{GTS} = -1$ V, the holes from the substrate are attracted by the gate and so the holes flow into *N*-channel. The holes recombine with electrons being repelled by the gate, thereby reducing the concentration of electrons in the channel as shown in Fig. 16.10.

The result is reduction in saturation current $I_{D(sat)}$. So to make V_{GS} more negative I_D keeps reducing till at $V_{GS} = V_P$, the channel pinches off. The chain characteristics and transfer characteristics are similar to those of JFET, as shown in Fig. 16.11.

However, unlike JFET, if V_{GS} is made positive, the minority electrons get attracted into the *N*-channel and so I_D begins to increase sharply. Even at small values of positive V_{GS}, I_D may exceed the prescribed limit.

Depletion mode and enhancement mode are both shown in Fig. 16.11.

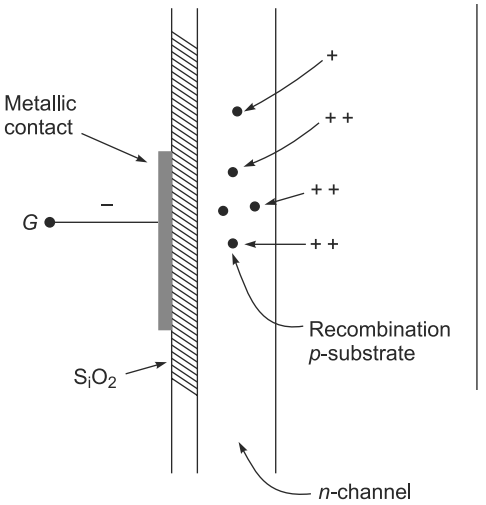


Fig. 16.10 *Channel depletion process*

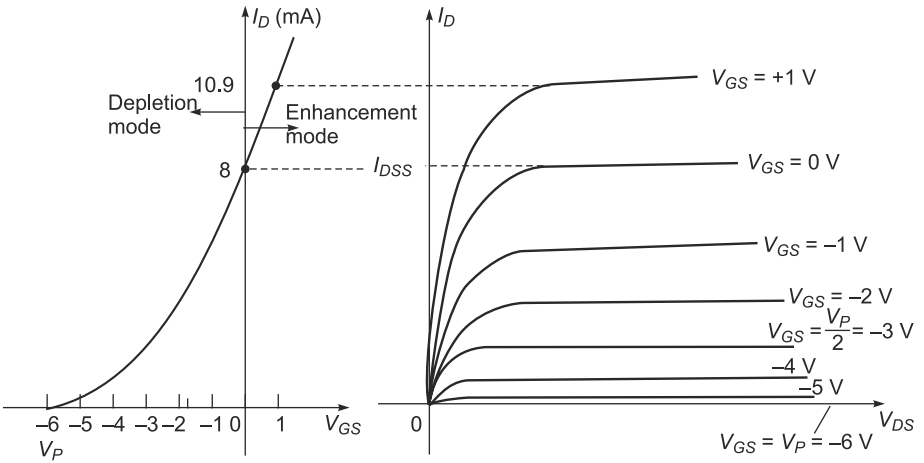


Fig. 16.11 *MOSFET N-channel depletion type*

P-Channel Depletion Type

Compared to *N*-channel type, V_{GS} is positive for depletion; V_{DS} reverses, –ve at *D* and +ve at *S*. The pinch-off voltage V_P will be positive; see Fig. 16.12.

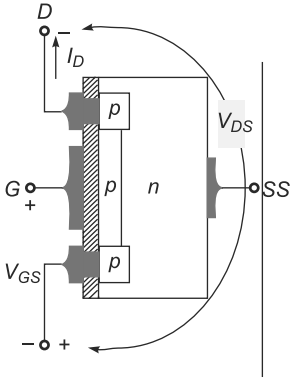


Fig. 16.12 *P-channel depletion type*

The Shockley Equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{16.4}$$

applies for the depletion MOSFET.

Symbols

The symbols for *n*-channel and *p*-channel depletion-type MOSFETs, and the gap between gate and channel are indicative of the insulation-layer of SiO_2.

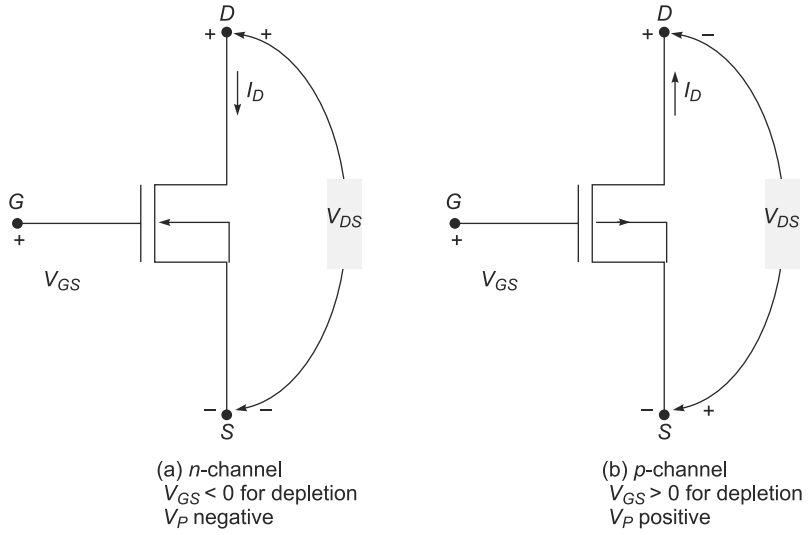


Fig. 16.13 *Symbols for depletion-type MOSFET*

Enhancement-Type MOSFET

The construction is similar to that of depletion type except that there is no channel. Only the *P*-substrate as shown in Fig. 16.14.

Channel Formation and Operation

Let a positive voltage be applied between the gate and source as shown in the circuit diagram of Fig. 16.15.

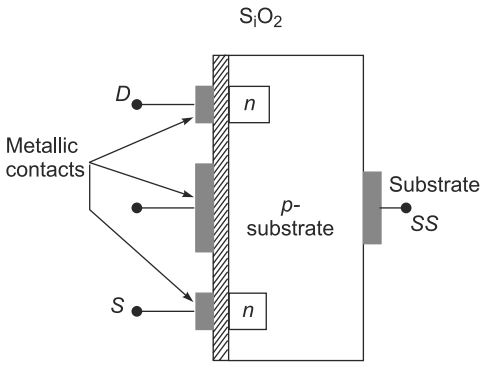


Fig. 16.14 *Constructional details of enhancement MOSFET*

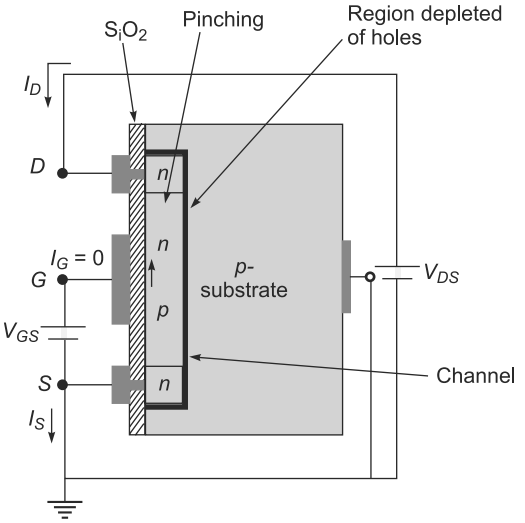


Fig. 16.15 *Pinch-off $V_{GS} > V_T$, $V_{DS} > V_{DS(sat)}$*

The positive gate pushes the holes in the region underneath the gate into the *P*-substrates, while the minority electrons are attracted more into the regions just below the SiO_2 layer. The result is the formation of an *N*-channel as shown in Fig. 16.15. As V_{GS} is increased, the concentration of electrons in the channel goes up, until $V_{GS} = V_T$, called *threshold voltage*. The channel begins to conduct with positive V_{DS} applied. There is a thin layer depleted of holes at the contact of *N*-channel and *P*-substrate.

Keeping V_{GS} constant above V_T, as V_{DS} is increased, a non-uniform depletion region widens at the *D*-end of the channel which becomes narrow as shown in Fig. 16.15. Further, as per KVL,

$$V_{GD} = V_{GS} - V_{DS}$$

At constant V_{GS}, increasing V_{DS} means V_{GD} reduces, i.e. gate becomes less positive than drain. For example, $V_{GS} = 8$ V, V_{DS} is increased from 2 to 5 V. V_{GD} reduces from 6 V to 3 V.

As a consequence, as in JFET, I_D reaches a saturation value at $V_{DS(sat)}$. This is brought out in the drain characteristics of Fig. 16.16.

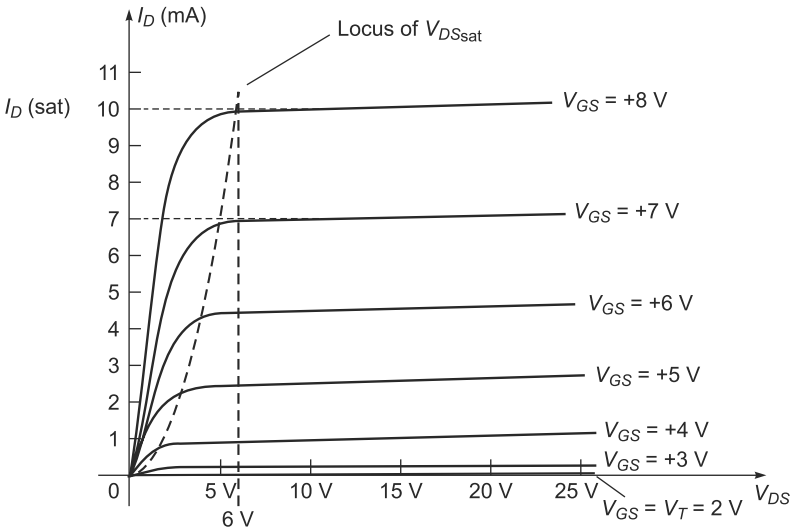


Fig. 16.16 *Drain characteristics of EMOSFET*

- It can be shown that the saturation level $V_{DS(sat)}$ is related to V_{GS} as

$$V_{DS(sat)} = V_{GS} - V_T \tag{16.5}$$

- For $V_{GS} > V_T$, it can be shown from the saturation region of the drain characteristics that I_D can be found from the analytical expression

$$I_D = k\,(V_{GS} - V_T)^2 \tag{16.6}$$

It is a nonlinear relationship which is obvious from Fig. 16.16 in which the characteristic spacing widens for equal increment of V_{GS}.

From any point on the drain characteristics, the constant k in Eq. (16.6) can found as

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \text{ A/V}^2 \tag{16.7}$$

The expression (16.6) is indeed the transfer characteristic. A typical plot is drawn in Fig. 16.17. It can also be plotted from the drain characteristics by reading $I_{D(sat)}$ against V_{GS}. V_T is also available there.

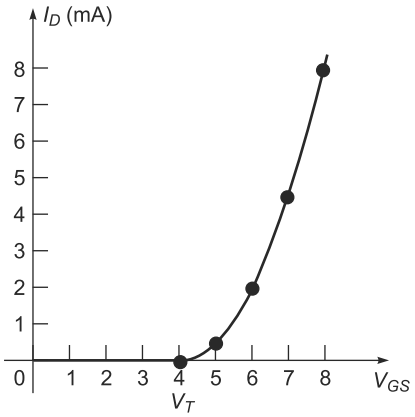


Fig. 16.17 *Transfer characteristic of EMOSFET N-channel k = 0.5 × 10^{-3} A/V^2*

P-type EMOSFET

Substrate is *N*-type, Channel is *P*-type, V_{GS} negative, V_T negative, *D* – and S +.

Symbol of EMOSFET (Fig. 16.18)

The channel is shown broken as it is formed on applying $V_{GS} > V_T$ for *N*-Channel.

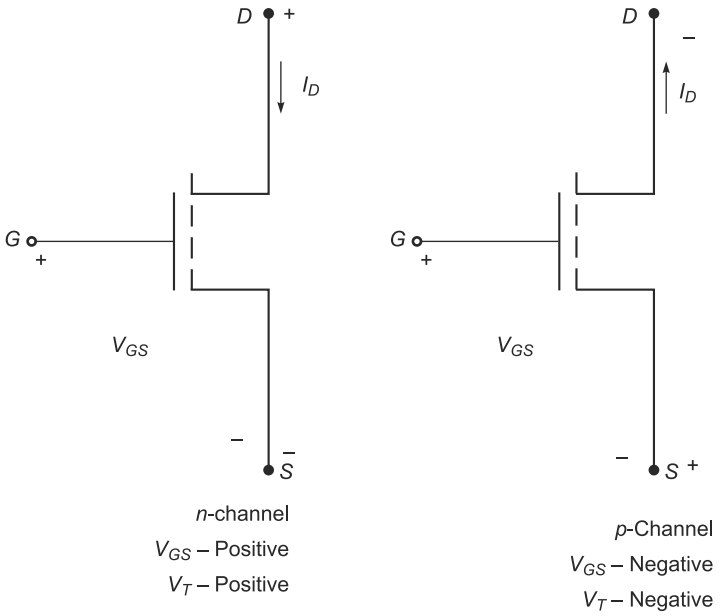


Fig. 16.18 *Symbol of EMOSFET*

Example 16.6

For a depletion-type MOSFET,

I_D = 10 mA at V_{GS} = −1 V

Determine V_P if I_{DSS} = 15 mA.

Solution

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$120 = 15\left(1 + \frac{1}{V_P}\right)^2$$

Solving $V_P = -5.5$ V

Example 16.7

For DMOSFET,

I_D = 4.5 mA, V_{GS} = −2 V

Determine I_{DSS} if V_P = −5 V.

Solution

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$4.5 = I_{DSS}\left(1 - \frac{-2}{-5}\right)^2$$

$$I_{DSS} = \frac{4.5}{(0.6)^2} = 12.5 \text{ mA}$$

Example 16.8

For EMOSFET,

V_T = 4 V, $I_{D(on)}$ = 4 mA, $V_{GS(on)}$ = 6 V

Determine to write the general expression for I_D and find I_D for V_{GS} = 8 V.

Solution

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} = \frac{4 \times 10^{-3}}{(6-4)^2} = 1 \times 10^{-3} \text{ A/V}^2$$

Then

$$I_D = k(V_{GS} - V_T)^2$$

$$I_D = 1 \times 10^{-3}\,(8 - 4) = 16 \text{ mA}$$

Example 16.9

For EMOSFET,

$$k = 0.45 \times 10^{-3}\ \text{A/V}^2,\ I_{D(\text{on})} = 3.5\ \text{mA},\ V_{GS(\text{on})} = 4.5\ \text{V}$$

Determine V_T.

Solution

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2}$$

$$0.45 = \frac{3.5}{(4.5 - V_T)^2}$$

$$(4.5 - V_T)^2 = \frac{3.5}{0.45}$$

$$4.5 - V_T = 2.79$$

$$V_T = 1.7\ \text{V}$$

16.4 FET CIRCUIT CONFIGURATIONS

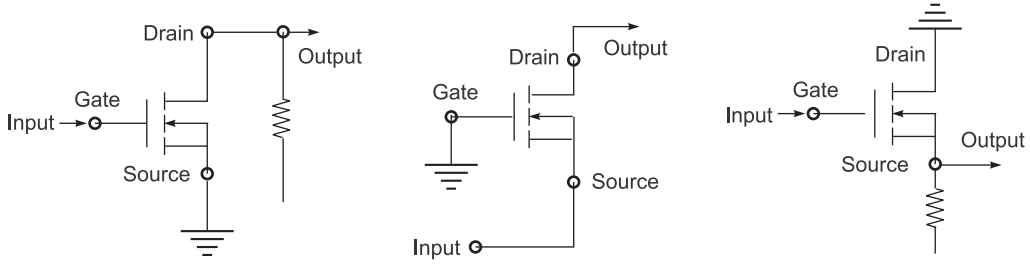
As FETs are three-terminal devices, there are three possible configurations in which these can be connected.

Common-Source (CS) Circuit

The input signal is connected to gate which is the control terminal. Output is taken from the drain across suitable impedance and source is the common terminal, which is grounded as shown in Fig. 16.19(a). This is the most useful and commonly used connection for voltage amplification.

Common-Gate (CG) Circuit

In this connection, the gate is the common terminal, the drain is the output terminal and source is where the input is connected as shown in Fig. 16.19(b). It hardly yields any gain and is not used in practice.



(a) Common-source connection (b) Common-gate connection (c) Common-drain circuit

Fig. 16.19 *Configuration of FET, enhancement mode, N-channel MOSFET*

Common-Drain (CD) Circuit

The input signal is applied at the gate, the drain is the common grounded terminal, while output is taken from the source across an impedance. This connection is shown in Fig. 16.20(c). It has special applications and is known as *source-follower* as the output signal has the same phase as the input signal.

Note: Figures 16.19(a), (b) and (c) do not include biasing details, which will be explained in the following part of this chapter.

16.5 CMOS CIRCUITS

CMOS is the complimentary MOS wherein two enhancement MOSFETs, one *N*-type (*N*MOS) and other *P*-type (*P*MOS), are connected as a complimentary pair. The two gates are connected to form the input terminal and the two drains are connected to form the output terminals as shown in Fig. 16.20(a). The CMOS circuit offers two advantages:

1. The drain current is very low and flows mainly during transition from one state to the other (ON/OFF).
2. The power drawn in steady state is extremely small.

Because of these two advantages, it has gained great popularity in digital circuits. It also has certain applications in analog circuits.

Digital-Circuit Applications

The circuit for a CMOS digital inverter is drawn in Fig. 16.20(a). The source terminal of *P*MOS (T_2) is connected to $V_{SS} = 5$ V, while the source terminal of *N*MOS (T_1) is grounded.

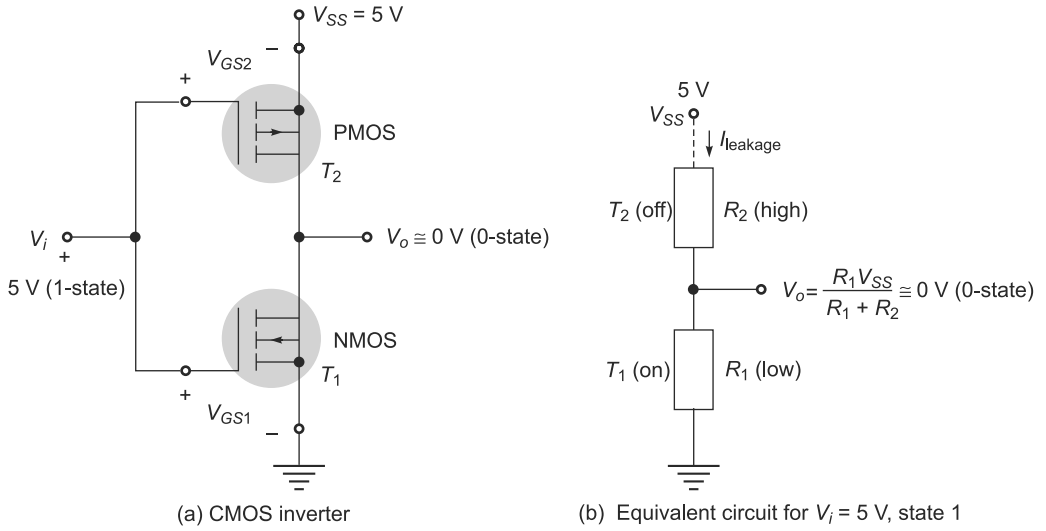


Fig. 16.20 *CMOS circuits*

Operation

1. Input

$$V_i = 5 \text{ V} \Rightarrow \text{1-state}$$

$$V_{GS2} = 5 - 0 = 5 \text{ V}$$

T_2 is nonconducting, OFF (its VT is negative), draws only leakage current, offers high resistance (R_2)

$$V_{GS1} = 5 \text{ V} > V_T$$

T_1 is conducting, ON; offers very low resistance (R_1). The circuit equivalent in this state is drawn in Fig. 16.20(b).

Output

$$V_o \approx 0 \Rightarrow \text{0-state}$$

It can be seen from the circuits of Fig. 16.20(b) that

$$V_o = \frac{R_1}{R_1 + R_2} V_{SS} \approx 0 \text{ V}$$

2. Input

$$V_i = 0 \text{ V} \Rightarrow \text{0-state}$$

$$V_{GS2} = -5 \text{ V}, T_2 \text{ conducting (low resistance)}$$

$$V_{GS1} = 0 \text{ V}; T_1 \text{ nonconducting (high resistance)}$$

Output

$$V_o \approx 5 \text{ V} \Rightarrow \text{1-state}$$

We thus see that the circuit acts as an inverter; 1-state input produces 0-state output and 0-state input produces 1-state output.

It is observed in this circuit that only one transistor is turned on in any of the output states. As the transistors are series connected, no current is drawn from the battery source in either of the two states. Current is drawn from the battery only during state transition (either way). CMOS circuits, therefore, draw extremely low power from the battery source and so their energy consumption is very small. This is the major attraction why CMOS is used in digital applications.

16.6 FET BIASING

We shall consider only voltage-divider biasing as this is most commonly adopted. By examining the drain characteristics of the device, a Q-point is selected in the middle of the saturation region, which fixes V_{GSQ} and I_{DQ}. The biasing circuit resistors are to be selected for the device under dc conditions to operate at the Q-point.

16.6.1 Voltage Divider Biasing

The circuit is drawn in Fig. 16.21. It is the same for any FET.

As per voltage divider

$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} \tag{16.8}$$

Then

$$V_{GS} = V_G - I_D R_S, I_S = I_D \tag{16.9}$$

$I_D R_S$ provides stabilising negative voltage feedback.

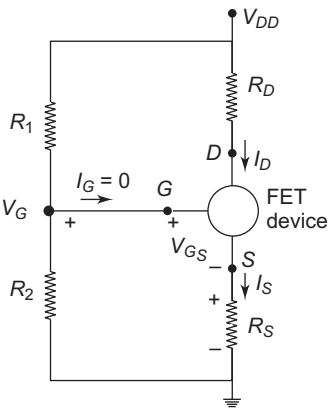


Fig. 16.21

Device transfer characteristic,

$$I_D = f(V_{GS})\big|_{\text{Device Parameters}}; \text{ nonlinear} \tag{16.10}$$

As V_{GSQ} has been chosen, the choice of R_S and simultaneous solution of Eqs (16.8) and (16.9) yields I_{DQ}.

KVL for DS load yields

$$V_{DSQ} = V_{DQ} - I_D(R_S + R_D),\ R_D \text{ has to be selected} \tag{16.11}$$

Biasing analysis/design is then complete.

Simultaneous Solution of Eqs. (16.9) and (16.10)

(i) Equation (16.10) is the transfer characteristic of FET (nonlinear function of V_{GS}). Equation (16.9) is a straight line, whose intersection with the transfer characteristic yields I_{DQ} and V_{GSQ}.

or

(ii) Substituting I_D from Eq. (16.9) in Eq. (16.10) leads to a quadratic equation in V_{GS} yielding two solutions from which the appropriate one is to be chosen.

JFET

Refer Fig. 16.21.

JFET: $I_{DSS} = 10$ mA, $V_P = -6$ V

Circuit: $R_1 = 2.2$ MΩ, $R_2 = 280$ kΩ, $V_{DD} = 16$ V

$R_D = 2$ kΩ, $R_S = 1.5$ kΩ

To determine at Q-point

V_{GS}, I_D, V_{DS}, V_{DG}

Plot the transfer characteristic (Fig. 16.22).

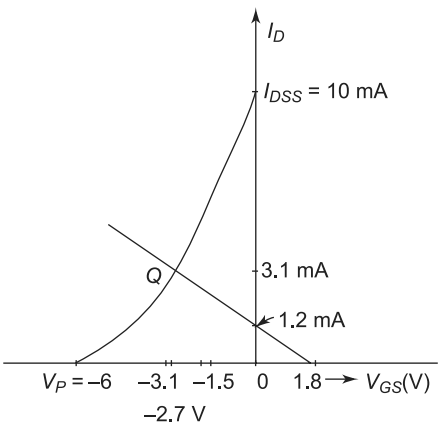


Fig. 16.22 *Transfer characteristic*

$$I_D = 10\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{16.12}$$

$$V_{GS} = -3 \text{ V},\ \frac{V_{GS}}{V_P} = \frac{1}{2},\ I_D = 2.5 \text{ mA}$$

$$V_{GS} = 1.5 \text{ V}, \frac{V_{GS}}{V_P} = \frac{1}{4}, I_D = 5.265 \text{ mA}$$

Plot Eq. (16.7).

$$V_G = \frac{280}{2.2 \times 10^3 + 280} \times 16 = 1.8 \text{ V}$$

$$V_{GS} = 1.8 - 1.5\, I_D \tag{16.13}$$

$$I_D = 0,\ V_{GS} = 1.8 \text{ V}$$

$$V_{GS} = 0,\ I_D = \frac{1.8}{1.5} = 1.2 \text{ mA}$$

At intersection, Q-point $\Rightarrow V_{GS} = -2.7$ V $I_D = 3.1$ mA

$$V_{DS} = 16 - (2 + 1.5) \times 3.1 = 5.15 \text{ V}$$

Analytic Approach

From Eq. (16.13),

$$I_D = \frac{2.8 - V_{GS}}{1.5} = 1.2 - 0.67\, V_{GS} \tag{16.14}$$

Substituting I_D in Eq. (16.13),

$$1.2 - 0.67\, V_{GS} = 10 \left(1 - \frac{V_{GS}}{-6}\right)^2$$

Let $V_{GS} = x$

$$1.2 - 0.67x = 10\left(\frac{6 + x}{6}\right)^2 = \frac{10}{36}\ (6 + x)^2$$

$$4.32 - 2.41x = x^2 + 12x + 36$$

$$x^2 + 14.41x + 31.68$$

$x = -2.7, -11.7$ (rejected as more negative than V_P)

Then $V_{GS} = -2.7$ V

The same result as obtained by the graphical solution.

DMOSFET

Refer Fig. 16.21.

DMOSFET parameters

$$I_{DSS} = 8 \text{ mA},\ V_p = -4$$

Circuit data

$$V_{DD} = 16 \text{ V}$$

$$R_1 = 100 \text{ M}\Omega,\ R_2 = 10 \text{ M}\Omega,$$

$$R_D = 1.6 \text{ k}\Omega,\ R_S = 700\ \Omega$$

To determine

$$I_{DQ},\ V_{GSQ},\ V_{DSQ}$$

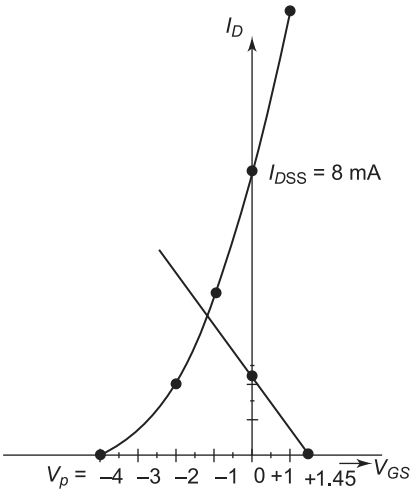


Fig. 16.23 *Transfer characteristic*

Plotting transfer characteristic (Fig. 16.23),

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = -2 \text{ V}; I_D = 8\left(1 - \frac{1}{2}\right)^2 - 2 \text{ mA}$$

$$V_{GS} = -1 \text{ V}, I_D = 8\left(1 - \frac{1}{4}\right)^2 = 4.5 \text{ mA}$$

$$V_{GS} = +1 \text{ V}, I_D = 8\left(1 - \frac{1}{4}\right)^2 = 12.5 \text{ mA}$$

Plotting Eq. (16.8),

$$V_G = \frac{10}{100 + 10} \times 16 = 1.45 \text{ V}$$

$$V_{GS} = V_G - 0.7\, I_D$$

$$I_D = 0 \qquad V_{GS} = V_G = 1.45 \text{ V}$$

$$V_{GS} = 0 \qquad I_D = \frac{1.45}{0.7} = 2.07 \text{ mA}$$

At intersection, Q-point

$$I_{DQ} = 3.8 \text{ mA}, V_{GSQ} = -1.2 \text{ V}$$

From Eq. (16.10),

$$V_{DSQ} = 16 - (1.6 + 0.7) \times 3.8 = 7.26 \text{ V}$$

EMOSFET

Refer Fig. 16.21.

EMOSFET parameters

$$V_T = 4 \text{ V}, V_{GS(\text{on})} = 8 \text{ V}, I_{D(\text{on})} = 2.5 \text{ mA}$$

Biasing circuit

$$V_{DD} = 35 \text{ V}, R_1 = 20 \text{ M}\Omega, R_2 = 16 \text{ M}\Omega$$
$$R_D = 2.5 \text{ k}\Omega, R_S = 0.75 \text{ k}\Omega$$

To determine: At Q-point

$$I_{DQ}, V_{GSQ}, V_{DS}$$

Plot transfer characteristic (Fig. 16.24).

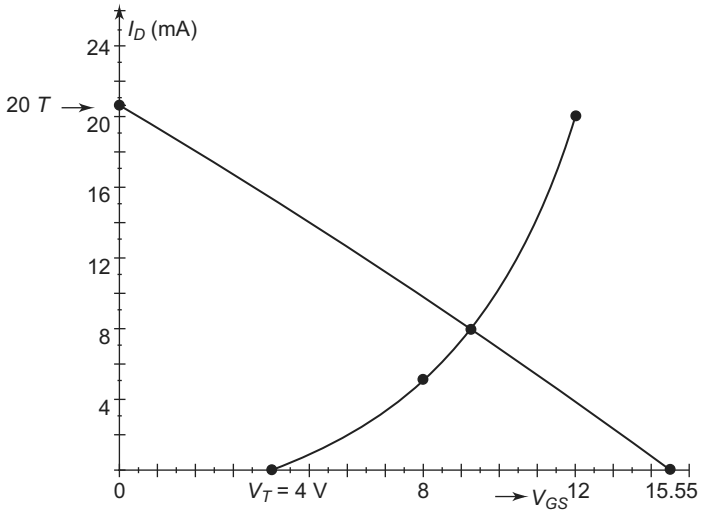


Fig. 16.24

$$k = \frac{2.5}{(8-4)^2} = 0.156 \text{ mA/V}^2$$
$$I_D = 0.156 (V_{DS} - 4)^2$$
$$V_{GS} = 8 \text{ V}, I_D = 0.156 \times 16 \; 2.5 \text{ mA}$$
$$V_{GS} = 12 \text{ V}, I_D = 0.156 \times 64 = 10 \text{ mA}$$

Plot Eq. (16.8).

$$V_G = \frac{16}{20+16} \times 35 = 15.55 \text{ V}$$

$$V_{GS} = 15.55 - 0.75 \, I_D$$
$$V_{GS} = 0, I_D = 20.7 \text{ mA}$$
$$I_D = 0, \; V_{GS} = 15.55$$

At Q-point,

$$V_{GSQ} = 9.2 \text{ V}, I_{DQ} = 8.4 \text{ mA}$$

From Eq. (16.11),

$$V_{DS} = 35 - (2.5 + 0.7) \times 8.4 = 8.12 \text{ V}$$

p-channel JFET

Refer Fig. 16.21 directions of I_D and I_S reverse, V_{DD} is negative, JFET parameters $I_{DSS} = 10$ mA, $V_P = 6$ V (positive).

Biasing circuit

$$V_{DD} = -20 \text{ V}, R_1 = 64 \text{ k}\Omega, R_2 = 20 \text{ k}\Omega$$

$$R_D = 2 \text{ k}\Omega. Rs = 1.2 \text{ k}\Omega$$

To determine at *Q*-point

$$V_{GSQ}, I_{DQ}, V_{DS}$$

Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 10\left(1 - \frac{V_{GS}}{6}\right)^2$$

Voltage divider

$$V_G = \frac{20}{64 + 20} \times (-20) = -4.76 \text{ V}$$

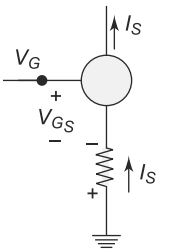


Fig. 16.25

KVL for *GS* loop (adjoining Fig. 16.25)

$$V_G - V_{GS} + R_S I_D = 0; I_D - I_S; \text{ direction of currents } S \text{ to } D$$

$$-4.76 - V_{GS} + 1.2\, I_D = 0; I_D = I_S$$

or
$$I_D = \frac{4.76 + V_{GS}}{1.2} = 4 + 0.833 V_{GS} \tag{16.15}$$

Let $V_{GS} = x$,

Substituting I_D in Eq (16.15),

$$4 + 0.833x = \frac{10}{36}(6 - x)^2$$

$$14.4 + 3x = 36 - 12x + x^2$$

$$x^2 - 15x + 21.6 = 0 \Rightarrow x = 1.6 \text{ V}, 13.476 \text{ V (rejected)}$$

Then,

$$V_{GSQ} = 1.6 \text{ V}$$

$$I_{DQ} = 10\left(1 - \frac{1.6}{8}\right)^2 = 5.38 \text{ mA}$$

KVL *DS* loop,

$$-20 - (2 + 1.2) \times 5.38 - V_{DS} = 0$$

or
$$V_{DS} = -2.78 \text{ V}$$

Summary

➢ **JFET**

$I_D = I_S$, $I_G \approx 0$

N-channel $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$R_{in} > 100$ MΩ, $I_{DSS} = I_D$ at $V_{GS} = 0$

V_P = pinch-off voltage, negative value

➢ **MOSFET**

$I_G = 0$, $I_D = I_S$

Depletion type, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

N-channel can conduct for $V_{GS} > 0$.

➢ **DMOSFET**

I_D rises very sharply

$R_{in} > 10^{10}$ Ω (not used in this mode)

➢ **MOSFET**

$I_D = k(V_{GS} = V_T)^2$

Enhancement type $V_T = V_{GS}$ (Threshold)

N-channel $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$

$R_{in} > 10^{10}$ Ω

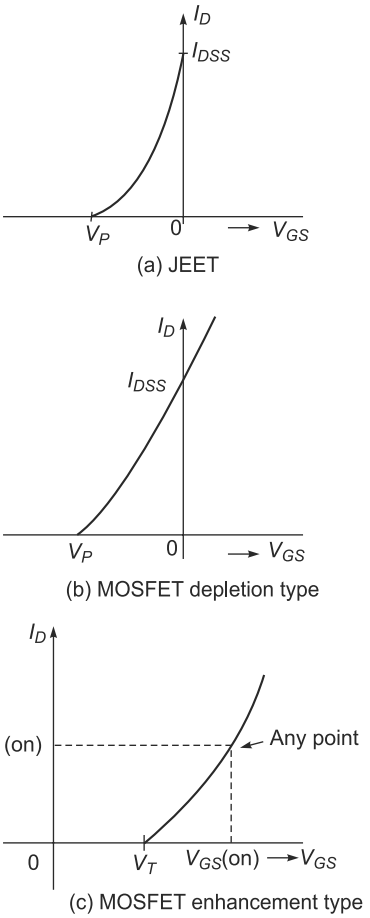


Fig. 16.26 *Transfer characteristic of various types of FETs*

Exercises

Review Questions

1. Sketch an *n*-channel JFET. Explain how the pinch-off takes place for $V_{GS} = 0$. What is meant by I_{DSS}?
2. Draw the symbols for *n*-and *p*-channel JFETs. Indicate the polarity of voltages and direction of current.
3. Define the pinch-off voltage V_P.
4. Explain why $I_G \approx 0$ for a JFET.
5. What is meant by a field effect transistor? How is it different for a BJT?
6. Explain the various regions of *n*-channel JFET. Comment in the space of saturation region drain current with respect to V_{GS}.
7. Why are *N*MOS devices preferred to *P*MOS devices?
8. Why is the input resistance of MOSFET larger than that of a JFET depletion type?
9. Sketch the constructional view of *p*-channel depletion-type MOSFET. Explain the form of the drain characteristic for $V_{CS} = 0$.

10. In what ways is the construction of depletion-type MOSFET similar to that of JFET and in what ways is it different?
11. Explain the construction difference between enhancement and depletion-type MOSFET.
12. What is the meaning and significance of V_T?
13. Draw the symbol of *N*- and *P*-type EMOSFETs. Indicate the polarity of voltages and direction of currents.
14. Sketch and compare the transfer characteristics of *N*-channel DMOSFET and EMOSFET.

Problems

1. From the JFET characteristics of Fig. 16.5, determine I_D for $V_{CS} = -0.5$ V and $V_{GS} = -1.5$ V.
2. From the JFET characteristics, determine the device resistance at the initial part of the characteristics for $V_{GS} = 0$ and $V_{GS} = -1$ V.
3. Plot the transfer characteristic for the JFET characteristics of Fig. 16.8.
4. For the characteristics of Fig. 16.8, determine V_{GS} for $I_D = 5$ mA.
5. Given $I_{DSS} = 6$ mA, $V_P = -3$ V. Determine the drain current at $V_{CS} = -1$, 0, 1and 2 V. What conclusions do you draw?
6. Given $I_D = 12$ mA and $V_{GS} = 1$ V. Determine V_P if $I_{DSS} = 8.5$ mA.
7. Given $I_D = 4.5$ mA at $V_{GS} = -2$ V. Determine I_{DSS} if $V_P = -5$ V.
8. Sketch the transfer and drain characteristic for *N*-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -6$ V, range of $V_{GS} = -V_P$ to $V_{GS} = 1$.
   Hint. Take $V_{GS} = -6$ V, – 4 V, –2 V, 0 V and 1 V. Calculate I_D for each value of V_{CS} and then sketch.
9. Given $V_P = -4$ V, $I_D = 2.5$ mA at $V_{GS} = -2$ V. Calculate I_{DSS}. Also calculate I_D at $V_{GS} = +1$ V
10. Given $V_T = 4$ V, $I_{D(on)} = 4$ mA, $V_{GS(on)} = 6$ V. Determine k and then find V_{GS} for $I_D = 12$ mA.
11. Given $k = 0.4$ mA/V^2, $I_{D(on)} = 4$ mA, $V_{GS(on)} = 8$ V. Determine V_T.
12. A *P*-channel EMOSFET has $V_T = -6$ V and $k = 0.5$ mA/V^2. Determine I_D at $V_{GS} = -10$ V. Sketch the transfer characteristics.
13. The transfer characteristic of an *n*-channel EMOSFET is drawn in Fig. 16.27. Determine k and T. Write the general expression for I_D.
    $k = 0.5$ m A/V^2, $V_T = 2$ V.
14. For the fixed-bias circuit of Fig. 16.28, determine
    (a) J_{DQ} and V_{GSQ} (b) V_{DS}

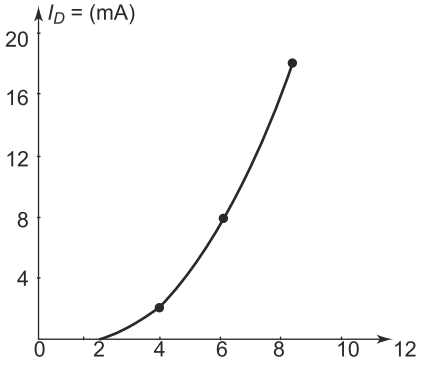


Fig. 16.27

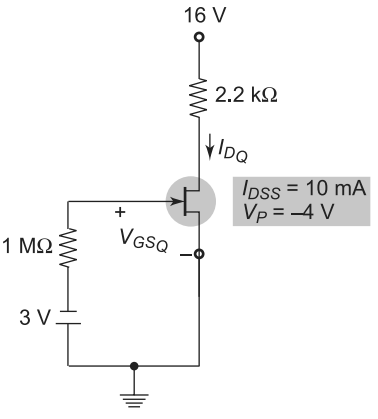


Fig. 16.28

15. For the self-bias circuit of Fig. 16.29, determine
(a) I_{DQ}, V_{GSQ} (b) V_{DS} (c) I_{DSS} = 119 mA
16. For the voltage-divider bias circuit of Fig. 16.30, determine
(a) V_{CSQ}, and I_{DQ} (b) V_{DS}

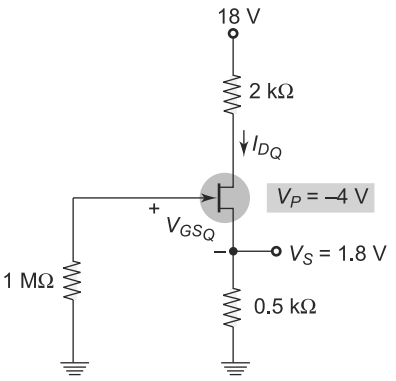


Fig. 16.29

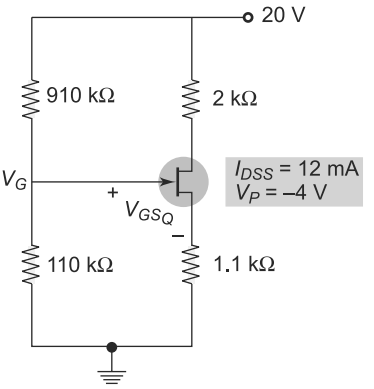


Fig. 16.30

17. For the fixed-bias configuration of Fig. 16.31, determine
V_{GSQ}, I_{DQ}, V_{DS}
Given I_{DSS} = 8 mA V_P = –5 V
18. The biasing circuits are drawn in Fig. 16.32. Find V_{GSQ}, I_{DA}, V_{DS}.

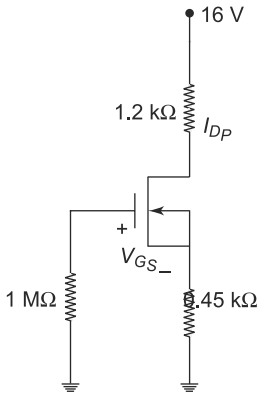


Fig. 16.31

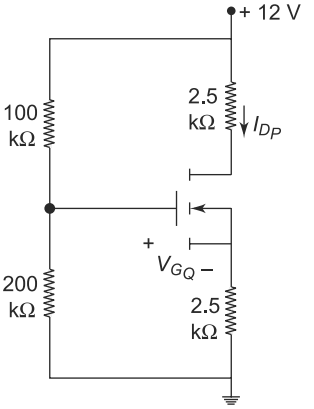


Fig. 16.32

Multiple-Choice Questions

1. The best location for setting a *Q*-point on dc load line of an FET amplifier is at
(a) mid-point (b) saturation point (c) cut-off point (d) none of these
2. Which of the following techniques is used for biasing the enhancement-type MOSFET?
(a) Voltage-divider bias (b) Current-source bias
(c) Collector-feedback bias (d) Self-bias

3. A common-gate amplifier has
   (a) high input resistance and high output resistance
   (b) low input resistance and high output resistance
   (c) low input resistance and low output resistance
   (d) high input resistance and low output resistance
4. If properly biased, a JFET will act as a
   (a) voltage-controlled voltage source (b) current-controlled voltage source
   (c) voltage-controlled current source (d) current-controlled current source
5. Which of the following bias methods provide a solid Q-point in JFET amplifiers?
   (a) Gate bias (b) Voltage-divider bias (c) Current bias (d) Self-bias
6. The voltage of a common source JFET amplifiers depends upon its
   (a) transconductance (b) amplification factor
   (c) internal load resistance (d) both (a) and (c)
7. The transconductance g_m of a JFET is equal to

   (a) $\dfrac{-2I_{DSS}}{V_P}$ (b) $\dfrac{2}{|V_P|}\left(\sqrt{I_{DSS} \cdot I_D}\right)$

   (c) $\dfrac{-2\,I_{DSS}}{V_P}\left(1-\dfrac{V_{GS}}{V_P}\right)$ (d) $\dfrac{I_{DSS}}{V_P}\left(1-\dfrac{V_{GS}}{V_P}\right)$

8. A zero-gate bias channel resistance for a JFET is 750 Ω and the pinch-off voltage is 3 V. For a gate bias of 1.5 V and very low drain voltage, the device would have a resistance of
   (a) 320 Ω (b) 1000 Ω (c) 816 Ω (d) 1270 Ω
9. A transconductance amplifier has
   (a) high input impedance and low output impedance
   (b) low input impedance and high output impedance
   (c) high input and output impedances
   (d) low input and output impedances
10. The threshold voltage of an n-channel enhancement-mode MOSFET is 0.5 V. When the device is biased at a gate voltage of 3 V, pinch-off would occur at a drain voltage of
    (a) 4.5 V (b) 3.5 V (c) 2.5 V (d) 1.5 V

Answers

Problems

1. 6.125 mA, 3.125 mA
2. 0.22 kΩ, 1.33 kΩ
4. − 4.24 V
5. 2.67 mA, 6 mA, 10.67 mA, 16.6 mA; The device cannot be used for $V_{GS} > 0$
6. −5.31 V
7. 12.36 mA
9. 10 mA, 15.63 mA
10. k = 1 mA/V^2, 7.46 V
11. 4.84 V
12. 8 mA
14. (a) 1.11 mA, − 3 V (b) 13.56 V
17. −3.3 V, 7.3 mA, 4 V
18. −4.8 V, 1.28 mA, 5.6 V

Multiple-Choice Questions

1. a 2. c 3. b 4. a 5. c 6. d 7. c 8. c 9. a 10. b

Small-Signal Model of Transistors and Amplifiers

chapter 17

Goals & Objectives

- Introduction of BJT and amplifiers
- Analysis of BJT small-signal model—common base and common emitter configuration
- Hybrid equivalent circuit parameters of BJT
- Calculating the current gain and voltage gain of CE BJT amplifier
- FETs small-signal models and amplifier
- Discussion of the effect of source and load resistance and frequency response

17.1 INTRODUCTION

One of the important application of transistors is amplification of small-signal (ac signal). For this purpose, the transistor is biased at an operating point. The signal is then applied to the appropriate terminal of the transistor through a *coupling capacitor*, which acts as short circuit for the signal frequencies but blocks the biasing dc from disturbing the signal source. The output is then taken from the output terminal of the transistor through another coupling capacitor, so that the dc is blocked and only amplified signal is available at the output.

The transistor is carrying both dc and ac currents and voltages. The amplifier circuit analysis is rendered simple by separating dc and ac analysis. The dc analysis has been carried out in **chapters 15, 16**. The coupling capacitors act as open circuits. For ac analysis, dc sources are shorted out and coupling capacitors bypass capacitor act as short circuit for a frequencies.

To illustrate the procedure consider the example of a small-signal (ac) *BJT RC-coupled amplifier* of Fig. 17.1(a) wherein voltage divide bias is provided biasing analysis is carried out (Chapter 16) by open circuiting all capacitors; coupling and bypass. For ac analysis, dc source is shorted out (grounded) and capacitor are shorted out resulting in the network of Fig. 17.1(b). Observe that R_E is shorted by the *bypass capacitor*. The transistor is now replaced by its smaller signal model at the operating point. This is the subject matter of this chapter for both BJT and FETs *RC*-coupled amplifier.

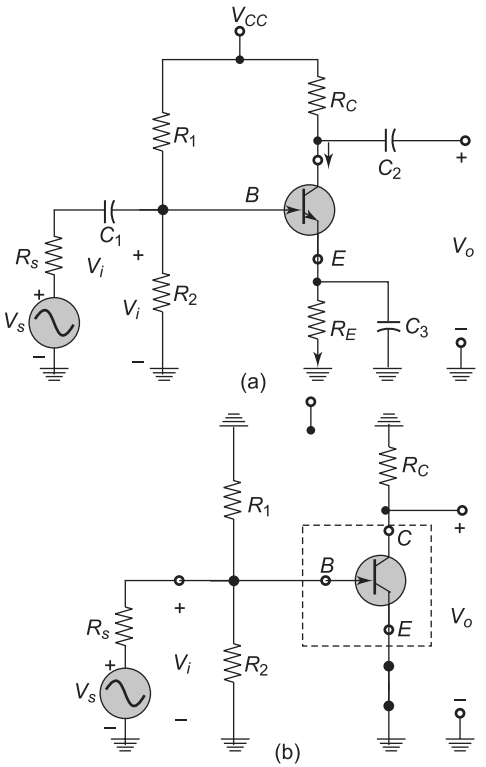


Fig. 17.1 *(a) BJT RC-coupled amplifier (b) Small-signal circuit: dc grounded capacitors shorted*

17.2 BJT SMALL-SIGNAL MODEL

We will employ the r_e model.

17.2.1 Common-Base Configuration (CB)

The biased *NPN* transistor in sketched in Fig. 17.2(a). The forward-biased *BE* junction acts like a forward-biased diode as shown in Fig. 17.2(b). For small signals imposed on bias currents and voltages, the diode after dynamic resistance r_e as shown in Fig. 17.2(c).

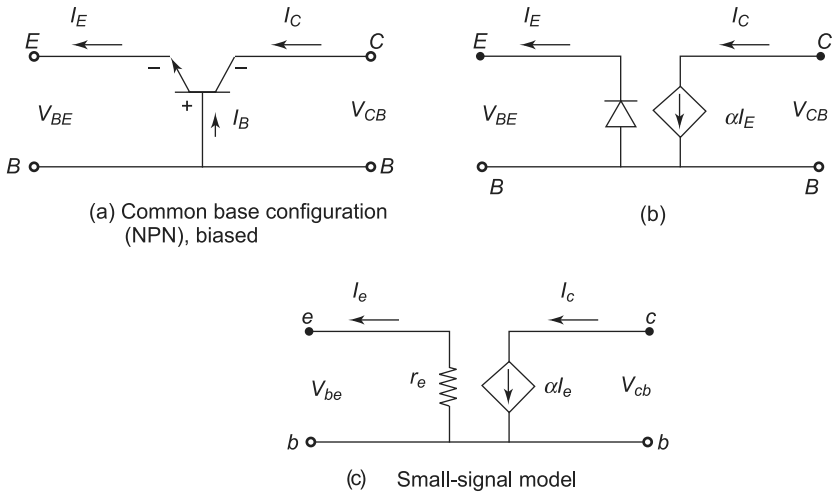


Fig. 17.2 *CB configuration*

As shown earlier,

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{V_{be}}{I_e} \tag{17.1}$$

17.2.2 Common-Emitter Configuration (CE)

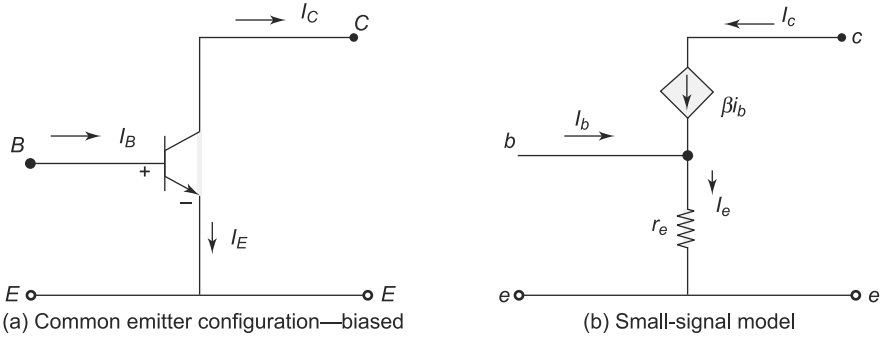


Fig. 17.3 *CE configuration*

The common-emitter configuration biased is shown in Fig. 17.3(a). The small-signal, forward-biased BE diode is replaced by dynamic resistance r_e carrying current I_e; $I_c = \beta I_b$. The small-signal model is drawn in Fig. 17.3(b).

Now,

$$I_e = (1 + \beta) I_b$$

So $$V_{be} = r_e I_e = (1 + \beta) r_e I_b \approx (\beta r_e)\, I_b$$

The circuit of Fig. 17.3(b) can be drawn as in Fig. 17.4.

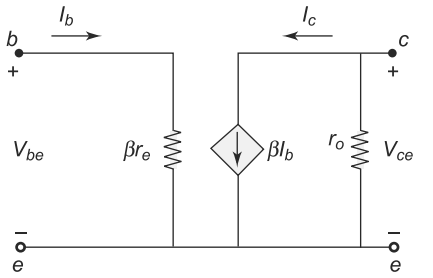


Fig. 17.4 *Small-signal model—CE configuration*

$$\beta r_e = \beta \frac{V_{be}}{I_e} = \frac{I_e}{I_b} \cdot \frac{V_{be}}{I_e} = \frac{I_c}{I_e}\left(\frac{V_{be}}{I_b}\right)$$

$$\beta r_e = \left(\frac{\beta}{1+\beta}\right)\frac{V_{be}}{I_b} = \left(\frac{\beta}{1+\beta}\right) r_\pi$$

$\beta r_e \approx r_\pi$; dynamic function resistance (17.2)

The slight upward slope of the collector characteristics contributes an output resistant at CE terminals.

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_c}\right|_{\text{at } Q} \text{; very high usually ignored}$$

It is shown in Figs 17.4 and 17.5.

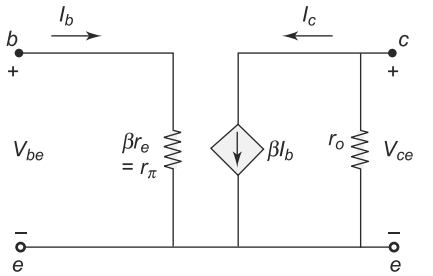


Fig. 17.5 r_π-β *model*

Now $$\beta I_b = \beta \frac{V_{be}}{\beta r_e} = \frac{V_{be}}{r_e} = g_m V_{be}$$

$$g_m = \frac{1}{r_e} = \text{transconductance, units S}$$

βr_e-g_m model is shown in Fig. 17.6; r_o neglected.

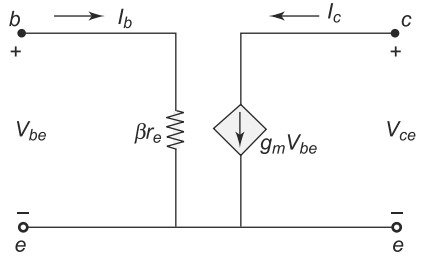


Fig. 17.6 βr_e-g_m *model*

The *circuit equivalent* of a BJT amplifier of Fig. 17.1(b) is drawn in Fig. 17.7. Voltage and current gain can be easily found by circuit analysis. One observation is made at a glance. The output voltage has a negative sign, which is indication of the fact that output voltage is *phase reversed* from the input voltage (source).

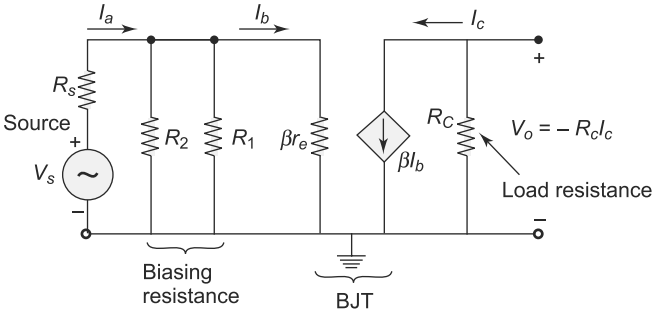


Fig. 17.7

17.3 HYBRID EQUIVALENT OF BJT—SMALL-SIGNAL MODEL

It has been seen above that BJT is a two-port device. It can therefore by expressed in the form of *h*-parameters defined as per Fig. 17.8(a).

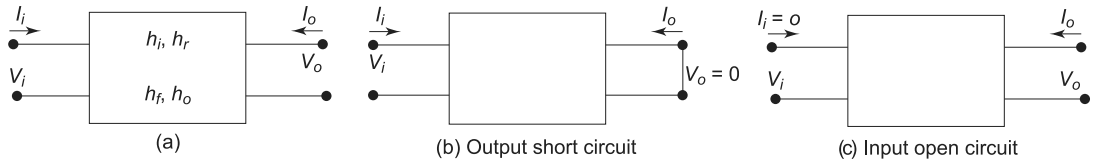


Fig. 17.8 *Small-signal model of BJT*

$$V_i = h_i I_i + h_r V_o \tag{17.3}$$

$$I_o = h_f I_i + h_o V_o \tag{17.4}$$

Output short circuited ($V_o = 0$), Fig. 17.8(b)

$$h_i = \frac{V_i}{I_i}, \text{ short circuit input impedance } (\Omega)$$

$$h_f = \frac{I_o}{I_i}, \text{ short circuit forward current transfer ratio (dimensionless)}$$

Input open circuited ($I_i = 0$), Fig. 17.8(c)

$$h_r = \frac{V_i}{V_o} = \text{open circuit reverse voltage ratio (dimensionless)}$$

$$h_o = \frac{I_o}{V_o} = \text{open circuit output admittance (S)}$$

The *h*-parameter circuit model is drawn in Fig. 17.9.

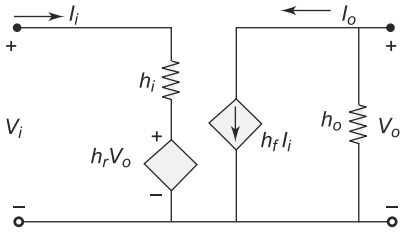


Fig. 17.9 *Parameter circuit model*

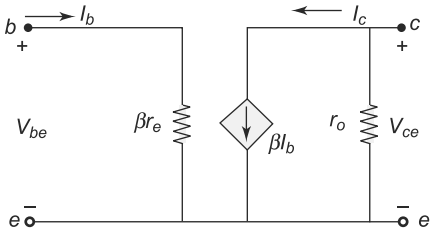


Fig. 17.10 *CE small-signal model*

The corresponding *CE* small-signal model is drawn in Fig. 17.10. By comparison,

$$h_i = \beta r_e$$

$$h_f = \beta$$

$$h_r = 0$$

$$h_o = r_o$$

In *CE* configuration, we write the *h*-parameters as

$h_{ie}, h_{fe}, h_{re}, h_{oe}$

In *CB* configuration, the *h*-parameters are

$h_{ib}, h_{fb}, h_{rb}, h_{ob}$

Finally, in terms of *h*-parameters, for small-signal BJT in *CE* configuration, the circuit model is drawn in Fig. 17.11.

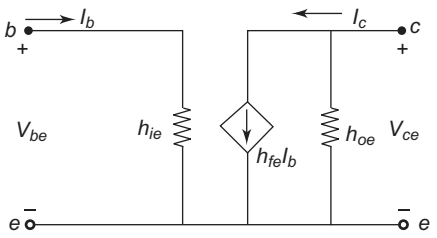


Fig. 17.11 *Hybrid model of BJT (small signal)*

Example 17.1

A BJT in *CB* configuration has I_E(dc) = 3.5 mA, $\alpha = 0.988$, applied voltage 50 mV, load 2.5 kΩ. Determine r_e, Z_o (input impedance), I_e, V_o, A_v (voltage gain), A_i (current gain), and I_b.

Solution The small-signal circuit is drawn in Fig. 17.12.

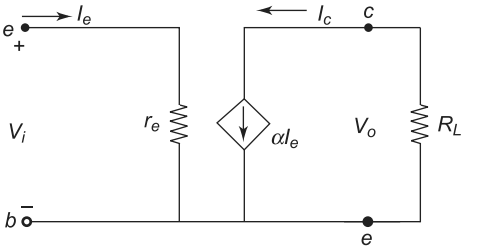


Fig. 17.12 *CB small-signal model*

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26}{3.5} = 7.43\ \Omega$$

Input impedance, $Z_i = r_e = 7.43\ \Omega$

$$I_i = I_e = \frac{V_i}{r_e} = \frac{30}{7.43} = 4 \text{ mA}$$

$$V_o = -\alpha I_e R_L$$

$$= -0.988 \times 4 \times 2.5 = 9.88 \text{ V}$$

Voltage gain, $A_V = \frac{V_o}{V_i} = \frac{-9.88}{30 \times 10^{-3}} = -329$

Current gain, $A_i = \frac{I_o}{I_i} = \frac{I_c}{I_e} = \alpha = 0.988$

$$I_c = 0.988\ I_e$$

$$I_e = I_c + I_b \quad \text{or} \quad I_b = I_e - I_c = (1 - 0.988)\ I_e$$

$$I_b = 0.011 I_e = 0.012 \times 4 = 0.048 \text{ mA or } 48\ \mu\text{A}$$

Example 17.2

A common-emitter amplifier has $\beta = 100$, I_E(dc) = 2 mA and r_o = 40 kΩ, input V_i = 100 mV. Determine Z_i : I_b : $A_i = I_o/I_i$ and A_v if R_L = 1.25 kΩ.

Solution

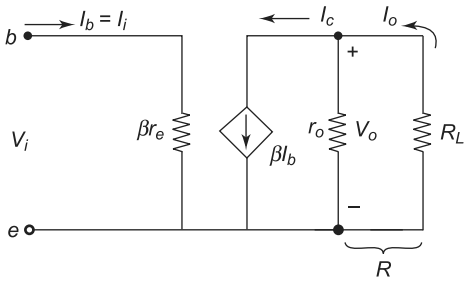


Fig. 17.13

CE amplifier (Fig. 17.13)

$$r_e = \frac{26\text{ mV}}{2} = 13\ \Omega$$

$$Z_i = \beta r_e = 100 \times 13 = 1.3\ \text{k}\Omega$$

$$V_i = 100\text{ mV}$$

$$I_i = I_b = \frac{100}{1300} = 0.077\text{ mA}$$

$$I_c = 100\ I_b = 7.7\text{ mA}$$

$$R = r_o \parallel R_L = \frac{40 \times 1.25}{40 + 1.25} = 1.21\ \text{k}\Omega$$

$$V_o = -I_c R = -7.7 \times 1.21 = -9.32\text{ V}$$

$$I_o = -\frac{9.32}{1.25} = 7.46\text{ mA}$$

$$A_i = \frac{I_o}{I_i} = \frac{7.46}{0.077} = 96.88\ (\text{slightly less than } \beta)$$

$$A_v = \frac{V_o}{V_i} = \frac{-9.32}{100 \times 10^{-3}} = -93.2$$

17.3.1 Small-Signal Model FETs and Amplifiers

The drain current of FET depends mainly on gate-to-source voltage related by the transfer characteristic JFET and DMOSFET. The relationship is the Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{17.5}$$

At the Q-point, the linearised (small-signal) relationship is given by

$$g_m = \frac{dI_D}{dV_{GS}} = \text{transconductance (S)} \tag{17.6}$$

In small-signal symbols,

$$I_d = g_m V_{gs} \tag{17.7}$$

By carrying out derivation of Eq. (17.5), it can be shown that

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right] \tag{17.8}$$

$|V_p|$ assures that g_m is a positive value.

At $V_{GS} = 0$, $$g_m = \frac{2I_{DSS}}{|V_P|} = g_{m0} \tag{17.9}$$

We can then write

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}} \tag{17.10}$$

❑ **Output Resistance** It is contributed by the slope of the drain characteristics at Q-point,

$$r_d = \left.\frac{dV_{DS}}{dI_D}\right|_{\text{at } V_{GS}} \tag{17.11}$$

or $$I_d = \frac{1}{r_d} V_{ds} \tag{17.12}$$

❑ **Circuit Model** Combining Eqs (17.7) and (17.12), we can write

$$I_d = g_m V_{gs} + \frac{1}{r_d} V_{ds} \tag{17.13}$$

From Eq. (17.16) and noting that $I_G = 0$, open circuit, circuit model is drawn in Fig. 17.14.

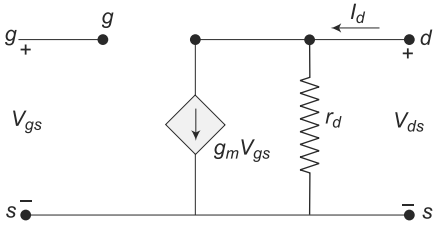


Fig. 17.14 *Circuit model of FET-common source*

EMOSFET

Its transfer characteristics is

$$I_D = k\,(V_{GS} - V_T)^2 \tag{17.14}$$

Taking derivative

$$g_m = 2k\,(V_{GS} - V_T) \tag{17.15}$$

or $$g_m = 2\sqrt{kI_D} \tag{17.16}$$

Example 17.3

For a JFET, calculate g_{m0}, other parameters are I_{DSS} = 15 mA , $V_p = -5$ V

Solution

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2 \times 15}{5} = 6 \text{ ms}$$

Example 17.4

The parameters of a JFET are g_{m0} = 5 ms and $V_p = -4$ V. What is the device current at V_{GS} = 0?

Solution

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$5 = \frac{2I_{DSS}}{4}$$

$$I_{DSS} = 10 \text{ mA} = I_D(\text{at } V_{as} = 0)$$

Example 17.5

A JFET has parameters I_{DSS} = 12 mA, $V_p = -6$ V. It is biased at $I_D = I_{DSS}/4$. What is its g_m at the *Q*-point?

Solution

$$I_D = 12/4 = 3\text{mA}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2 \times 12}{6} = 4 \text{ ms}$$

$$g_m = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}} = 4\sqrt{\frac{3}{12}} = 2 \text{ ms}$$

Example 17.6

A JFET has r_d = 100 kΩ and voltage gain of $A_v = -200$. What is the value of g_m?

Solution Refer common-source small-signal model of Fig. 17.14.

$$V_{ds} = -g_m V_{gs} r_d$$

Ideal gain, $$A_v = \frac{V_{ds}}{V_{gs}} = -g_m r_d = -200$$

$$g_m = \frac{200}{r_d} = \frac{200}{100} = 2 \text{ ms}$$

Example 17.7

For the transfer characteristics of Fig. 17.15, determine:
(a) g_{m0} (b) g_m at $V_{GS} = -1.5$ V (c) g_m at $V_{GS} = -2.5$ V

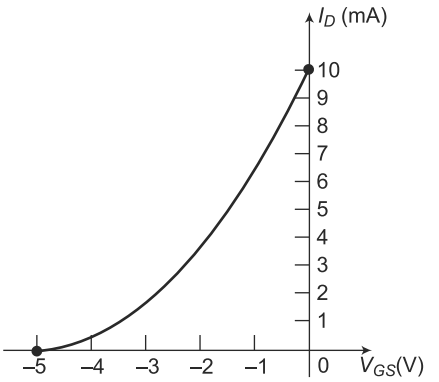


Fig. 17.15

Solution

(a) $I_{DSS} = 10$ mA. $V_p = -5$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{10}{5} = 2 \text{ mS}$$

(b) $V_{GS} = -1.5$ V

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_p}\right)$$

$$= 2\left(1 - \frac{1.5}{5}\right) = 1.4 \text{ mS}$$

(c) $V_{GS} = -2.5$

$$g_m = 2\left(1 - \frac{2.5}{5}\right) = 1 \text{ mS}$$

Remark: g_m reduces with increases of V_{GS}.

Example 17.8

For the JFET amplifier of Fig. 17.16, assume that the biasing circuit causes $V_{GSQ} = -3$ V. Determine: Z_i (input impedance) Z_0 (output impedance) and A_v (voltage gain).

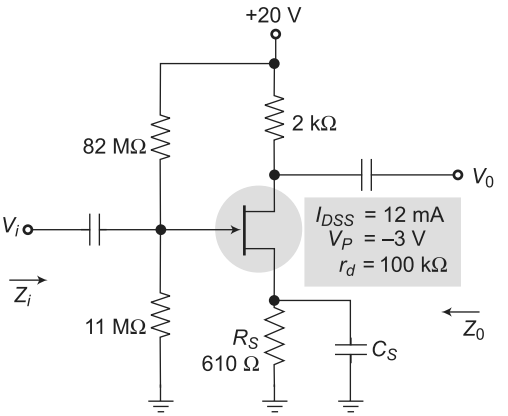


Fig. 17.16

Solution

Steps

- Replace all capacitors by short circuit. R_S gets eliminated.
- Make +20 V to zero and connect to ground.
- Replace JFET by its small-signal model.

The small-signal circuit in drawn in Fig. 17.17.

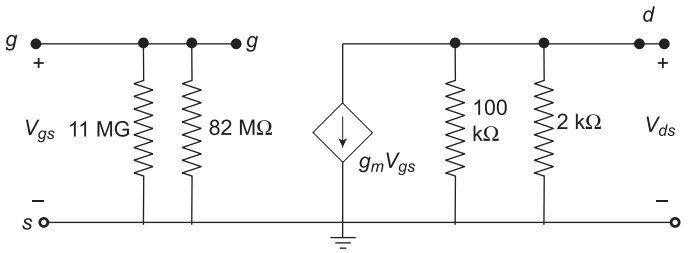


Fig. 17.17 *Small-signal circuit*

$$g_m = \frac{2I_{DSS}}{|V_p|}\left(1 - \frac{V_{GS}}{V_p}\right) = \frac{2 \times 12}{3}\left(1 - \frac{1.5}{3}\right) = 4 \text{ mS}$$

$$Z_i = \frac{82 \times 11}{82 + 11} = 9.7 \text{ M}\Omega$$

Open circuit input dependent current source open.

$$Z_0 = \frac{2 \times 100}{2 + 100} = 1.96 \text{ k}\Omega \quad r_d \text{ has very little effect}$$

$$V_0 = V_{ds} = -1.96\, g_m V_{gs}$$

$$V_i = V_{gs}$$

$$A_v = \frac{V_0}{V_i} = -1.96 g_s = -1.96 \times 4 = -7.81$$

Example 17.9

DMOSFET amplifier network is drawn in Fig. 17.18. The biasing (voltage divider) has been designed to place the *Q*-point at $V_{GSQ} = -1.2$ V and $I_{DQ} = 2.07$ mA.

(a) Determine g_{m0} and g_m.

(b) Sketch the small-signal equivalent circuit.

(c) Calculate Z_i and Z_0.

(d) Calculate A_v.

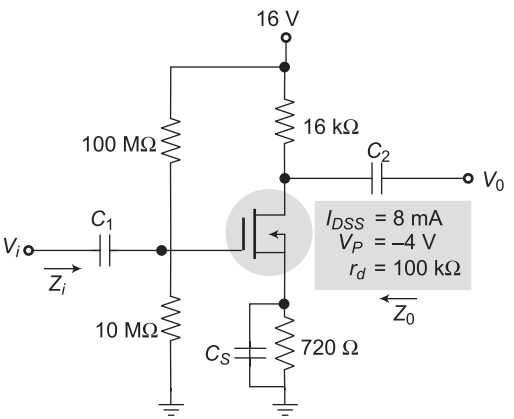


Fig. 17.18

Solution

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_p|} = \frac{2 \times 8}{4} = 4 \text{ mS}$$

$$g_m = 4\left(1 - \frac{1.2}{4}\right) = 5.71 \text{ mS}$$

(b) Small-signal equivalent is drawn is Fig. 17.19.

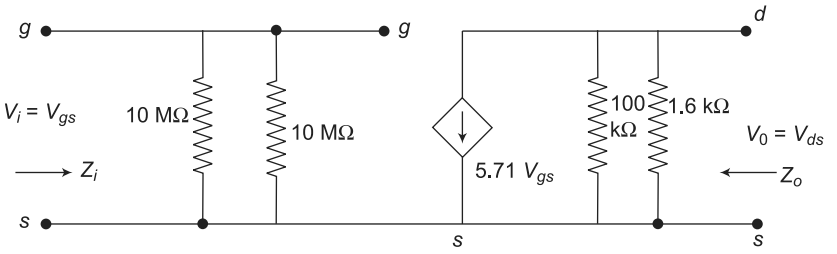


Fig. 17.19

(c) $Z_i = 10 \| 100 = 9.1\ \text{m}\Omega$

(d) $Z_0 = 1.6 \| 100\ \text{k}\Omega = 1.57\ \text{k}\Omega$

(e) $A_v = -g_m (r_d \| R_D)$

$= -5.71 \times 1.57 = -8.96$

17.3.2 Source Follower (Common Drain) Configuration

This corresponds to BJT's emitter follower. The circuit is drawn in Fig. 17.20. Its small-signal circuit equivalent is drawn in Fig. 17.21(a). It is redrawn in Fig. 17.21(b) in modified form.

$$V_{gs} = V_i - V_0$$

$$V_0 = g_m V_{gs} (r_d \| R_s)$$

$$= g_m (r_d \| R_s)\ (V_i - V_0)$$

$$[1 + g_m (r_d \| R_s)] V_0 = g_m (r_d \| R_s) V_{gs}$$

$$A_v = \frac{V_0}{V_i} = \frac{g_m (r_d \| R_s)}{1 + g_m (r_d \| R_s)}$$

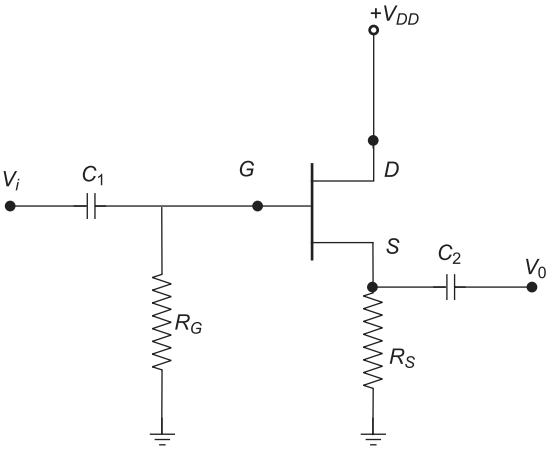


Fig. 17.20 *Emitter follower circuit*

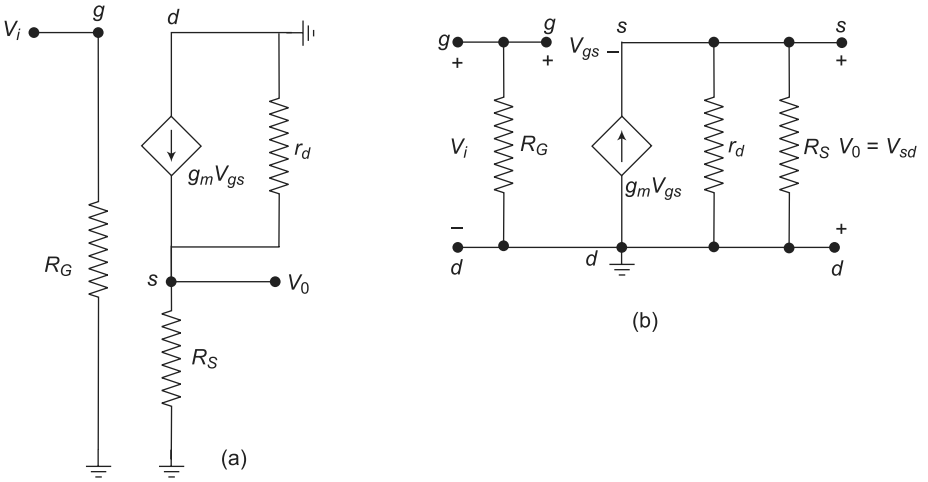


Fig. 17.21 *(a) Small-signal circuit equivalent (b) modified form*

Observation

$A_v < 1$, A_v positive, no phase reversal as in common-source $Z_i = R_G$.

To find Z_0,

Open-circuit voltage = V_0

Short-circuit current (s-d shorted),

$$I_{sc} = g_m V_{gs}$$

$$V_0 = \frac{g_m (r_d \parallel R_s) V_{gs}}{1 + g_m (r_d \parallel R_s)}$$

$$Z_0 = \frac{V_0}{I_{sc}} = \frac{g_m (r_d \parallel R_s)}{g_m [1 + g_m (r_d \parallel R_s)]} = \frac{1}{r_d \parallel R_s + g_m}$$

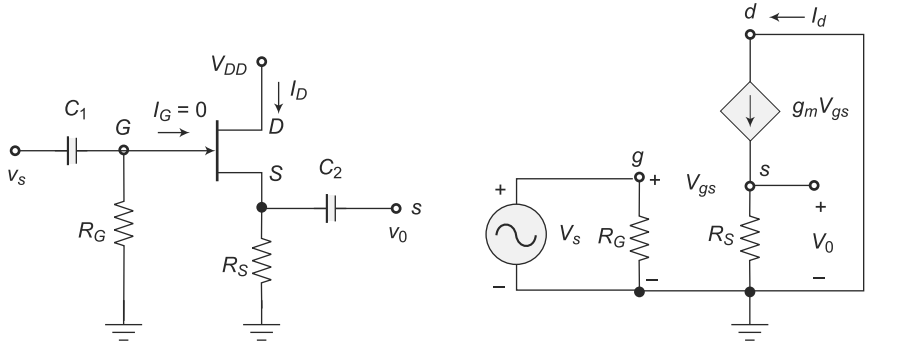
or
$$Z_0 = \frac{1}{\frac{1}{r_d} + \frac{1}{R_s} + g_m} \tag{17.18}$$

Example 17.10

For the source-follower of Fig. 17.22,

I_{DSS} = 16 mA, V_p = −4 V, R_G = 1 MΩ, R_s = 2.2 kΩ, V_{DD} = +9 V

Calculate the voltage gain, and output impedances.



(a) Source-follower (b) Small-signal model of source-follower

Fig. 17.22

Solution dc bias conditions

Assume $I_G = 0$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{i}$$

$$V_{GS} = -R_S I_D \tag{ii}$$

Substituting values,

$$I_D = 16\left(1 + \frac{V_{GS}}{4}\right)^2 \quad \text{(iii)}$$

$$V_{GS} = -2.2\, I_D \quad \text{(iv)}$$

Substituting I_D from Eq. (iv) in Eq. (iii),

$$I_D = 16\left(1 - \frac{2.2 I_D}{4}\right)^2$$

or $$I_D^2 - 3.84\, I_D + 3.31 = 0$$

or $$I_D = 1.3 \text{ mA or } 2.54\text{mA}$$

The second value is rejected as its gives V_{GS} more negative than V_P (pinch-off voltage). Thus,

$$I_D = 1.3 \text{ mA}$$

$$V_{GS} = -2.2 \times 1.305 = -2.86 \text{ V}$$

$$g_{m0} = -\frac{2I_{DSS}}{V_P} = 2 \times \frac{16}{4} = 8 \text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = 8\left(1 - \frac{286}{4}\right) = 2.28 \text{ mS}$$

$$r_m = \frac{1}{g_m} = 0.439 \text{ k}\Omega$$

$$A_V = \frac{2.2 \times 2.28}{1 + 2.2 \times 2.28} = 0.834 \ (< 1)$$

$$Z_i = R_G = 1 \text{ M}\Omega$$

$$Z_0 = R_S \| r_m = 2.2 \| 0.439 = 365\ \Omega \text{ [very low]}$$

Note: r_d is ignored.

EMOSFET

The relationship between drain current and controlling voltage is

$$I_D = k(V_{GS} - V_T)^2 \quad (17.19)$$

Taking derivation wrt $V_{GS,}$

$$g_m = 2k(V_{GS} - V_T) \quad (17.20)$$

g_m has to be evaluated at V_{GSQ} (Q-point)

Example 17.11

Determine g_m if $V_T = 4$ V and $V_{GSQ} = 8$ V. Take $k = 3.5/\text{V}^2$

Solution

$$g_m = 2 \times 3.5(8 - 4) = 20 \text{ mS}$$

Example 17.12

For the amplifier of Fig. 17.23, EMOSFET data is

$V_T = 3$ V, $k = 0.4$ mA/V^2

$r_d = 40$ kΩ

Find the voltage gain A_v.

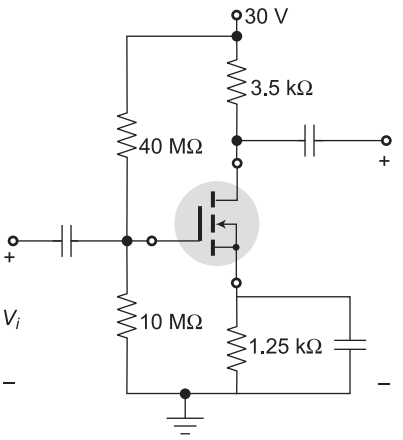


Fig. 17.23

Solution For ac signal analysis, we need V_{GSQ} for determining g_m. We carry out dc analysis by upon short circuiting all capacitors. Note that $I_G = 0$

$$V_G = 30 \times \frac{10}{10+40} = 6 \text{ V}$$

$$I_D = k(V_{GS} - V_T)^2 = 0.4(V_{GS} - 3)^2 \quad \text{(i)}$$

$$V_{GS} = V_G - I_S R_S = 6 - 1.25\, I_D \quad \text{(ii)}$$

$$V_{GS} = 0 \rightarrow I_D = \frac{6}{1.25} = 4.8 \text{ mA}$$

$$I_D = 0 \rightarrow V_{GS} = 6 \text{ V}$$

Equations (i) and (ii) are plotted in Fig. 17.24. Their intersection gives $V_{GSQ} = 4.7$ mV

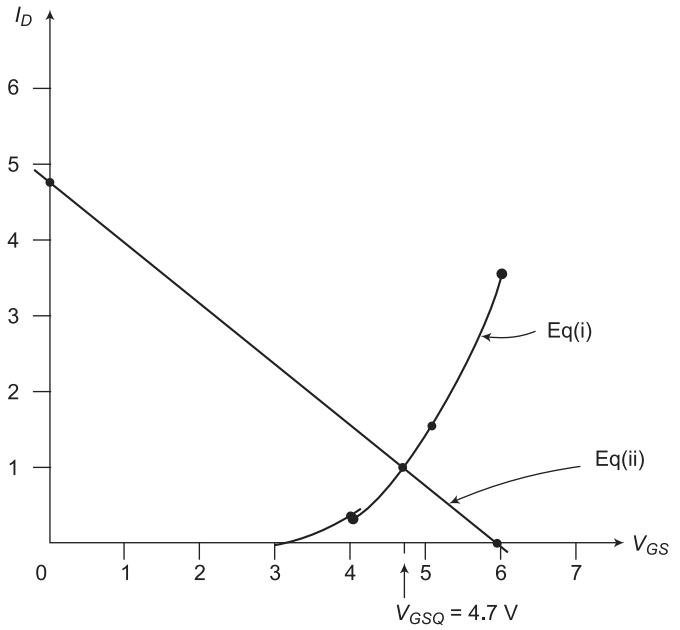


Fig. 17.24

We now find

$$g_m = 2k(V_{GSQ} - V_T)$$

$$= 2 \times 0.4\,(4.7 - 3) = 1.36 \text{ mS}$$

The ac signal circuit of the amplifier is drown in Fig. 17.25.

$$V_0 = -g_m V_{gs}\,(40 \| 3.5)$$

$$V_{gs} = V_i$$

$$V_0 = -1.36\,(40 \| 3.5) V_i$$

$$A_v = \frac{V_0}{V_i} = -4.38$$

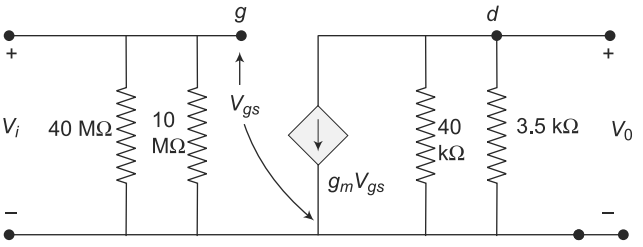


Fig. 17.25

Effect of Source Resistance and Load Resistance

Treatment is similar to that of BJT based amplifier

$$\frac{V_i}{V_s} < \frac{V_p}{V_i}$$

17.4 CE BJT AMPLIFIER

A small-signal BJT amplifier with voltage divider bias is drawn in Fig. 17.26. In the range of frequencies called *midband*, the coupling capacitors act as short circuits ($1/C\omega \approx 0$). Thereby, the input and output signals are connected directly to the BJT. Also, the *bypass* capacitor acts as a short across R_E. This is needed, otherwise R_E would provide negative feedback reducing the small-signal gain of the amplifier.

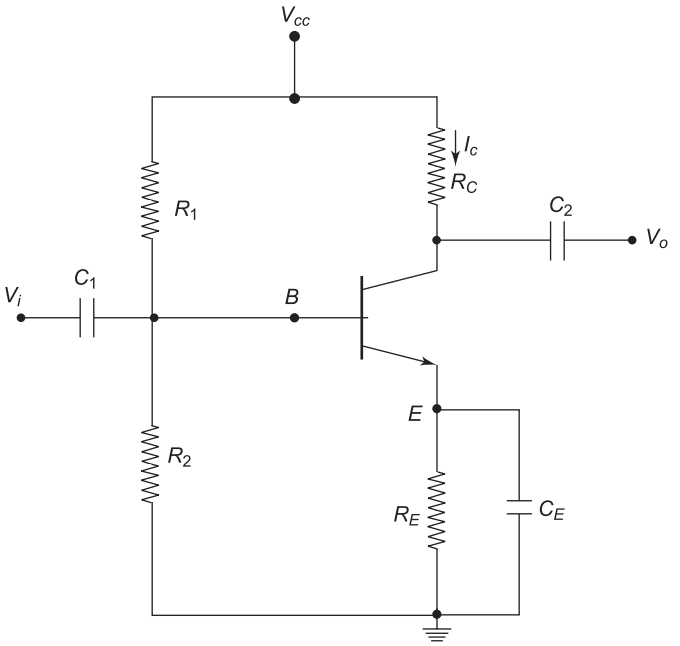


Fig. 17.26 *CE amplifier*

The small-signal circuit equivalent of the amplifier is drawn in Fig. 17.27.

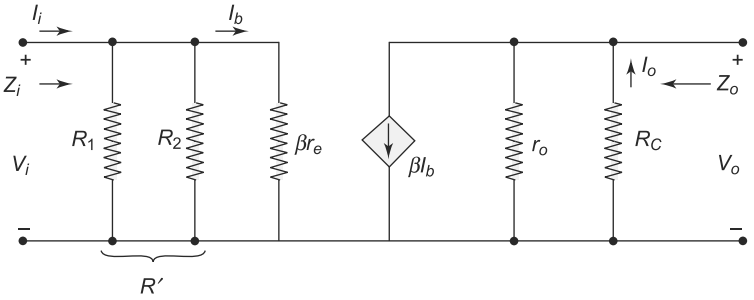


Fig. 17.27 *Small-signal circuit equivalent*

Circuit Analysis

Input impedance

$$Z_i = R_1 \parallel R_2 \parallel \beta r_e$$

Output impedance

$$Z_o = r_o \parallel R_C \approx R_C \text{ as } r_o \geq 10\, R_c$$

Voltage Gain

$$I_i = \frac{V_i}{R \parallel \beta r_e}$$

Output impedance – Short-circuit input

The $Z_o = r_o \parallel R_c$

$$V_o = -\beta I_b Z_o$$

$$= -\beta\left(\frac{V_i}{\beta r_e}\right) Z_o = -\left(\frac{V_i}{r_e}\right) Z_o$$

$$A_v = \frac{V_i}{V_o} = -\frac{Z_o}{r_e} = -\frac{r_o \parallel R_c}{r_e} \tag{17.21a}$$

or $$A_v = -\frac{R_c}{r_e} \text{ for } r_o \geq 10\, R_c \tag{17.21b}$$

Current Gain

$$I_o = \beta I_b\left(\frac{r_o}{r_o + R_c}\right) \Rightarrow \frac{I_o}{I_b} = \frac{\beta r_o}{(r_o + R_c)}$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$I_i = I_b + \frac{V_i}{R'}$$

$$= I_b + \left(\frac{\beta r_e}{R'}\right) I_b = \left(\frac{R' + \beta r_e}{R'}\right) I_b$$

or $$\frac{I_b}{I_i} = \left(\frac{R'}{R' + \beta r_e}\right)$$

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b} \cdot \frac{I_b}{I_i} = \frac{R' \beta r_e}{(r_o + R_c)(R' + \beta r_e)} \tag{17.22}$$

❑ To Sum Up

- From the *RC*-coupled amplifier circuit, draw the small-signal circuit.
- From the biasing analysis, find I_E (dc).
- Compute $r_e = \dfrac{26 \text{ mA}}{I_E}$
- The transition β is known from manufacturing data.
- Z_i, Z_o, A_v and A_i are now computed for the small-signal circuit.

The expressions for these have been derived earlier.

Example 17.13

For the BJT amplifier of Fig. 17.28, draw the small-signal models and determine there from Z_i, Z_o, A_v, A_i.

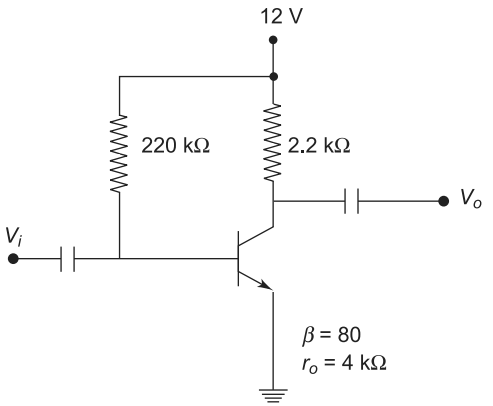


Fig. 17.28

Solution The dc analysis (capacitor open circuit)

$$I_B = \frac{12 - 0.7}{220} = 0.051 \text{ mA}$$

$$I_E \approx I_C = 80 \times 0.051 = 4.08 \text{ mA}$$

$$r_e = \frac{26}{4.08} = 6.37\ \Omega$$

$$\beta r_e = 80 \times 6.37$$

$$= 509.6\ \Omega = 0.51\ \text{k}\Omega$$

Small-signal model (Fig. 17.29)

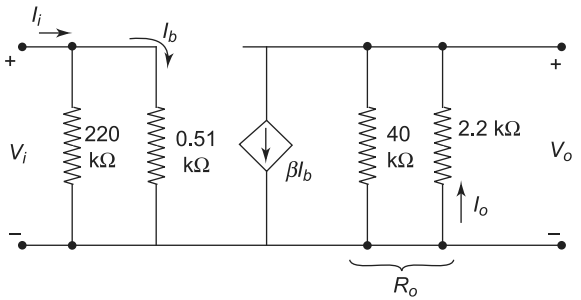


Fig. 17.29

$$R_o = \frac{2.2 \times 40}{2.2 + 40} = 2.085\ \text{k}\Omega$$

$$Z_i = 0.51\ \text{k}\Omega;\ 220\ \text{k}\Omega \text{ ignored}$$

Short input, βI_b open circuit

$$Z_o = R_o = 2.085\ \text{k}\Omega$$

Let $V_i = 1\text{V}$ (for convenience)

$$I_b = \frac{1}{0.51},\ \beta I_b = \frac{80}{0.51} = 157\ \text{mA}$$

$$V_a = -\frac{80}{0.51} \times 2.085 = -327\ \text{V}$$

$$A_V = -327$$

Output current

$$I_o = 157 \times \frac{40}{2.2 + 40} = 148.8\ \text{mA}$$

Current gain

$$A_i = \frac{I_o}{I_b} = \frac{148.8}{1/0.51} = 75.9 \quad I_b \approx I_c$$

Example 17.14

Draw the small-signal of the amplifier circuit of Fig. 17.30. Determine Z_i, Z_o, A_v, A_i. The dc analysis yields I_E = 1.38 mA. All resistance are in kΩ.

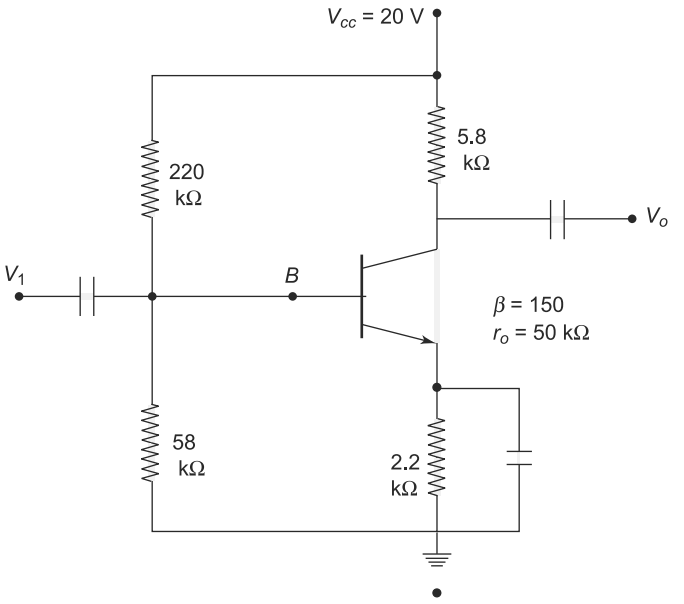


Fig. 17.30

Solution

$$r_e = \frac{26}{1.38} = 18.84\ \Omega$$

$$\beta r_e = 2.826\ \text{k}\Omega$$

The small-signal model is drawn Fig. 17.31.

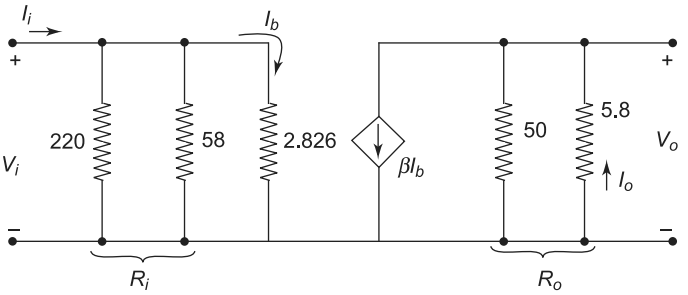


Fig. 17.31

Let V_i = 1 V (for convenience)

$$I_b = \frac{1}{2.826} = 0.354\ \text{mA}$$

$$\beta I_b = 150 \times 0.354 = 53.1\ \text{mA}$$

$$R_o = 50 \parallel 5.8 = 5.2\ \text{k}\Omega$$

$$V_o = -53.1 \times 5.2 = -276\ \text{V}$$

$$A_V = -276$$

$$R_i = 220 \| 58 \| 2.826 = 45.9 \| 2.826 = 2.66 \text{ k}\Omega$$

$$I_i = \frac{1}{2.66} = 0.376 \text{ mA}$$

$$I_o = 53.1 \times \frac{50}{50 + 5.8} = 47.6 \text{ mA}$$

$$A_i = \frac{47.6}{0.376} = 126.6$$

$$Z_i = R_i = 2.66 \text{ k}\Omega$$

$$Z_o = R_o = 5.2 \text{ k}\Omega$$

17.5 EFFECT OF SOURCE AND LOAD RESISTANCE

A real voltage source which feeds the amplifier has a series resistance as shown Fig. 17.32(a). The series voltage drop reduces V_i fed to the amplifier.

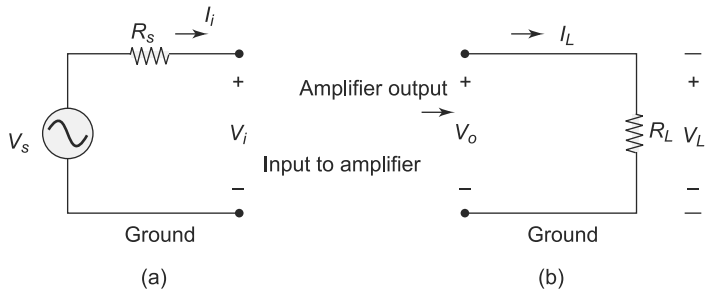


Fig. 17.32 *Voltage source*

The voltage amplifier as the output feeds a load, which is a shunt connector, as shown in Fig. 17.32(b). R_L is in shunt with $r_o \| R_c \approx R_c$. The output voltage

$$V_L = \beta I_b (R_c \| R_L) \text{ which is less than } V_0 = \beta I_b R_c \text{ as } R_c \| R_L < R_c$$

The overall affect of source and load resistance is to reduce the net voltage gain of the amplifier.

The ac circuit of a voltage-divider biased CE amplifier fed from a source and feeding a load is drawn in Fig. 17.33.

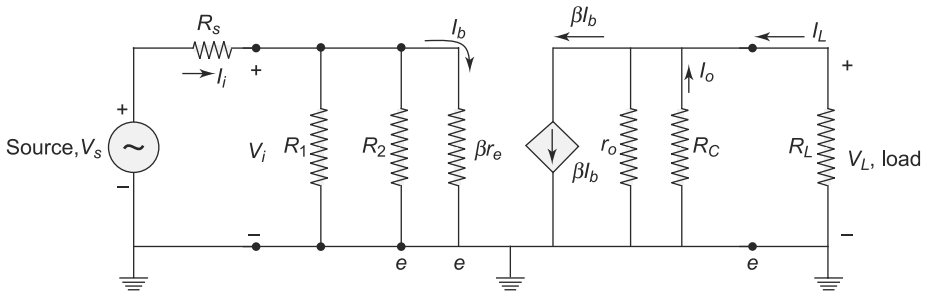


Fig. 17.33 *ac circuit of voltage-divider biased CE amplifier*

It is easy to see that $V_i < V_s$ and $I_L < \beta I_b$. The overall amplifier gain is

$$A_v(\text{overall}) = \frac{V_L}{V_s} < \frac{V_o}{V_i}, \; V_o \text{ is found by disconnecting } R_L$$

17.6 FREQUENCY RESPONSE

So far we have studied the BJT *RC*-coupled small signal amplifiers in the mid-band range of frequencies. In the mid-band, the capacitors are effective short circuits and the amplifier's mid-band gain is constant. Also, in the high-frequency end of mid-band, the transistor capacitances are in shunt but act as open circuits.

Let us now consider the frequency response of amplifiers at low frequencies end of mid-band and also at high-frequency end of mid-band.

The effect of coupling capacitors is *R*C series wherein the voltage drop in capacitive reactance ($1/2\pi fC$) increases as the signal frequency reduces; resulting in gain reduction. The bypass capacitor across (R_E or R_S) is a shunt effect (C in parallel with R). As the capacitive reactance increases with lower signal frequency, the effectiveness of bypassing reduces causing increase in negative voltage feedback and so gain reduction.

At high–frequency, the device capacitances—inter-terminal, stray (wiring, etc.) and load capacitance—are effectively in shunt (C in parallel with R). At high frequencies, ($1/2\pi fC$) decreases and so, the shunt effect reduces the gain. A typical frequency response is plotted to scale in log frequency in Fig. 17.34.

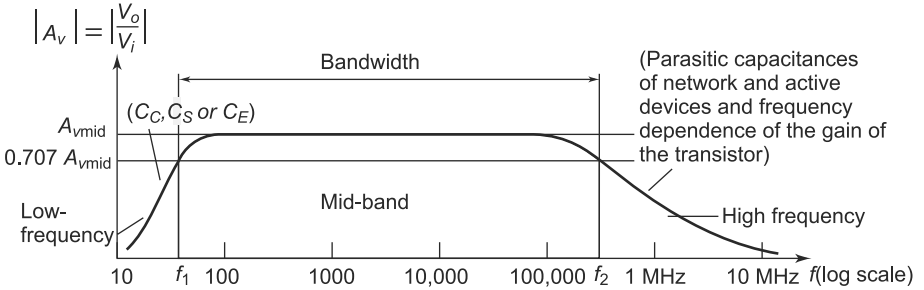


Fig. 17.34 *Typical frequency response of RC-coupled amplifier*

As f_1 is very small, BW $\approx f_2$ (17.23a)

Decibel (dB)

It is 1/10th of bel. It is defined as gain

$$G_{\text{dB}} = 10 \log \frac{P_2}{P_1} \tag{17.23b}$$

where P_2 and P_1 are two equipment power being compared.

It is advantageous to take P_1 as reference power. It is taken as

1 mW, for 600 Ω

Thus, $$G_{\text{dB}m} = \left.\frac{P}{1\,\text{mW}}\right|_{\text{at } 600\Omega} \tag{17.24}$$

For ratio of voltage (voltage gain, amplification), for a given R

$$P_2 = V_2^2/R, \; P_1 = V_1^2/R$$

Then $$G_{\text{dB}} = 10 \log \left(\frac{V_2}{V_1} \right)^2 = 20 \log \frac{V_2}{V_1} \tag{17.25}$$

At least frequency, the gain reduces by $(1/\sqrt{2})$. In dB scale

$$\text{dB}\left(\frac{1}{\sqrt{2}} \right) = 20 \log \frac{1}{\sqrt{2}} = -3 \text{ dB} \tag{17.26}$$

Thus, at least frequency, gain drops by 3 dB.

17.7 LOW-FREQUENCY RESPONSE

The frequency response of C_s (input side) and C_c (output side) can be simulated by the simple circuit of Fig. 17.35(a). The circuit is redrawn in frequency domain in Fig. 17.35(b). By voltage division,

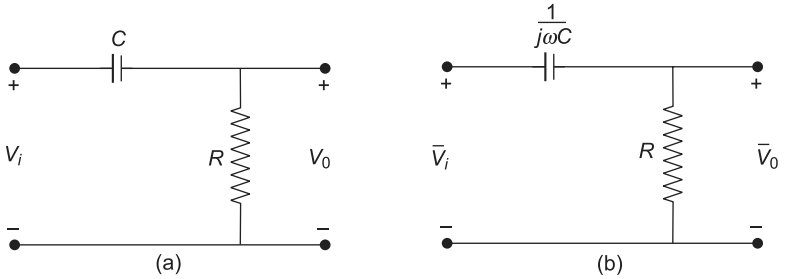


Fig. 17.35 *(a) RC circuit (b) RC circuit in frequency domain*

$$\bar{V}_0 = \left(\frac{R}{R + \frac{1}{j\omega c}} \right) \bar{V}$$

The circuit gain (complex) is

$$\bar{A}_v = \frac{\bar{V}_0}{\bar{V}_i} = \frac{1}{1 - j(1/\omega CR)}$$

or $$\bar{A}_v = \frac{1}{(1 - j(\omega_1/\omega))} \tag{17.27}$$

where $\omega_1 = \dfrac{1}{CR}$ or $f_1 = \dfrac{1}{2\pi CR}$; *break frequency* (17.28)

We can write

$$\bar{A}_V = \frac{1}{1 - j(f_1/f)} \tag{17.29}$$

$$dB \left| \bar{A}_v \right| = 20 \log \frac{1}{\sqrt{1 + (f_1/f)^2}}$$

For $f >> f_1$, dB $\left|\bar{A}_v\right| = 20 \log 1 = 8$ dB, asymptote

For $f << f_1$, dB $\left|\bar{A}_v\right| = -20 \log(f_1 / f)$, asymptote slope + 20 dB/decade as f decreases

At $f = f_1$, dB $\left|\bar{A}_v\right| = 20 \log \frac{1}{\sqrt{2}} = -3$ dB

The asymptote and corrected dB log f (Bode plot) is drawn in Fig. 17.36.

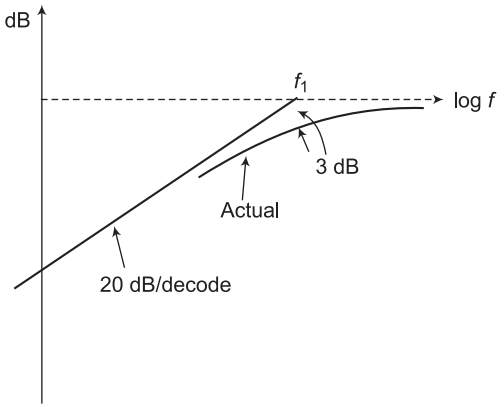


Fig. 17.36 *Bode plot*

Low Frequency Response BJT Amplifier

From small-signal equivalents.

❑ **Input Side (C_s)** The input side small-signal circuit retaining C_s is drawn in Fig. 17.37. If follows that

$$\bar{V}_a = \left[\frac{R_i}{(R_s + R_i) - jX_c}\right] V_s \tag{17.30(a)}$$

Break frequency from Eq. 17.28,

$$f_{Li} = \frac{1}{2\pi(R_s + R_i)C} \tag{17.30(b)}$$

❑ **Output Side (C_c)** The output side small-signal circuit retaining C_c is drawn in Fig. 17.38. The break frequency

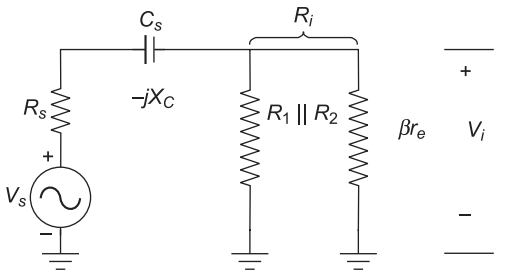


Fig. 17.37 *Input side*

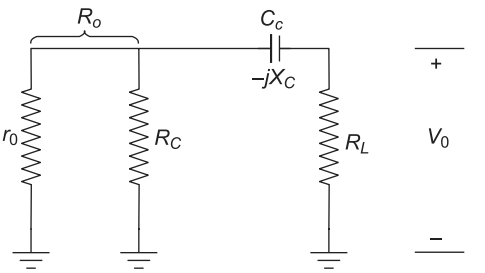


Fig. 17.38 *Output side*

$$f_{L0} = \frac{1}{2\pi(R_0 + R_L)C_c} > R_0 \approx R_c \tag{17.31}$$

❑ **Emitter Circuit (R_E || C_E)** If can the shown by certain assumptions that

$$F_{LE} = \frac{1}{2\pi\, R_e C_E} \tag{17.32}$$

where $R_e = R_E \| \left(\frac{R'_s}{\beta} + r_e \right)$

$R'_s = R_s \| R_1 \| R_2$

If low frequency and there are three break frequencies (not coincident). The slope of Bode plot beyond lowest break frequency is then –3 × 20 = –60 dB/decade. Highest of the three is the break frequency f_1.

Low Frequency Response JFET Amplifier

If can be similarly shown that

$$f_{L_i} = \frac{1}{2\pi(R_s + R_c)C_c} \tag{17.33}$$

$$f_{L_0} = \frac{1}{2\pi(R_a + R_L)C_c} \tag{17.34}$$

$R_0 = R_D \| Z_d$

$$f_{Ls} = \frac{1}{2\pi R_{\text{eq}} C_s} \tag{17.35}$$

$R_{\text{eq}} = R_s \| \frac{1}{g_m}.r_d$ ignored

17.8 HIGH-FREQUENCY RESPONSE

The effect of device capacitances, stray capacitance and load capacitance can be lumped as shunt capacitance C_i in input side and C_0 on output side. Of course, coupling and bypass capacitors are more effective short circuit. Thus, the input and output circuits have the terms as of Fig. 17.39 from which it follows that

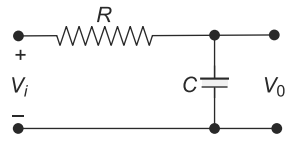


Fig. 17.39 *High-frequency response*

$$\bar{V}_0 = \left(\frac{-jX_C}{R - jX_C} \right) \bar{V}_i$$

$$\frac{-jX_C}{R - jX_C} = \frac{1}{1 + j\frac{R}{X_c}} = \frac{1}{1 + j\omega R} = \frac{1}{1 + j(f/f_2)}$$

Break frequency, $f_2 = \frac{1}{2\pi RC}$ (17.36)

Asymptote slope = –20 dB/decade as shown in Fig. 17.40.

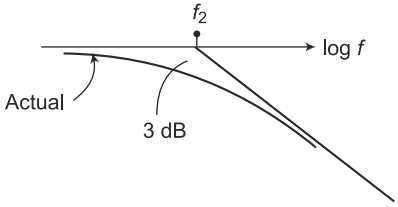


Fig. 17.40 *Asymptote slope*

High-Frequency Response

❑ **BJT** The ac circuit of high frequency is shown in Fig. 17.41, the coupling and bypass capacitors are shorts.

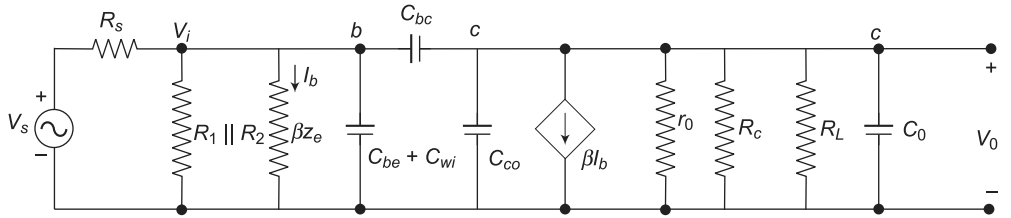


Fig. 17.41 *BJTCE amplifier ac circuit at high frequencies*

Various capacitances are

- Device capacitances C_{be}, C_{bc}, C_{ce}
- Stray wiring capacitances C_{wi} (input side) C_{wo} (output side)
- Load capacitances, C_L

The capacitances C_{bc} is converted to C_{mi} input side and C_{mo} output side by application of Miller theorem (not taken in this text)

Net input capacitances, $C_i = C_{wi} + C_{bc} + C_{mi}$

Net output side capacitances, $C_0 = C_{w0} + C_{ce} + C_{mo}$, C_{ce} is of negligible orders.

The resistances are combined by Thevenine theorem as

$$R_{THi} = R_r \parallel R_1 \parallel R_2 \parallel \beta r_e$$

$$R_{H0} = r_0 \parallel R_c \parallel R_L$$

The Thevenin equivalent circuit is drawn in Fig. 17.42.

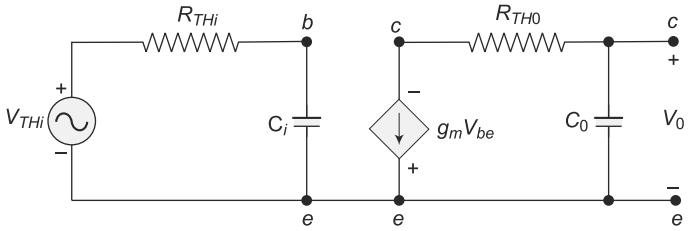


Fig. 17.42 *Thevenin equivalent circuit*

The break frequencies are then

$$f_{Hi} = \frac{1}{2\pi R_{THi} C_i} \tag{17.37}$$

and

$$f_{H0} = \frac{1}{2\pi R_{TH0} C_0} \tag{17.38}$$

❑ **FET** If can be similarly shown that

$$f_{Hi} = \frac{1}{2\pi R_{THi} C_i}$$

where $R_{THi} = R_s \parallel R_G$

$C_i = C_{wi} + C_{gs} + C_{mi}$

and $$f_{H0} = \frac{1}{2\pi R_{TH0} C_i}$$

where $R_{TH0} = R_s \parallel R_D \parallel r_d$

$C_0 = C_{w0} + C_{ds} + C_{m0,}$ C_{ds} in of negligible order C_{mi} and C_{m0} arise from C_{gd}.

Example 17.15

The circuit analysis of a BJT RC coupled amplifier is drawn in Fig. 17.43. The data given

V_{CC} = 20 V

R_1 = 220 kΩ. R_2 = 58 Ω

R_E = 2.2 kΩ. R_c = 5.8 kΩ

β = 150. R_s = 1 kΩ

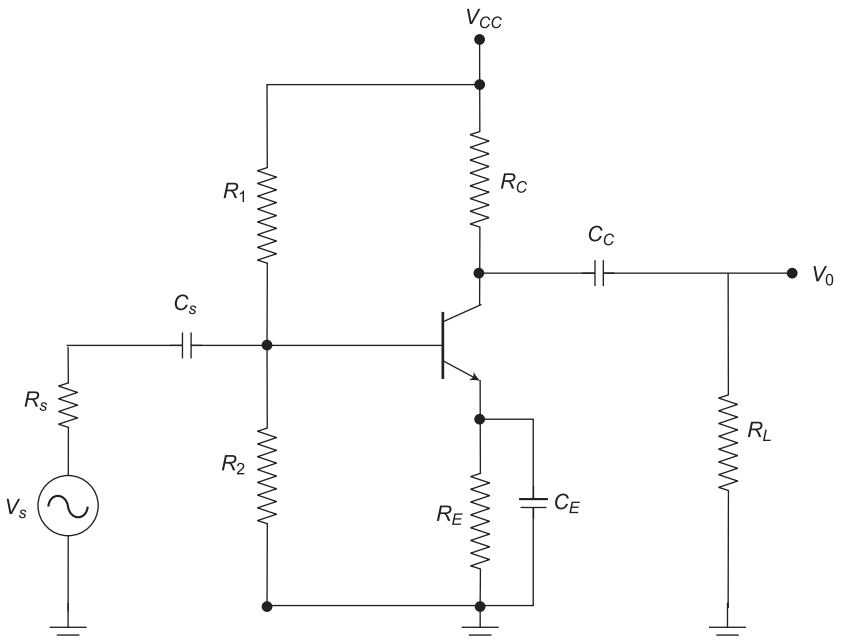


Fig. 17.43

Solution *dc analysis yields*

$$I_E = 1.38 \text{ mA}$$

$$r_e = \frac{26}{1.38} = 18.84\ \Omega$$

$$\beta r_e = 150 \times 18.84 = 2.864 \text{ k}\Omega$$

$$C_s = 10\ \mu\text{F},\ C_c = 1\ \mu\text{F},\ C_E = 20\ \mu\text{F}$$

Mid-band gain $A_v = \dfrac{V_0}{V_i} = \dfrac{-R_c \parallel R_L}{r_e} = -\dfrac{\dfrac{5.8 \times 2.2}{5.8 + 2.2}}{18.84 \times 10^{-3}} = -84.7$

$$Z_i = R_1 \parallel R_L \parallel \beta Z_e = \frac{1}{\frac{1}{220} + \frac{1}{5.8} + \frac{1}{2.864}} = 1.9 \text{ k}\Omega$$

$$\frac{V_i}{V_s} = \frac{1.9}{1 + 1.9} = 0.655$$

$$A_{vs} = \frac{V_0}{V_i} = -84.7 \times 0.655 = -55.5$$

Low-frequency breaks

$$f_{Ls} = \frac{1}{2\pi(R_s + R_i)C_s} = \frac{10^6}{2\pi(2 + 1.9) \times 10^3 \times 10} = 5.5 \text{ Hz}$$

$$f_{L0} = \frac{1}{2\pi(R_c + R_L)C_c} = \frac{10^6}{2\pi(5.8 + 2.2) \times 10^3 \times 1} = 20 \text{ Hz}$$

$$f_{LE} = \frac{1}{2\pi R_e C_E} = \frac{10^6}{2\pi \times 24.5 \times 20} = 325 \text{ Hz}$$

R_e is compiled below

$$R_e = R_E \parallel \left(\frac{R_s}{\beta} + r_e \right),\ R_s' = R_s \parallel R_1 \parallel R_2 = \frac{1}{\frac{1}{1} + \frac{1}{220} + \frac{1}{5.8}} = 0.85 \text{ k}\Omega$$

$$= \frac{2.2 \times 10^3 \times 24.5}{2.2 \times 10^3 + 24.5},\ \frac{R_s'}{\beta} = \frac{0.85}{150} = 5.7\ \Omega,\ \frac{R_s'}{\beta} + r_e = 5.7 + 18.84 = 24.5\ \Omega$$

$$= 24.23\ \Omega$$

Therefore, for bandwidth calculations $f_1 = 325$ Hz (highest of the three break frequencies)

Example 17.16

The circuit of a DMOSFET is drawn in Fig. 17.44. The data is an in Example 17.6 repeated below.

$R_1 = 100$ MΩ, $R_2 = 10$ MΩ, $R_D = 1.6$ kΩ, $R_S = 720$ Ω, $V_{DD} = 16$ V

As found in Example 17.6,

$g_m = 5.7$ mS

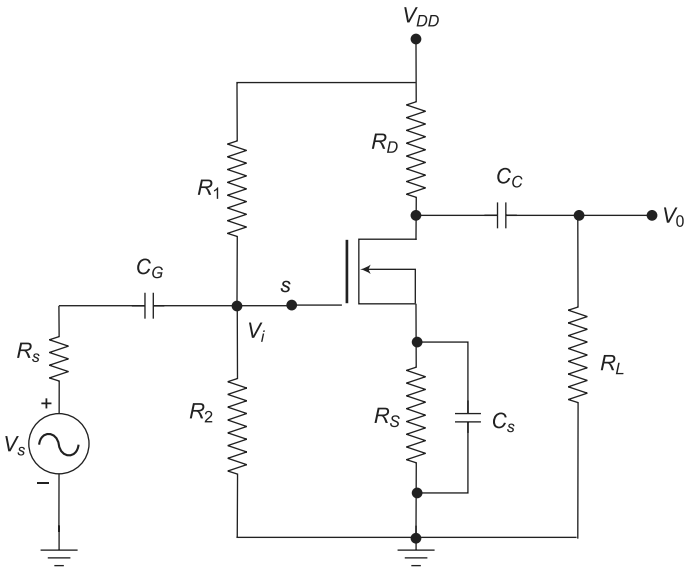


Fig. 17.44

Additional data:

R_S = 10 kΩ, $r_d = \infty$, R_1 = 2.2 kΩ, C_G = 0.01 μF, C_c = 0.5 μF, C_s = 2 μF

Determine the corner frequencies in the low frequency end.

Solution

$$R_1 \| R_2 = \frac{100 \times 10}{110} = 9.1\ \text{M}\Omega$$

$$f_{LG} = \frac{1}{2\pi(R + \text{R}_1 \| \text{R}_2)C_G} = \frac{10^6}{2\pi \times 9.1 \times 10^6 \times 0.01} = 1.75\ \text{Hz}$$

$$f_{L0} = \frac{1}{2\pi(R_D + \text{R}_1)C_C} = \frac{10^6}{2\pi\,(1.6 + 2.2) \times 10^3 \times 0.51} = 83.7\ \text{Hz}$$

$$f_{LS} = \frac{1}{2\pi R_{eq} C_s} = \frac{10^6}{2\pi \times 0.141 \times 10^3 \times 2} = 564\ \text{Hz}$$

$$R_{\text{eq}} = R_s \| \frac{1}{g_m} = 0.72 \| \frac{1}{5.7} = 0.72 \| 0.175 = 0.141\ \text{k}\Omega$$

Thus, low-frequency break is $f_1 = f_{LS} = 564$ Hz

Summary

➢ BJT and amplifiers are introduced. Anlaysis of different configurations are carried out. Current and voltage gain are calculated. Frequency response is discussed.

Exercises

Review Questions

1. Derive the expressions of 'voltage gain', 'current gain', 'input impedance' and 'output impedance', for a BJT using low frequency *h*-parameter model for (a) *CE* configuration, (b) *CB* configuration and (c) *CC* configuration.
2. Compare the performance of a BJT as an amplifier in *CE*, *CB* and *CC* configuration.
3. Derive the expressions of 'voltage gain', 'current gain', 'input impedance' and 'output impedance'. For a BJT using the approximation *h*-parameter model for (a) *CE* configuration, (b) *CB* configuration, and (c) *CC* configuration.
4. What is an amplifier? What are the various types of amplifiers?
5. Draw the circuit diagram of a *CE* amplifier and explain its working.
6. Draw the ac equivalent of a *CE* amplifier with fixed-bias using *h*-parameter model and 'r_e' model and derive the equations for input impedance, voltage gain and current gain.
7. Draw the ac equivalent circuit of a *CE* amplifier with 'voltage divider' bias using *h*-parameters model and r_e model and also derive the equations for 'input impedance' and 'voltage gain'.
8. Draw the small-signal model of BJT for low frequency and high-frequency regions.
9. Justify the validity of approximate hybrid model applicable in low-frequency regions.
10. Draw the r_e model for a BJT in *CE* configurations and derive the equations for voltage gain and current gain.
11. A *CE* amplifier is drawn by a voltage source of internal resistance $R_s = 1000\ \Omega$ and the load impedance is a resistance 'R_L' = 1200 Ω. The *h*-parameters are $h_{ie} = 1.2$ kΩ, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 60$ and $h_{oe} = 25$ μA/V. Compute the current gain A_I, input resistance R_i, voltage gain A_v and output resistance R_o using exact analysis.
12. A *CE* amplifier stage uses an *NPN* transistor having $\beta_o = 125$ and is biased at $I_{CQ} = 1$ mA. If $R_s = 300\ \Omega$, $R_c = 1.2$ kΩ, determine A_v and R_i.
13. For any single-stage amplifier, prove that, $\left[R_i = \dfrac{h_i}{1 - h_r A_v} \right]$
14. Draw the ac equivalent circuit of *CE* and *CC* amplifiers subject to $R_L = 0$. Show that the input impedances of the two circuits are identical.
15. Which of the three BJT configurations has (a) highest R_i, (b) lowest R_i, (c) highest R_o, (d) lowest R_o, (e) highest A_v, and (f) lowest A_v?
16. What is meant by-frequency response of a voltage amplifier?
17. Explain the meaning of a break frequency as half-power frequency.
18. What is meant by-bandwidth of an amplifier? What is its significance?
19. What are low-frequency breaks and their censes?
20. What are the causes of high-frequency breaks?
21. How much is the dB gain drop at break frequency?
22. Draw the BJT amplifier's ac circuit showing all elements. Identify the capacitors which effect the low-frequency response and those which effect the high-frequency response. Explain why.
23. Repeat Question 22 for an FET amplifier.
24. How is capacitance connecting *b* and *c* in BJT amplifier ac circuit for finding high-frequency break.
25. Repeat Question 24 for FET amplifier for capacitance connecting *d* and *s*.
26. Draw the small-signal model of common base configuration.
27. How do you find the value of r_e base-emitter resistance?
28. Draw the small-signal model of common-emitter configuration. What is the meaning of each circuit element? What is output resistance r_o?

29. Outline the steps in a determining the ac gain of a BJT based CE amplifier. Why do we need the biasing (dc) analysis of the circuit?
30. What is an *RC*-coupled amplifier?
31. In ac analysis of an *RC* coupled amplifier, the coupling capacitors and by-pass capacitors can be assumed to the short circuit in mid band frequencies. Elaborate.
32. In a CE-amplifier, the output is phase reversed. Elaborate.
33. What is an emitter follower? How is it different from a CE amplifier? What are its applications?
34. What is g_m, transconductance?
35. Write the expression for g_m for JFET, DMOSFET and EMOSFE. Elaborate the symbols used.
36. What contributors the output resistance r_d?
37. Draw the common source circuit model FETs.
38. Draw the circuit of a source follower with feedback bias.
39. Draw the ac circuit of the source follower. What are its properties in comparison to common-source circuit?

Problems

1. For the CE amplifier of Fig. 17.45, determine:
   (a) I_B, I_c and r_e (b) Z_i and Z_o (c) A_v and A_i
   Given: $\beta = 100$, neglect $r_{o.}$
2. For the CE amplifier of Fig. 17.46, BJT has $\beta = 110$ and $r_o = \infty$
   (a) Determine r_e, Given $I_E = 7.36$ µA
   (b) Calculate Z_i and Z_o
   (c) Find A_v and A_i
   Hint: R_E is shorted

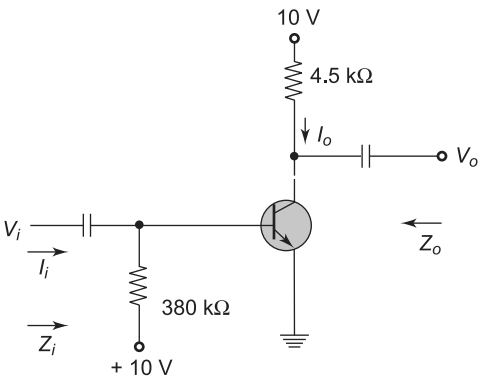


Fig. 17.45

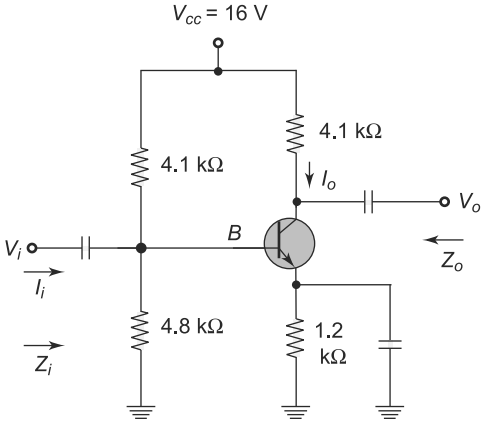


Fig. 17.46

3. For the BJT amplifier circuit of Fig. 17.47,
   (a) Determine the break frequencies in the low-frequency end due to C_{c1}, C_{c2} and C_E-what is the cut-off frequency?
   (b) Calculate the mid-band voltage gain.
   Data: $C_{C1} = 1$ µF $= C_{C2}$, $C_E = 50$ µF, $\beta = 100$

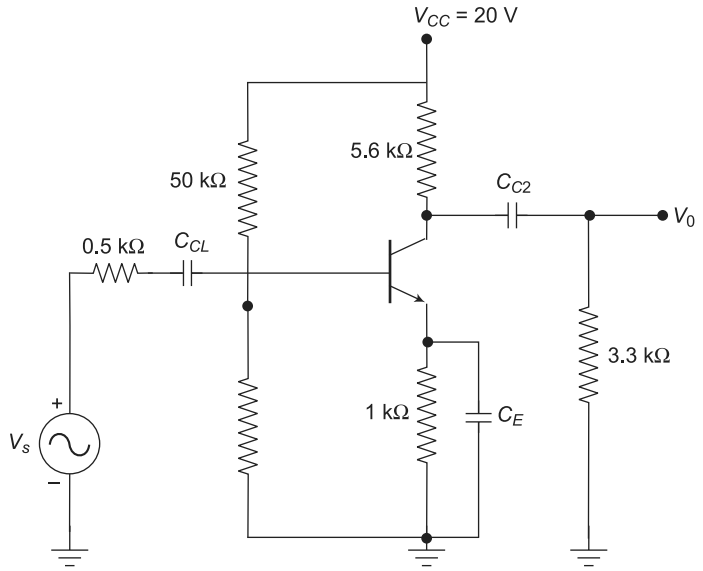


Fig. 17.47

4. For the FET amplifier circuit of Fig. 17.48,
   (a) Find the mid-frequency voltage gain
   (b) Find the lower cut-off frequency
5. Calculate the size of the emitter resistance bypass capacitor to provide a low-frequency 3 dB point of 100 Hz for a CE BJT amplifier.
   Given: $R_E = 1.5$ kΩ, $\beta = 100$, $r_e = 10$ Ω, $R_s = 1$ kΩ, $R_B = \infty$.
6. For the BJT amplifier circuit of Fig. 17.49, determine:
   (a) The lower half-power frequency due to (i) C_{C1} (ii) C_E
   (b) Hence, determine the overall lower cut-off frequency of the amplifier circuit.

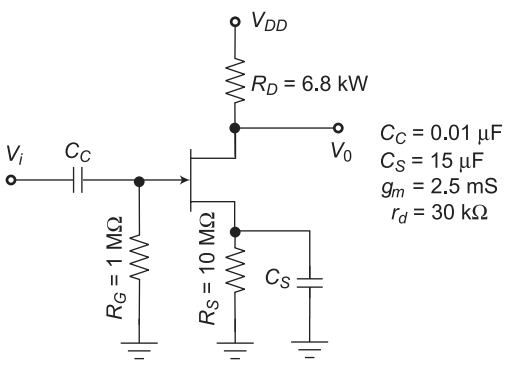


Fig. 17.48

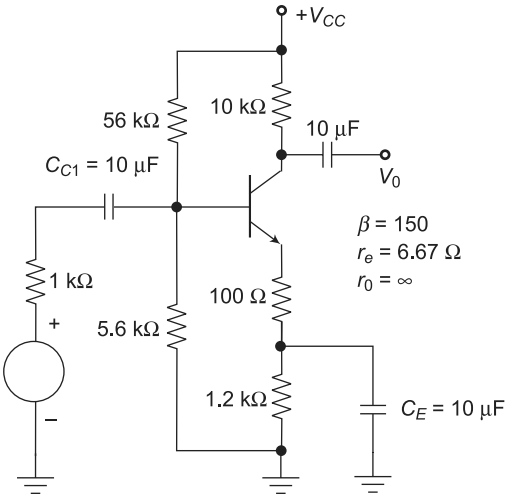


Fig. 17.49

7. For the FET amplifier circuit of Fig. 17.50,
   (a) Determine the lower 3 dB cut-off frequencies due to capacitor C_{C1} and C_S. Then find the effective cut-off frequency.
   (b) Find the mid-frequency gain.

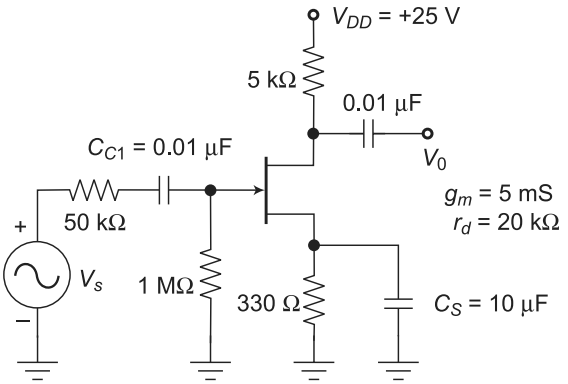


Fig. 17.50

8. The amplifier in Fig. 17.51 is to have a lower cut-off frequency of 20 Hz. Assuming I_C = 1.18 mA and C_E, C_{C2} to be large, drawn an approximate circuit model and specify C_{C1} (β = 100).

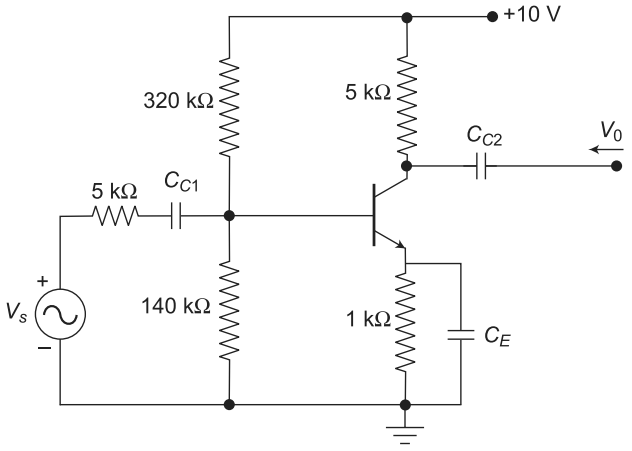


Fig. 17.51

9. For the JFET drain characteristics drawn in Fig. 17.52,
   (a) Find r_d for $V_{GS} = 0$
   (b) Find g_{m0} for V_{DS} = 10 V
10. A JFET has parameters J_{DSS} = 10 mA, V_p = – 6 V. If is biased at $V_{GSQ} = V_p/4$. Determine $g_{m.}$
11. A JFET has r_d = 100 kΩ and its ideal voltage gain is –250. What is the value of g_m?

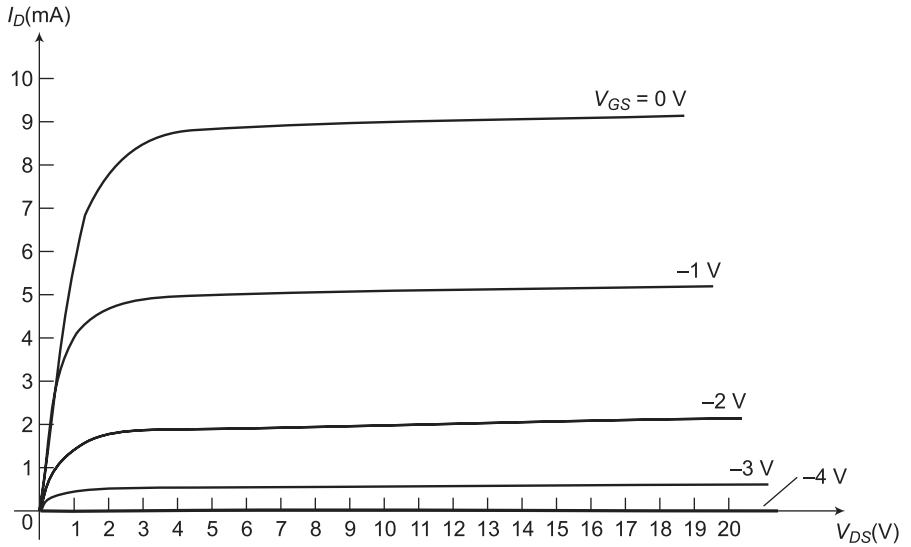


Fig. 17.52

12. A JFET fixed bias amplifier circuit is drawn in Fig. 17.53. JFET data: I_{DSS} = 12 mA, V_p = – 4 V, r_d = 25 kΩ. Determine Z_i, Z_0 and A_v.
13. A JFET amplifier with voltage divider bias is shown in Fig. 17.54 JFET parameters are
    I_{DSS} = 12 mA, V_p = – 4 V, r_d = 100 kΩ
    Determine Z_i, Z_0 and A_v

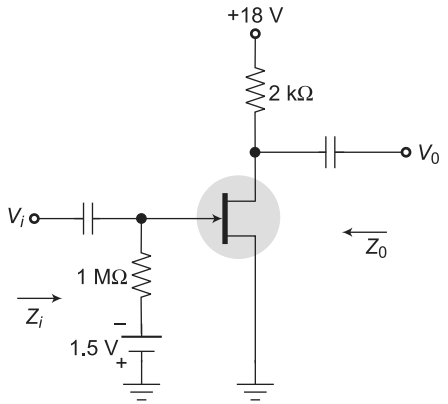


Fig. 17.53

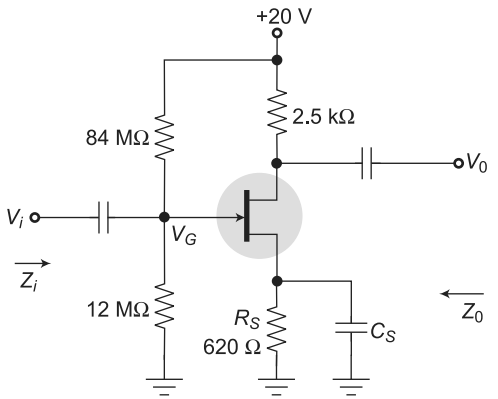


Fig. 17.54

14. The DMOFET amplifier of Fig. 17.55 has g_m = 6 mS, r_d = 30 kΩ. Determine Z_i Z_0 and A_v.
15. For EMOSFET drain feedback bias amplifier determine Z_i, Z_0, A_v
    EMFOST data
    V_T = 3.5 V
    $k = 0.3 \times 10^{-3}$ A/v^3
    r_d = 100 kΩ

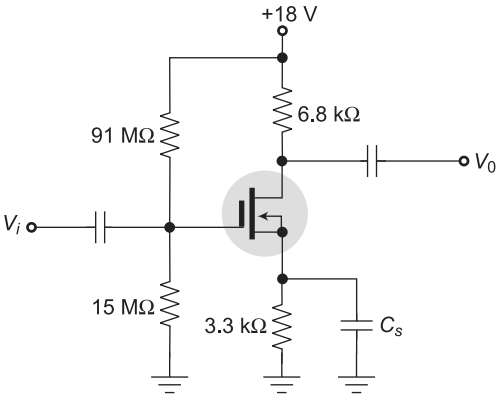


Fig. 17.55

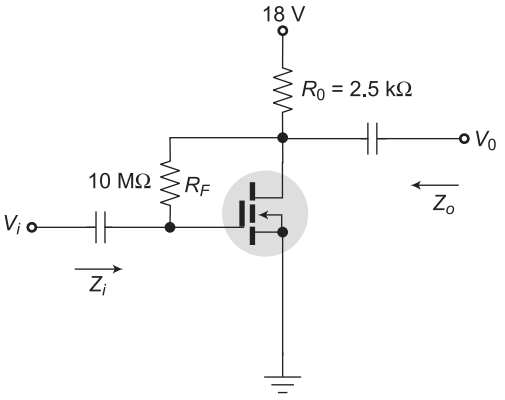


Fig. 17.56

Hint: ac circuit

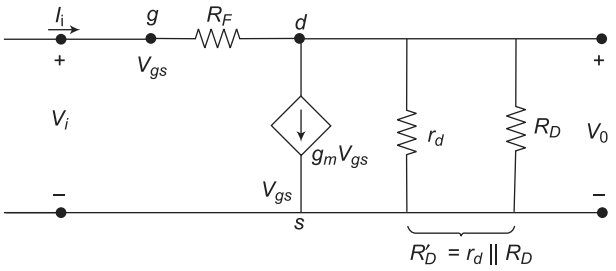


Fig. 17.57

At node *d*

$$I_i = \frac{V_i - V_0}{R_F} = V_i g_m + \frac{V_0}{R_0} \tag{i}$$

$$V_i\left[\frac{1}{R_F} - g_m\right] = V_0\left[\frac{1}{R_F} + \frac{1}{R'_D}\right]$$

$$A_v = \frac{V_0}{V_i} = \frac{\left[\frac{1}{R_F} - g_m\right]}{\left[\frac{1}{R_F} + \frac{1}{R'_g}\right]} \tag{ii}$$

Substituting V_0 from Eq. (ii) in Eq. (i)

$$I_i = V_i\left\{g_m + \frac{1}{R'_D}\frac{\left[\frac{1}{R_F} - g_m\right]}{\left[\frac{1}{R_F} + \frac{1}{R'_D}\right]}\right\}$$

$$Z_i = \frac{V_i}{I_i} = \frac{R_F + R'_D}{1 + g_m R'_D}; \text{ upon simplification}$$

$$Z_0 = R_F \parallel R'_D$$

Multiple-Choice Questions

1. The voltage gain of a common-base amplifier is
   (a) zero (b) unity (c) less than unity (d) greater than unity
2. For a common-base transistor amplifier having input resistance (R_i) and output resistance (R_o), which of following statements holds good?
   (a) R_i is high, R_o is low (b) R_i is low, R_o is high
   (c) R_i and R_o are both medium (d) None of these
3. When an emitter-bypass capacitor in a common-emitter amplifier is removed, its ..... is considerably reduced.
   (a) output load resistance (b) voltage gain
   (c) collector-current (d) emitter current
4. Determine the quiescent levels of I_C and V_{CE} for the network in Fig. 17.58.

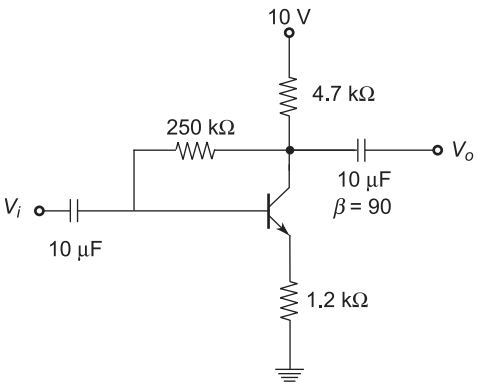


Fig. 17.58

   (a) 1.07 mA, 3.69 V (b) 1.07 A, 3.69V (c) 1 mA, 4.5 V (d) 2 mA, 5 mV
5. The dc load line of a transistor circuit
   (a) is a graph between I_C and I_B (b) is a curved line
   (c) is a graph between I_C and V_{CE} (d) does not contain the locating point
6. When a BJT is employed as an amplifier, it operates
   (a) in saturation (b) in cut-off
   (c) well into saturation (d) over the active region.
7. The negative part of the output signal in a transistor circuit-starts clipping, if Q-point of the circuit moves.
   (a) towards the cut-off point (b) towards the saturation point
   (c) towards the center of the load line (d) none of the above
8. Thermal runaway will take place if the quiescent point is such that
   (a) $V_{CE} > ½ V_{CC}$ (b) $V_{CE} < 2V_{CC}$
   (c) $V_{CE} < ½ V_{CC}$ (d) None of these

Answers

Review Questions

11. $A_I = -58.25$, $R_i = 1.186$ kΩ, $A_v = -58.937$, $R_o = 51.162$ kΩ, –43.78, 3.425 kΩ

Problems

1. (a) 24 μA, 2.4 mA, 10.7 Ω
   (b) $Z_i = 1.067$ kΩ, $Z_o = 4.5$ kΩ
   (c) $A_v = -4.8$, $A_i = -99.74$
2. (a) 0.81 mA, 31.7 Ω
   (b) 1.92 kΩ
   (c) –129, –0.225
3. (a) 77.6 Hz, 17.9 Hz, 112.4 Hz, $f_2 = 112.4$ Hz
   (b) 66.5
4. –13.9, 15.9 Hz
5. 81.45 μF
6. 3.27 Hz, 15.38 Hz, 15.38 Hz
7. (a) $f_{c_{c1}} = 15.16$ Hz, $f_{c_{c2}}$ = does not exist, $f_{c_s} = 97.64$ Hz, $f_L = 97.64$ Hz
8. 1.13 μF
9. (a) ≈ 50 kΩ (b) 7.6 mS
10. 2.5 ms
11. 2.5 ms
12. 1 MΩ, 2 kΩ, –6
13. 10.5 MΩ, 2.43 kΩ, –10.2
14. 12.88 MΩ, 5.54 kΩ, 33.24
15. 1.524 MΩ, 2.44 kΩ, –4.36

Multiple-Choice Questions

1. (d) 2. (b) 3. (b) 4. (a) 5. (c)
6. (d) 7. (b) 8. (c) 9. (d) 10. (a)

9. The stability factor of a BJT circuit is defined as
   (a) $S = \frac{dI_E}{dI_B}$ (b) $S = \frac{dI_C}{dI_B}$ (c) $S = \frac{dI_C}{dI_E}$ (d) $S = \frac{dI_C}{dI_{CO}}$
10. Low-frequency hybrid-TT model of transistor parameter transconductance g_m is
    (a) $g_m = \frac{I_C}{25}$ (b) $g_m = \frac{I_C}{2}$ (c) $g_m = I_C$ (d) $g_m = \frac{I_C}{100}$

Op-Amp

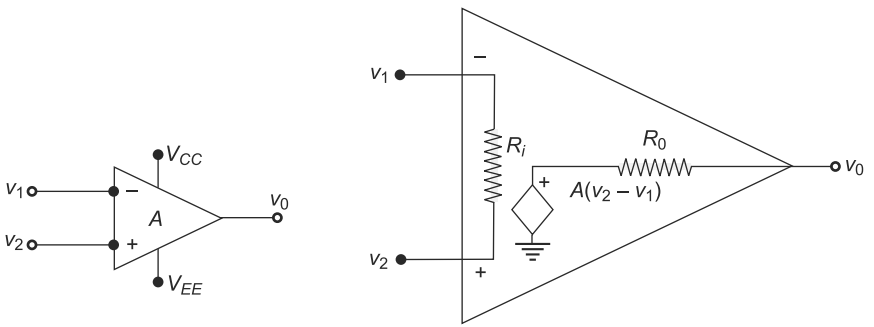
chapter 18

Goals & Objectives

- Introduction of op-amp's and its characteristics
- Block diagram of basic op-amp circuit and its architecture
- Detailed explanation of Schmitt trigger configuration
- Operation of constant-gain multiplier
- Analysis of basic logarithmic amplifier using diode and transistor

18.1 INTRODUCTION

An op-amp is perhaps the most important and versatile analog IC; it is applied in analog signal processing and analog filtering. The symbol of an op-amp is drawn in Fig. 18.1(a). It has two input terminals, inverting (–) and non-inverting (+), and the output is a single terminal. The voltages are measured w.r.t. ground reference, which may not be always shown. The simplified circuit model of an op-amp is drawn in Fig. 18.1(b). It has a gain of A, input resistance R_i and output resistance R_o. An ideal op-amp has $A = \infty$, $R_{\text{in}} = \infty$ and $R_o = 0$.



(a) Symbol, power supply need not be indicated

(b) Circuit model

Fig. 18.1 *op-amp – IC 741*

Infinite gain means

$$v_o = A(v_2 - v_1)$$

or $$v_2 - v_1 = \frac{v_o}{A = \infty} = 0$$

or $$v_2 = v_1$$

It means that inverting and non-inverting terminals are at the same potential.

OP-AMP Architecture

The block diagram of an op-amp is drawn in Fig. 18.2. Various blocks are described under.

Differential Amplifier (DA)

It amplifies the difference of inputs, $v_d = (v_2 - v_1)$, where the differential mode gain is A_d. If the same input $v_c = \frac{v_2 + v_1}{2}$ is applied to both the terminals, the amplification is labelled A_c. As the difference of common-mode signals is zero, A_c should be zero but in a practical differential amplifier, it is a small value.

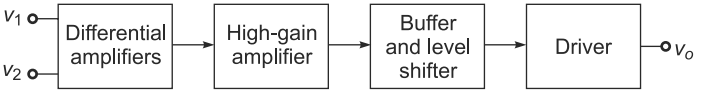


Fig. 18.2 *Block diagram of an operational amplifier*

The ratio of these gains is called

$$\text{Common-Mode Rejection Ratio (CMRR)} = \frac{A_d}{A_c}; \tag{18.1}$$

Being very large it is measured in dB.

We will not deal with the circuit of a DA except to state that it is two BJT [or MOSFET] amplifiers connected in opposition so as to amplify the difference of two input signals.

- It is a high-gain amplifier (direct coupled, highly stabilised).
- The buffer is emitter follower for matching the load. If the output is nonzero for zero input, the level shifts make it zero.
- Driver is power amplifier.

The most popular op-amp and the industry standard is the **IC 741 op-amp**. It is an analog (linear) IC. Its power supply voltages are $+V_{CC}$ and $-V_{EE}$ with $V_{CC} = V_{EE} = 15$ V. The range of output is $-10 \le v_0 \le +10$ V. Further, it is short-circuit protected. Typical parameters for the 741 op-amp are

$A = 200{,}000$ $R_{in} = 2$ MΩ, $R_0 = 75$ Ω

$CMRR = 80$-100 dB 100 dB $\rightarrow 10^5$

The output of the op-amp is

$$v_o = A_d (v_2 - v_1) + A_c \left(\frac{v_2 + v_1}{2} \right)$$

or

$$v_o = A_d V_d + A_c V_c = A_d V_d \left[1 + \frac{1}{CMRR} \cdot \frac{V_c}{V_d} \right] \tag{18.2}$$

As CMRR is very high (10^5),

$$V_o = A_d V_d = A(v_2 - v_1)$$

Thus, the op-amp gain is $A = A_d$; common-mode signal is of no consequence.

Other important parameters of the op-amp are

- **Input offset voltage** Differential voltage (v_{os}) needed to make $v_o = 0$
  Typical value $V_{os} = 1$ mV
- **Bias current** $I_B = \frac{I_{B1} + I_{B2}}{2}$ to make $v_o = 0$, I_{B1} and I_{B2} are base currents of the two transistors
  Typical value is 80 mA.

Frequency Response

Some *RC* couplings are provided in an op-amp circuit so as to reduce the gain at high frequencies. Otherwise, a positive feedback occurs from stray capacitances causing high-frequency oscillations. The op-amp acts like a low-pass filter with a break frequency at $f_h = 10$ Hz. The typical frequency response (Bode plot) is drawn in Fig. 18.3.

From the Bode plot,

$$20 \log \frac{f_T}{f_h} = \text{dB(A)} = 20 \log \text{A},$$

Therefore,

$$\frac{f_T}{f_h} = A$$

or

$$\text{A}f_h = f_T = \text{unity gain (0 dB) frequency} = \text{constant}$$

$$\text{A}f_h = \text{gain-bandwidth product}$$

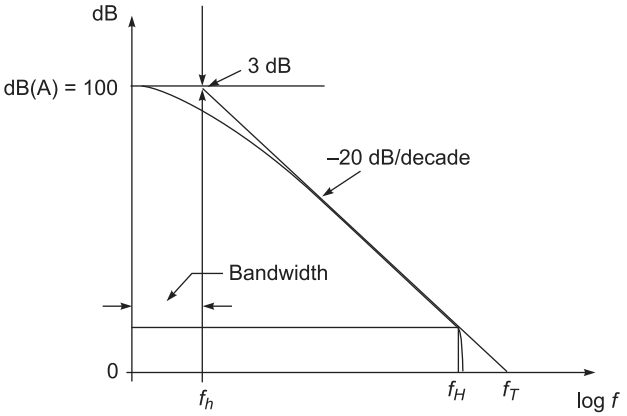


Fig. 18.3 *Op-amp frequency response*

If negative feedback around op-amp it reduces the gain to A_F, then

$$A_F f_H = f_T \tag{18.3a}$$

or

$$f_H = \frac{f_T}{A_F} \gg f_h \tag{18.3b}$$

Due to reduction in gain caused by feedback, the bandwidth increases from f_h to f_H.

Slew Rate

Because of the presence of capacitances, which is *RC* combination, it can charge at a limited rate, and the rate of change of output of the op-amp is limited to

$$\text{Slew rate } S = \left.\frac{dv_o}{dt}\right|_{\max} \tag{18.3c}$$

Its typical value is 0.5 V/μs as shown in Fig. 18.4.

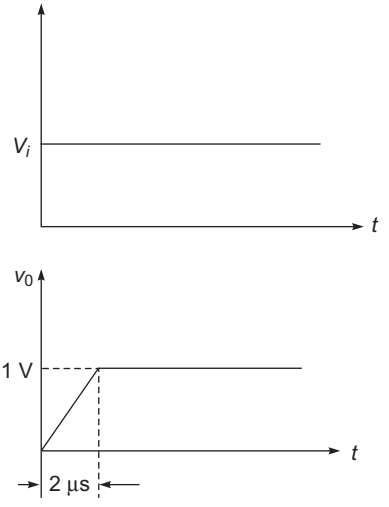


Fig. 18.4 *Illustrating effect of slew rate*

For a sinusoidal signal,

$$V_o = V_m \sin \omega$$

$$S = \left.\frac{d v_o}{dt}\right|_{\max} = V_m \omega$$

or $$S = 2\pi f V_m \tag{18.4}$$

It is a combination of frequency and peak value of output.

18.2 BASIC OP-AMP CIRCUITS

Inverting Amplifier

The op-amp circuit with voltage feedback is shown in Fig. 18.5.

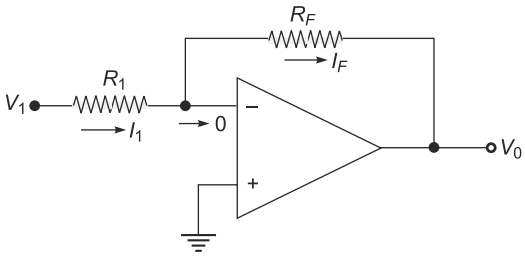


Fig. 18.5 *Investing amplifier*

Virtual Ground

As the (+) terminal is grounded, the (–) terminal is virtually at ground potential.

- Current into op-amp terminal is always zero as $R_{\text{in}} = \infty$

  Therefore,

$$I_F = I_1 \tag{18.5a}$$

$$\frac{0 - V_o}{R_F} = \frac{V_1}{R_1} \tag{18.5b}$$

The gain is

$$\frac{V_o}{V_1} = -\frac{R_F}{R_1} \text{ or } V_0 = -\left(\frac{R_F}{R_1}\right) V_1 \tag{18.6}$$

We find that output voltage is the negative of the input voltage, i.e. it is inverted.

Non-inverting Amplifier (Fig. 18.6)

As the two input terminals of op-amp must be at same potential,

$$V(A) = V_1$$

Applying KCL at A,

$$\frac{V_1}{R_1} + \frac{V_1 - V_0}{R_F} = 0 \tag{18.7a}$$

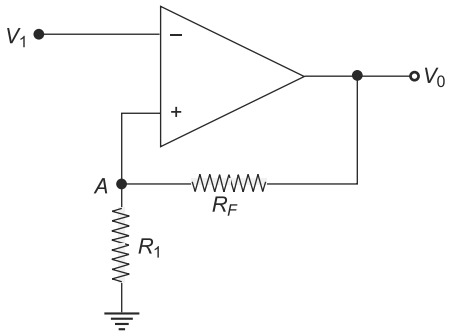


Fig. 18.6 *Non-inverting amplifier*

Reorganising, we get

$$\frac{V_0}{V_1} = 1 + \frac{R_F}{R_1} \text{ or } V_0 = +\left(1 + \frac{R_F}{R_1}\right) V_1 \tag{18.7b}$$

As V_0 has the same sign as V_1, the amplifier is non-inverting.

Note: In analysis of op-amp circuits, we note the following:

- Inverting and non-inverting terminals are at the same potential.
- The current into these terminals is zero.

Transfer Characteristic of OP-AMP

An op-amp is linear with high gain over a very small value of $V_i = \in$ as shown in Fig. 18.7 beyond which it saturates, $V_0 = V_{CC}$.

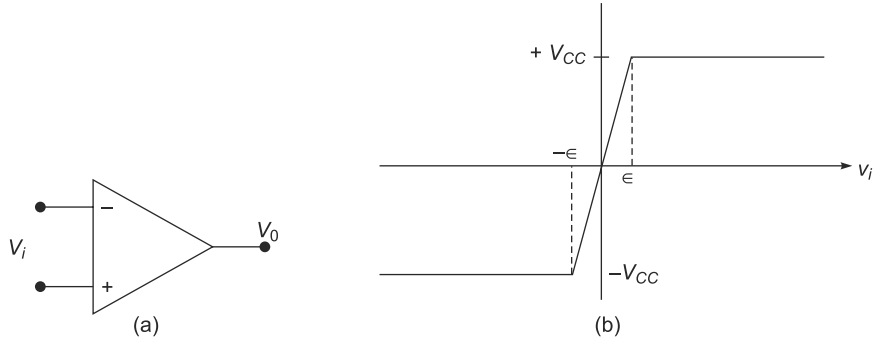


Fig. 18.7 *(a) Open-loop op-amp (b) Transfer characteristic*

Applications of op-amp are linear or nonlinear according to the region of its operation.

Linear Applications of OP-AMP

❑ **Summer Circuit** The op-amp circuit is drawn in Fig. 18.8.

$$I_1 + I_2 + I_3 = I_F \tag{18.8a}$$

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} = -\frac{v_0}{R_F} \tag{18.8b}$$

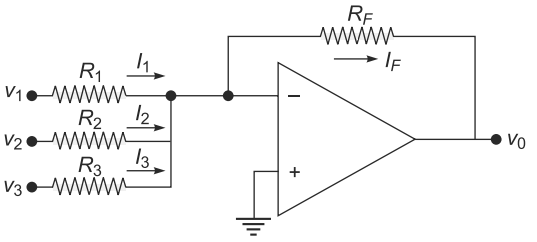


Fig. 18.8 *Summer circuit*

Reorganising,

$$v_0 = -\left\{\left(\frac{R_F}{R_1}\right)v_1 + \left(\frac{R_F}{R_1}\right)v_2 + \left(\frac{R_E}{R_3}\right)v_3\right\} \tag{18.9a}$$

For $R_1 = R_2 \pm R_3 = R_F$

$$v_0 = -(v_1 + v_2 + v_3) \tag{18.9b}$$

$$= -(\text{sum of voltages})$$

❑ **Subtractor** The op-amp circuit is shown in Fig. 18.9.

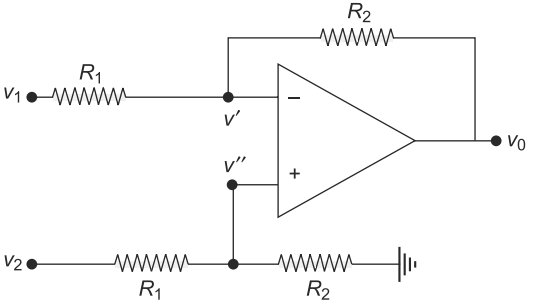


Fig. 18.9 *Subtractor*

$$v' = \left(\frac{R_2}{R_1 + R_2}\right)v_2 \tag{18.10a}$$

$$\frac{v_1 - v'}{R_1} = \frac{v' - v_0}{R_2} \tag{18.10b}$$

or $$\frac{v_0}{R_2} = v'\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{v_1}{R_1} \tag{18.10c}$$

Substituting v' from Eq. (18.10a) in Eq. (18.10c),

$$\frac{v_0}{R_2} = \left[\frac{R_1 + R_2}{R_1 R_2} \cdot \frac{R_2}{R_1 + R_2}\right]v_2 - \frac{v_1}{R_1} = \frac{v_2 - v_1}{R_1}$$

or $$v_0 = \frac{R_2}{R_1}(v_2 - v_1) \text{ or } v_0 = v_2 - v_1 \text{ for } R_1 = R_2 \tag{18.11}$$

Source Converters

❑ **Voltage Follower** Refer op-amp circuit of Fig. 18.10. As terminal voltages must be equal, so

$$v_0 = v_s$$

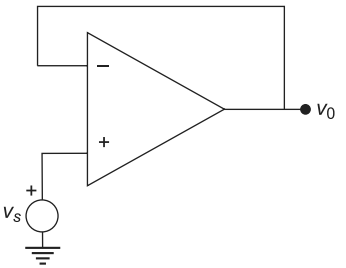


Fig. 18.10 *Op-amp circuit*

❑ **Current-to-voltage Converter** (Transresistance amplifier, Fig. 18.11)

$$V_0 = -R_F I_i$$

The disadvantage is that the bias current I_B gets added to I_i, introducing a small error.

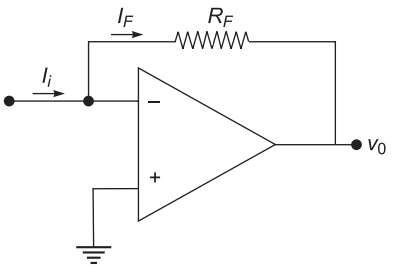


Fig. 18.11 *Transresistance amplifier*

❑ **Voltage-to-current Converter** (Transconductance amplifier)

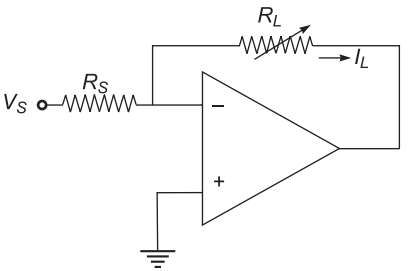


Fig. 18.12 *Voltage-to-current converter*

Op-amp current of Fig. 18.12,

$$I_L = -\left(\frac{V_S}{R_S}\right)$$

For a grounded load, the circuit is drawn in Fig. 18.13.

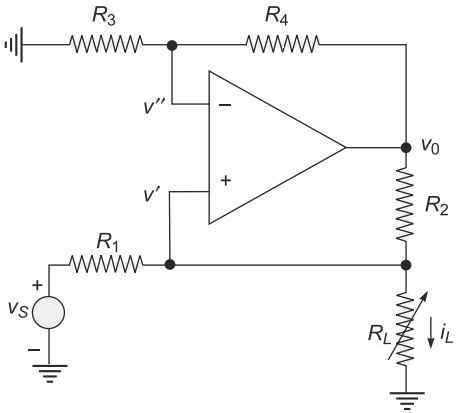


Fig. 18.13 *Circuit for grounded load*

Prove that $i_L = \frac{v_s}{R_1}$

Proof

$$v' = \left(\frac{R_3}{R_3 + R_4}\right) v_0$$

$$\frac{v_s - v'}{R_1} + \frac{v_0 - v'}{R_2} = i_L$$

$$\frac{v_s}{R_1} - \left(\frac{1}{R_1} + \frac{1}{R_2}\right) v' + \frac{v_0}{R_2} = i_L$$

$$\frac{v_s}{R_1} - \left[\left(\frac{R_1 + R_2}{R_1 R_2}\right) \frac{R_3}{R_3 + R_4} - \frac{1}{R_2}\right] v_0 = i_L$$

Hence,

$$\frac{V_S}{R_1} = i_L$$

❑ Constant Voltage Source (Fig. 18.14)

$$\frac{V_S}{R_S} = -\frac{V_0}{R_F}$$

or $$V_0 = -\left(\frac{R_F}{R_S}\right)V_S$$

Independent of load resistance

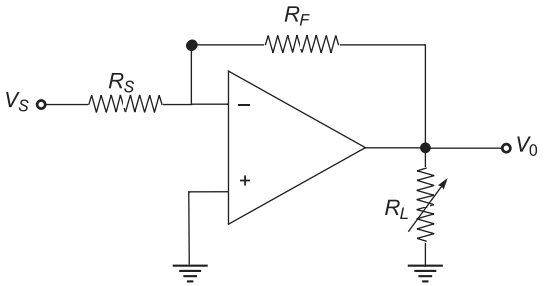


Fig. 18.14 *Constant voltage source*

Integrator

The output is fed back through a capacitor as in Fig. 18.15.

$$i_1 = i_F = \frac{v_1}{R_1}$$

$$v_0 = -\frac{1}{C_F}\int i_F\,dt = -\frac{1}{R_1 C_F}\int v_1\,dt$$

Thus, v_0 is a scaled version of the integral of v_1.

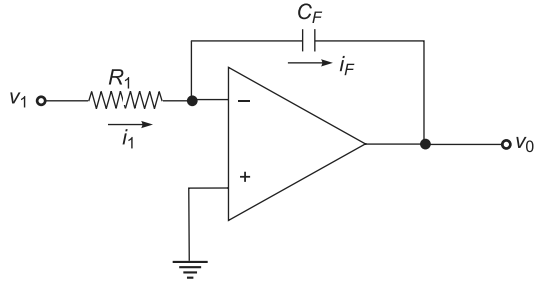


Fig. 18.15 *Integrator*

The dc offset current and input bias current on continuous integration cause the output to reach saturation limit; well before that the integrator must be recycled. We will not discuss this in detail any further.

Differentiator

The input is through capacitance C_1 as shown in Fig. 18.16.

$$i_1 = i_F$$

$$C_1 \frac{dv_1}{dt} = -\frac{v_0}{R_F}$$

$$v_0 = -R_F C_1 \frac{dv}{dt}\text{; scaled differentiation}$$

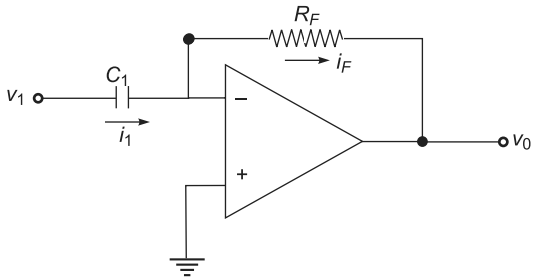


Fig. 18.16 *Differentiator*

Let $v_1 = \sin \omega t$,

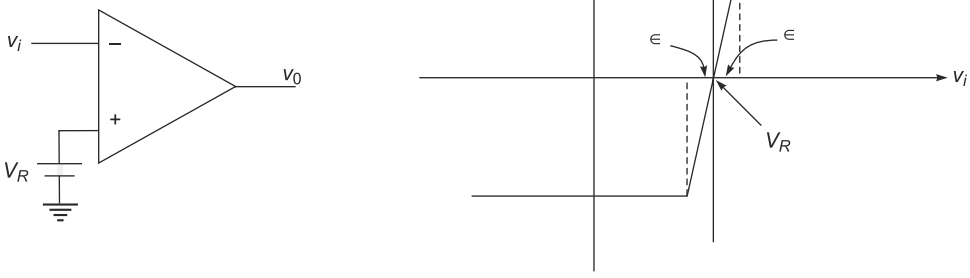
Then

$$v_0 = -(R_F C_1)\, \omega \cos \omega t$$

The output amplitude increases linearly with signal frequency. Therefore, high-frequency noise would get amplified. Differentiation is avoided in op-amp circuits.

❑ **Comparator** The saturation characteristic of an op-amp in open loop (see Fig. 18.17) is made use of in determining if a signal is more or less than a certain value (V_R). The op-amp circuit and the output are shown in Fig. 18.17(a) and (b). If the + terminal is grounded ($V_R = 0$), the circuit becomes zero crossing detector.

If v_i is sinusoidal, the waveform of v_0 (reader to make sketch) will be rectangular, assuming $\in = 0$.



(a) (b) Input-output, $\in$ is μV as gain A is very high

Fig. 18.17 *Comparator*

Example 18.1

For the op-amp circuit of Fig. 18.18, find the output and closed-loop gain.

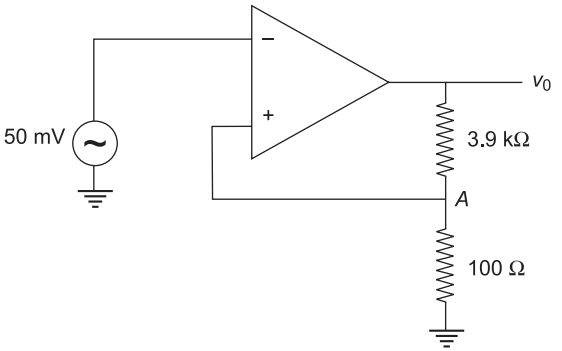


Fig. 18.18

Solution

$$V_A = 50 \text{ mV}$$

$$I(100\ \Omega) = \frac{50}{100} = 0.5 \text{ mA}$$

As no current flows into the + terminal,

$$I(3.9 \text{ k}) = 0.5 \text{ mA}$$

$$V_0 = V_A + 3.9 \times 0.5 \times 10^3 = 50 + 1950$$

$$= 2000 \text{ mV}$$

Gain, $$A_F = \frac{2000}{50} = 40$$

Example 18.2

In Fig. 18.19, R_L is the transducer resistance which can vary from 1 kΩ to 10 kΩ. Determine the range of variation of the output voltage.

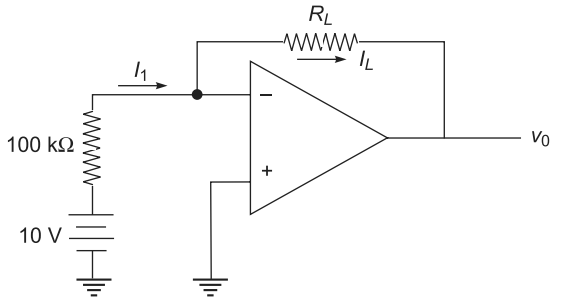


Fig. 18.19

Solution

$$I_1 = I_L$$

$$\frac{10}{100} = -\frac{V_0}{R_L}$$

or $$V_0 = -\frac{R_L}{10}$$

$$\left.\begin{array}{ll} R_L = 1\,\text{k}\Omega & V_0 = -0.1\,\text{V} \\ R_L = 10\,\text{k}\Omega & V_0 = -1\,\text{V} \end{array}\right\} \text{range}$$

Example 18.3

For the op-amp circuit of Fig. 18.20, find V_0.

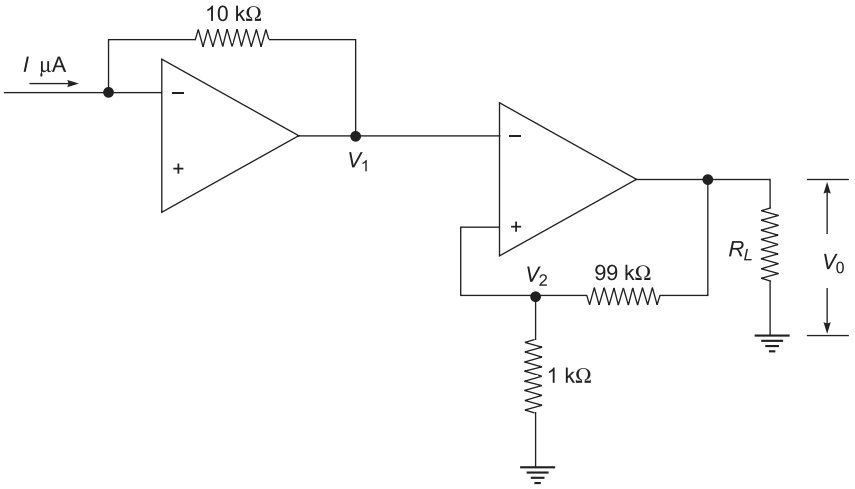


Fig. 18.20

Solution

$$V_1 = -1 \times 10^{-3} \times 10 = -0.1\ \text{V},\ V_2 = V_1$$

Applying KCL at the node (2),

$$\frac{V_1}{1} + \frac{V_1 - V_0}{99} = 0$$

$$V_1\left(\frac{1}{1} + \frac{1}{99}\right) = \frac{V_0}{99}$$

$V_0 = (99 + 1)\ V_1 = 100 \times -0.01 = -1\text{V}$; independent of R_L

Example 18.4

For the op-amp circuit of Fig. 18.21, determine v_p, v_n, v_0, and also power supplied/absorbed by the 4 V source.

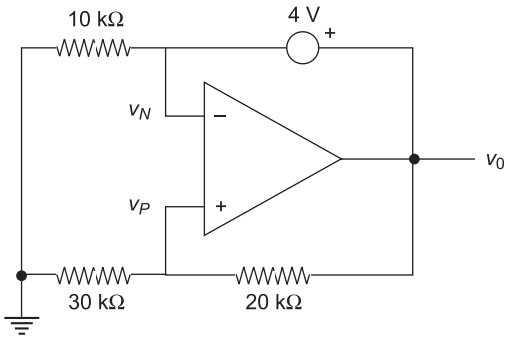


Fig. 18.21

Solution

$$v_p = \left(\frac{30}{30+20}\right) v_0 = 0.6\, v_0$$

$$v_N = v_p = 0.6\, v_0$$

$$v_N + 4 = v_0$$

$$0.6\, v_0 + 4 = v_0$$

or $$v_0 = 10 \text{ V}$$

$$v_p = 6 \text{ V} = v_N$$

$$i\,(10k) = \frac{6}{10} = 0.6 \text{ mA}$$

i(4 V source) = 0.6 mA entering + terminal

Power absorbed, $P = 4 \times 0.6 = 2.4$ mW

Example 18.5

For the op-amp circuit of Fig. 18.22, find v_0 if v_s = 9 V. All reisitances are in kΩ.

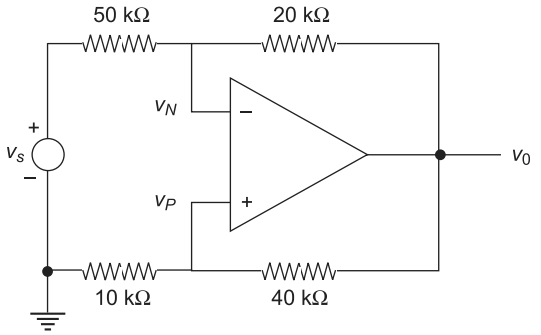


Fig. 18.22

Solution

$$v_p = \left(\frac{10}{10+40}\right) v_0 - 0.2\, v_0$$

$$v_N = 0.2\, v_0$$

Apply KCL at v_N node

$$\frac{v_s - v_N}{50} = \frac{v_N - v_0}{20}$$

$$\frac{9 - 0.2v_0}{50} = \frac{0.2v_0 - v_0}{20}$$

Solving, we get

$$v_0 = -5 \text{ V}$$

Example 18.6

An op-amp has a slew rate of 0.8 v/μs. What is the maximum amplitude of undistorted sine wave that the op-amp can produce at a frequency of 40 kHz? What is the maximum frequency of the sine wave that op-amp can reproduce if the amplitude is 3 V?

Solution $S = 2\pi f V_m$

(a) $0.8 \times 10^6 = 2\pi \times 40 \times 10^3\, V_m$

or $V_m = 3.18$ V

(b) $0.8 \times 10^6 = 2\pi f \times 3$

or $f = 42.44$ kHz

Example 18.7

Figure 18.23 shows the effect of bias current ($I_{B1} = I_{B2} = I_B$) on the output for an inverting op-amp circuit. What value of R_2 will make $V_o = 0$?

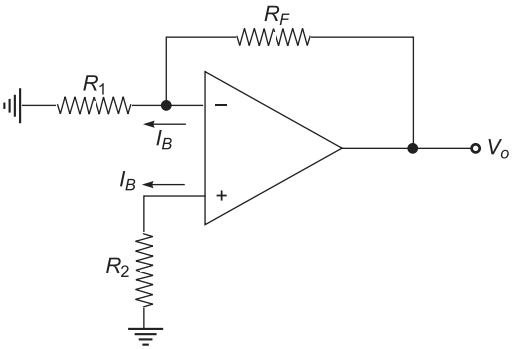


Fig. 18.23

Solution $V_+ = R_2\, I_B$

At the –terminal,

$$I_B = \frac{V_+}{R_1} + \frac{V_+ - V_o}{R_F}$$

For $V_o = 0$

$R_2 = R_1 \parallel R_F$

18.3 SCHMITT TRIGGER

The Schmitt trigger configuration is shown in Fig. 18.24 where the fraction of the output voltage is fed back to the non-inverting terminal of the comparator is

$$\beta = \frac{R_1}{R_1 + R_2}$$

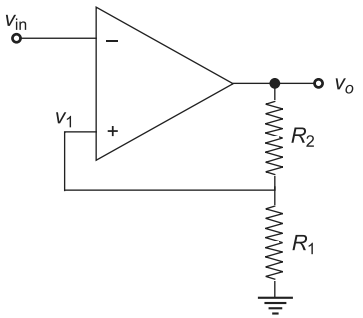


Fig. 18.24 *Schmitt-trigger configuration*

When the comparator output is $v_o = +V_o$,

$$v_1 = +\beta V_o$$

and the triggering (transition of state) will occur at $v_{in} > +\beta V_o$.

When the comparator output is $v_o = -V_o$.

$$v_1 = -\beta V_o$$

and so the state transition will occur for $v_{in} < -\beta V_o$.

The comparator thus has two trip points: the Upper Trip Point ($UTP = +\beta V_0$) and Lower trip Point ($LTP = -\beta V_o$). The operations around UTP and LTP are indicated in Fig. 18.25(a) and 18.25(b) and the overall operation of the trigger is shown in Fig. 18.25(c), which clearly brings into focus the hysteresis phenomenon wherein the hysteresis voltage V_H is given as

$$V_H = \text{UTP} - \text{LTP} = 2\beta V_o.$$

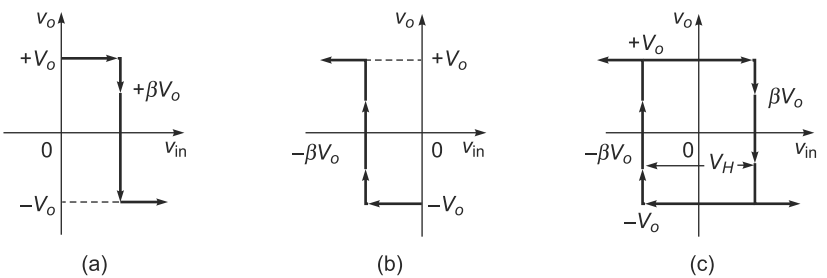
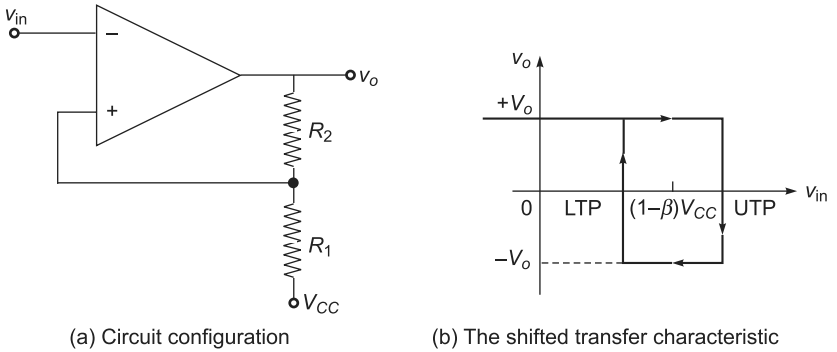


Fig. 18.25 *Transfer characteristics of Schmitt trigger*

When the input signal is above $+\beta V_o$, the output is $+V_o$. Thus, the Schmitt trigger prevents erroneous operation for any noise level less than V_H. Similar noise immunity is present at input signal less than $-\beta V_o$ with output $-V_o$.

The trip voltages can be shifted by modifying the basic circuit of Fig. 18.24 by providing a fixed bias voltage at the lower end of the feedback circuit (resistive voltage divider) as shown in Fig. 18.26(a).



(a) Circuit configuration (b) The shifted transfer characteristic

Fig. 18.26 *Schmitt trigger with fixed bias voltage*

It can be easily shown in this case that

$$\text{UTP} = (1 - \beta)\, V_{CC} + \beta V_o$$

$$\text{LTP} = (1 - \beta) V_{CC} - \beta V_o$$

with hysteresis voltage, V_H remains the same. The shifted transfer characteristic is drawn in Fig. 18.26(b).

One of the most important uses of a Schmitt trigger is to convert a slowly varying voltage signal into a square waveform with sharp edge transitions. This use is illustrated in Fig. 18.27, wherein the input waveform can be arbitrary except that its amplitude is sufficiently large for the signal to go beyond both the hysteresis limits (range V_H). The output in general would be asymmetric.

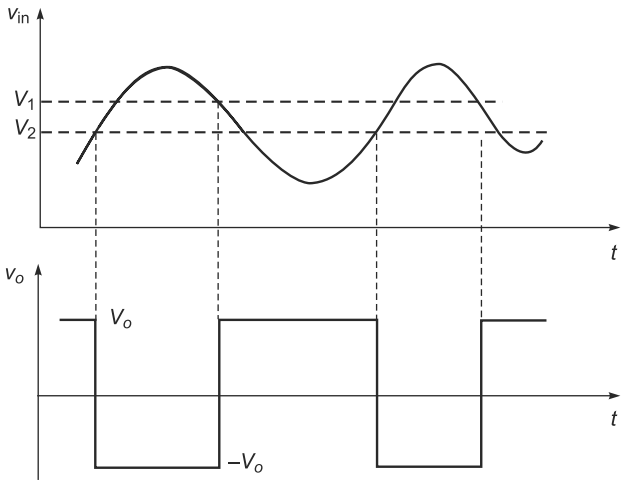


Fig. 18.27 *Input and output waveforms of a Schmitt trigger*

18.4 CONSTANT-GAIN MULTIPLIER

One of the most common op-amp circuits is the inverting constant-gain multiplier, which provides a precise gain or amplification. Figure 18.28 shows a standard circuit connection, with the resulting gain given by.

$$A = \frac{-R_f}{R_1}$$

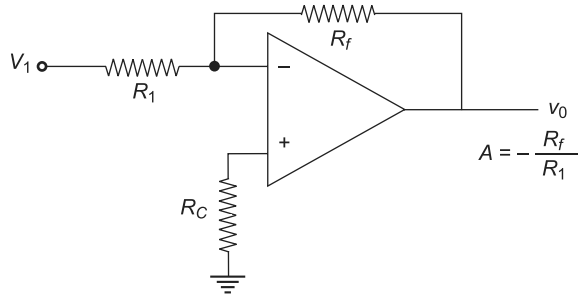


Fig. 18.28 *Constant-gain multiplier*

18.5 BASIC LOGARITHMIC AMPLIFIER

With the background of diode and current equations, let us study the basic logarithmic amplifier circuit using an op-amp. The fundamental log amplifier is formed by placing a diode or a transistor in the negative feedback path of the op-amp.

18.5.1 Basic Log Amplifier using Diode

The circuit diagram of a basic log amplifier using a diode is shown in Fig. 18.29.

The diode D is used in the negative feedback path. The node A is grounded, hence node B is at virtual ground. Hence, $V_B = 0$.

$$\therefore \qquad I = \frac{V_{\text{in}}}{R} \tag{18.12}$$

As the op-amp input current is zero,

$$I = I_f = \text{diode current} \tag{18.13}$$

Now I_f is the current through the diode and voltage across the diode is $V_B - V_o$, i.e. $-V_o$

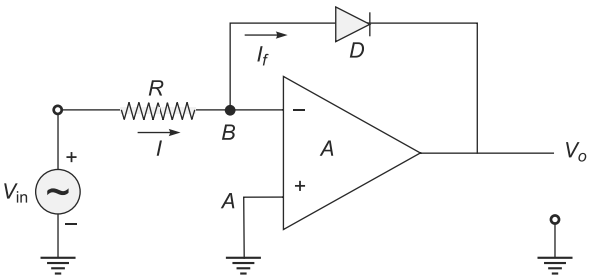


Fig. 18.29 *Basic log amplifier*

From diode equation,

$$I_f = I_0 \left[e^{v/\eta V_T} - 1 \right]$$

we can write the expression for V as,

$$V = \eta V_T \ln \left[\frac{I_f}{I_o} \right]$$

Using this with $V = -V_o$ for the circuit,

$$-V_o = \eta V_T \ln \left[\frac{I_f}{I_o} \right] \tag{18.14}$$

Substituting $I_f = I = \dfrac{V_{\text{in}}}{R}$

$$\therefore \quad V_o = -\eta V_T \ln \left[\frac{V_{\text{in}}}{R I_o} \right] \tag{18.15}$$

As $I_o R$ is constant dc voltage, let us denote it as V_{ref}.

$$\therefore \quad \boxed{V_o = -\eta V_T \ln \left[\frac{V_{\text{in}}}{V_{\text{ref}}} \right]} \tag{18.16}$$

where $V_{\text{ref}} = I_o R$

Thus, the output voltage V_o is a function of logarithm of the input voltage V_{in}. The circuit gives the logarithm to base, i.e. nature logarithm. But the same circuit can be used to find out logarithm values to base 10 by proper scaling as,

$$\log_{10} X = 0.4343 \ln (X) \tag{18.17}$$

18.5.2 Basic Log Amplifier using Transistor

The basic log amplifier can be obtained by using a transistor as a diode in the negative feedback path of an op-amp, as shown in Fig. 18.30.

The node B is at virtual ground, hence $V_B = 0$.

$$\therefore \quad I = \frac{V_{\text{in}} - V_B}{R} = \frac{V_{\text{in}}}{R} \tag{18.18}$$

As the op-amp input current is zero,

$$I = I_C = \text{collector current} \tag{18.19}$$

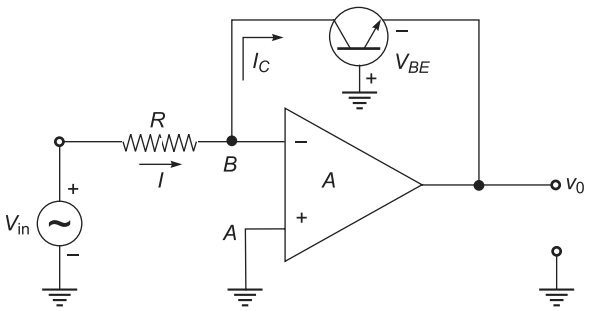


Fig. 18.30 *Basic log amplifier*

The voltage $V_{CB} = 0$ as the collector is at virtual ground and base is grounded. Hence, we can write the equation of I_C as,

$$V_{BE} = V_T \ln \left(\frac{I_C}{I_s} \right) \tag{18.20}$$

Applying to the output side, we get,

$$V_o + V_{BE} = 0 \tag{18.21}$$

$$\therefore \quad V_{BE} = -V_o \tag{18.22}$$

and $$I_C = I = \frac{V_{\text{in}}}{R}$$

Substituting in Eq. (18.20),

$$-V_o = V_T \ln \left(\frac{V_{\text{in}}}{R I_s} \right) \tag{18.23}$$

Let $$V_{\text{ref}} = R I_s,$$

$$\therefore \quad \boxed{V_o = -V_T \ln \left[\frac{V_{\text{in}}}{V_{\text{ref}}} \right]} \tag{18.24}$$

The equation is similar to Eq. (18.16), which gives the output, proportional to the logarithm of the input voltage V_{in}.

Summary

➢ This chapter has described OP-AMP, one of the most important and versatile analog IC, various types of OP-AMPs with their characteristics are discussed.

Exercises

Review Questions

1. Describe an op-amp; and the various stages of an op-amp circuit.
2. Draw a simple current equivalent of op-amp. Derive from this an ideal op-amp. Justify idealisation op-amp in current analysis.
3. What is CMRR? Why does it have a high value?
4. Sketch the frequency response of an op-amp open-loop mode.
5. What is meant by gain-bandwidth product?
6. How does negative feedback around an op-amp affect the bandwidth?
7. What is meant by slew rate of op-amp? How does it affect its performances?
8. What is meant by virtual ground?
9. State some of the applications of op-amp.
10. Sketch the transfer characteristic of op-amp.
11. How is an op-amp used as a comparator? How is it used as a zero crossing detector?

Problems

1. In the op-amp circuit of Fig. 18.31, show that
$$v_0 = (v_1 + v_2) - (v_2 + v_4)$$
If all resistances are equal, is it a subtractor circuit?

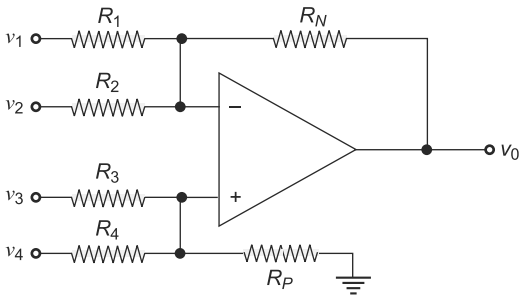


Fig. 18.31

2. For the op-amp circuit of Fig. 18.32, determine V_0.

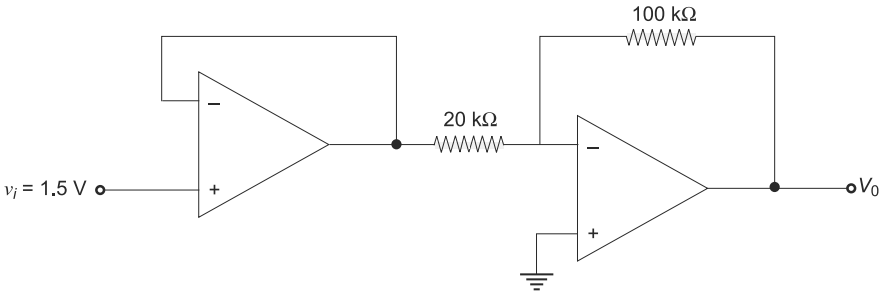


Fig. 18.32

3. For the op-amp circuit of Fig. 18.33, find V_0.

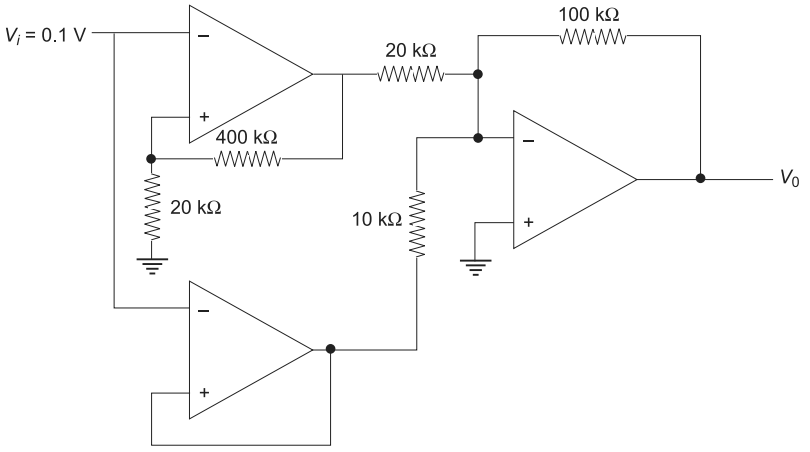


Fig. 18.33

4. In the op-amp circuit of Fig. 18.34, the gain A is finite but $R_{in} = \infty$ and $R_0 = 0$. Calculate the gain.

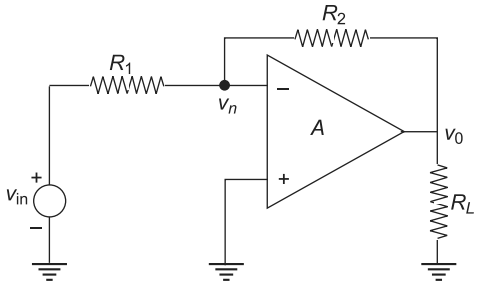


Fig. 18.34

5. In Problem 3, the bandwidth of the op-amp is f_h. Determine the bandwidth of the feedback amplifier.
6. For the op-amp circuit of Fig. 18.35, determine the values V_o.
7. For the op-amp circuit Fig. 18.36, find the value of V_o.

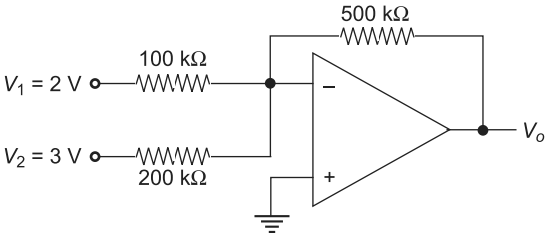


Fig. 18.35

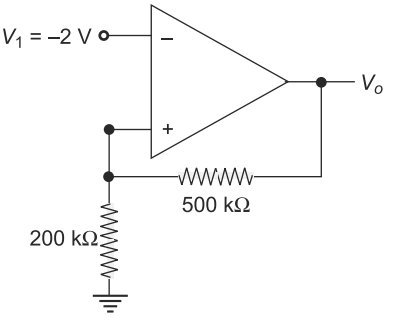


Fig. 18.36

8. For the instrumentation amplifier shown in Fig. 18.37, verify that

$$V_o = \left(1 + \frac{R_2}{R_1} + \frac{2R_2}{R}\right)(V_2 - V_1)$$

Can the gain can be adjusted by varying R?

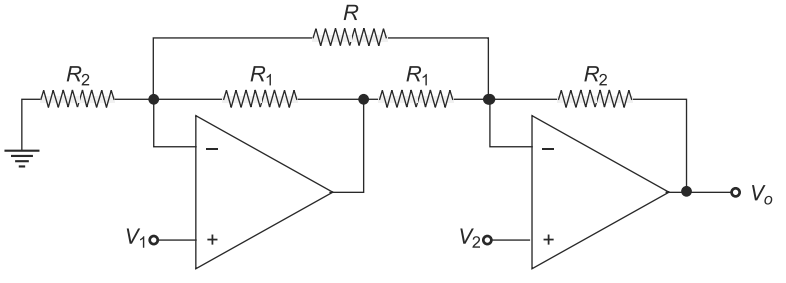


Fig. 18.37

9. For the op-amp circuit of Fig. 18.38, sketch waveforms i_1, i_2, i_3 for the given waveforms of v_1, v_2 and v_3. Hence, sketch the waveform v_o.

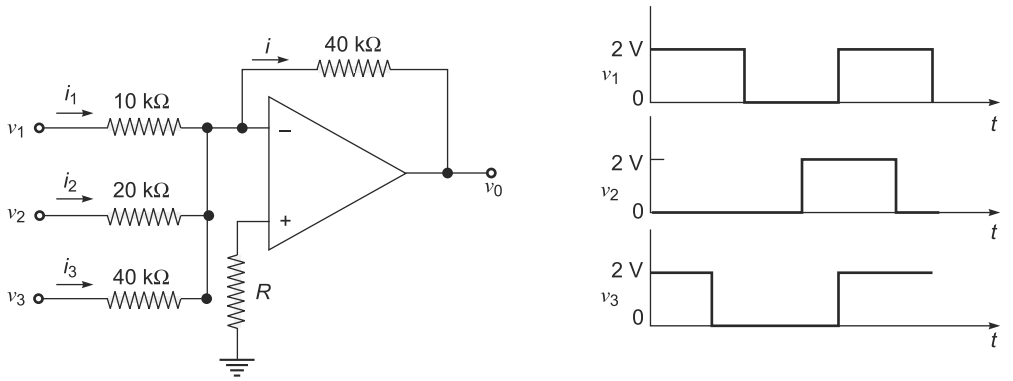


Fig. 18.38

10. For the op-amp circuit of 18.39, find $v_o(t)$. The capacitor initially uncharged.

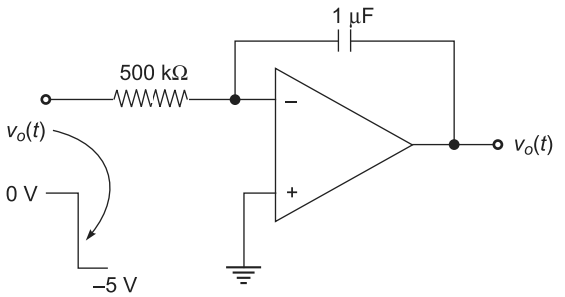


Fig. 18.39

Multiple-Choice Questions

1. An ideal op-amp has
   (a) zero R_o (b) infinite R_i (c) infinite Av (d) all of these
2. An op-amp has
   (a) very small input resistance and very large output resistance
   (b) very small input resistance and very small output resistance
   (c) very large input resistance and very small output resistance
   (d) very large input resistance and very large output resistance
3. The two input terminals of an op-amp are known as
   (a) positive and negative (b) differential and non-differential
   (c) inverting and non-inverting (d) high and low
4. The voltage gain of an open-circuit ideal op-amp is
   (a) infinity (b) around 300 (c) 0 (d) around 10,000
5. The input impedance of an ideal op-amp is
   (a) 0 (b) 10 kΩ (c) infinity (d) none

6. A circuit using an op-amp has
   (a) current-series feedback (b) current-shunt feedback
   (c) voltage-shunt feedback (d) voltage-series feedback

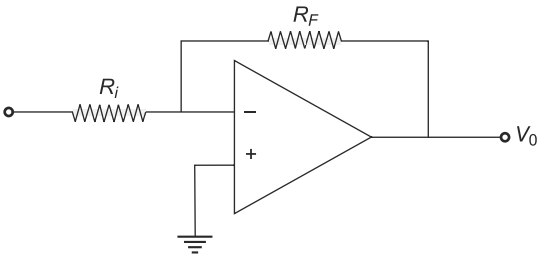


Fig. 18.40

7. An op-amp has a common mode gain of 0.01 and a differential mode gain of 10^5. Its common mode rejection ratio would be
   (a) 10^3 (b) 10^5 (c) 10^7 (d) 10^{-7}
8. A differential amplifier is used in the input stage of all op-amps to provide the op-amp with a very high
   (a) slew rate (b) bandwidth (c) open-loop gain (d) CMRR
9. The input stage of an op-amp is usually a
   (a) level shifter (b) *CE* amplifier
   (c) Class-B push-pull amplifier (d) differential amplifier
10. In a circuit if the open loop gain is 10^6 and output voltage is 10 V, the differential voltage will be
   (a) 10 μV (b) 100 μV (c) 0.1 V (d) 1 μV

Answers

Problems

2. $V_0 = -7.5$
3. $V_0 = 11$ V
4. $A_F = \dfrac{R_2}{R_1 + (R_1 + R_2)\,\Delta}$
5. $\left[(A+1)\dfrac{R_1}{R_2} + 1\right] f_h$
6. 2.5 V
7. -7 V
10. $10t\ u(t)$

Multiple-Choice Questions

1. d 2. c 3. c 4. a 5. c 6. d 7. c 8. c 9. d 10. a

Feedback Amplifiers and Oscillators

chapter 19

Goals & Objectives

- Introduction and discussion about types of feedback-voltage series, voltage shunt, current series and current shunt
- Analysis of gain and bandwidth of feedback amplifier and gain stability with feedback
- Description of oscillators—Wein bridge oscillator, tuned oscillator and crystal oscillator

19.1 INTRODUCTION

In a feedback amplifier, voltage or current output is fed back to the input through a modifying network, which determines the magnitude and phase. The feedback centre opposes the input (*negative feedback*) or aids the input (*positive feedback*). The feedback can change certain important characteristics of the amplifier in a desirable manner.

19.2 TYPES OF FEEDBACK

There are four types of feedback: (1) Voltage series (2) Voltage shunt (3) Current series (4) Current shunt

We will consider *voltage series* feedback whose circuit is drawn in Fig. 19.1. It is also known as series-parallel feedback. Observe that the *feedback is negative*.

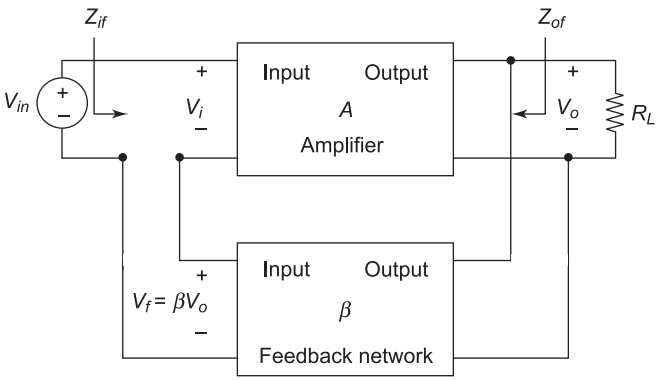


Fig. 19.1 *Voltage-series feedback*

From the figure,

$$V_i = V_{\text{in}} - \beta V_o$$

$$V_o = AV_i = AV_{\text{in}} - A\beta V_o$$

Reorganising, we get gain with feedback as

$$\frac{V_o}{V_{\text{in}}} = A_F = \frac{A}{1 + \beta A} \tag{19.1}$$

This is a general result, which applies to all types of feedback circuits.

The amplifier gain reduces by a factor $(1 + \beta A)$ (19.2)

It can be shown that

Input impedance with feedback, $Z_{if} = Z_i(1 + \beta A)$, increases

Output impedance with feedback, $Z_{of} = Z_o/(1 + \beta A)$, decreases (19.3)

Other types of feedbacks can be analysed on similar lines.

If $\beta A >> 1$ then Eq. (19.1) yields the feedback amplifier gain as

$$A_F = \frac{1}{\beta} \tag{19.4}$$

This means the gain is independent of amplifier gain A. Thus, all the distortions (like amplitude and frequency distortion) do not appear in A_F. This also happens to a noise signal, which gets attenuated by feedback. Any variation in magnitude of A does not appear in A_F, which means A_F has high gain stability. As the cost of these improvements is paid in terms of reduced gain, which can be made up.

Gain and Bandwidth of Feedback Amplifier

As shown above, the negative feedback reduces the amplifier gain. Therefore, as per the general principle, it should increase its bandwidth. In *RC*-coupled amplifiers, the gain reduces at low-frequency and high-frequency ends. So βA_o is no longer much more than unity. As a result, the percent reduction in gain is less at the two frequency ends compared to the mid-band. The reduction in gain and increase in bandwidth of feedback amplifiers are illustrated in Fig. 19.2.

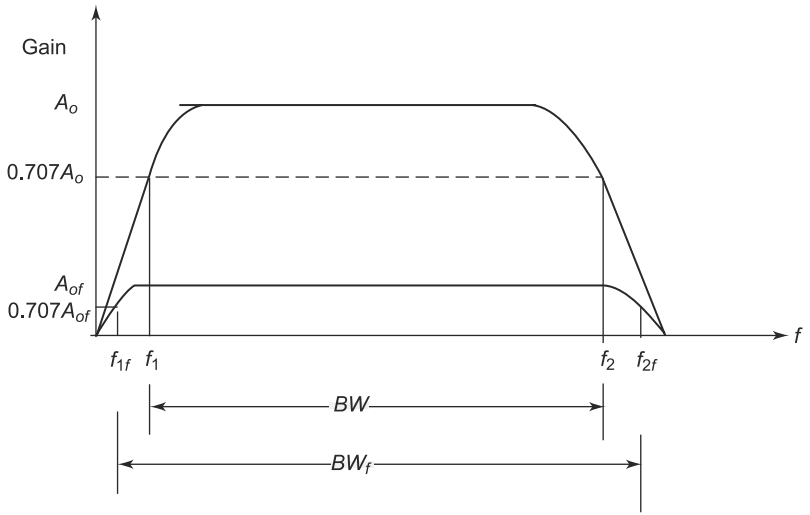


Fig. 19.2 *Effect on A_o and bandwidth of negative feedback*

As $f_1 << f_2$ and $f_{1f} << f_{2f}$, therefore,

$\text{BW} \approx f_2$

$\text{BW}_f \approx f_{2f}$

It can be shown that

$$A_o f_2 = A_{of} f_{2f} = \text{constant product of gain bandwidth} \tag{19.5}$$

Example 19.1

An amplifier has a high-frequency response described as

$$A = \frac{A_o}{1 + (j\omega/\omega_2)}$$

wherein $A_o = 1000$, $\omega_2 = 10^4$ rad/s.

Find the feedback (negative) factor β, which will raise the upper corner frequency (ω_2) to 10^5 rad/s. What is the corresponding overall gain of the amplifier? Find also the gain-bandwidth product in each case.

Solution

$$A_f = \frac{A_o}{1+\{j\omega/[\omega_2(1+\beta A_o)]\}} = \frac{A(\text{new})}{1+[j\omega/\omega_2(\text{new})]}$$

where, $$A(\text{new}) = \frac{A_o}{1+\beta A_o}$$

$$\omega_2(\text{new}) = \omega_2(1+\beta A_o)$$

Substituting values, $10^5 = 10^4(1+\beta \times 1000)$

or $$\beta = 0.009$$

$$A(\text{new}) = \frac{A_o}{1+\beta A_o} = 100$$

Gain-bandwidth products, without and with feedback are

$$\omega_2 A_o = 10^4 \times 10^3 = 10^7$$

$$\omega_2(\text{new})\, A(\text{new}) = 10^5 \times 100 = 10^7$$

Observe that the gain-bandwidth product is maintained constant.

19.3 GAIN STABILITY WITH FEEDBACK

We have seen that the overall gain with negative feedback is

$$A_f = \frac{1}{1+\beta A}$$

Differentiation of the above equation leads to

$$\frac{dA_f}{A_f} = \frac{A_o}{(1+\beta A_o)}\left(\frac{dA}{A}\right) \tag{19.6}$$

$$\frac{dA_f}{A_f} \approx \frac{1}{\beta A}\left(\frac{dA}{A}\right) \approx \text{for } \beta A >> 1 \tag{19.7}$$

This shows that a relative change (dA/A) in the basic amplifier gain is reduced by the factor βA in the relative change (dA_f/A_f) in the overall gain of the feedback amplifier.

Example 19.2

A feedback amplifier comprises two amplifying blocks in tandem; each block having a gain of 100. What should be the gain of the feedback block in order for overall gain to be 100? If the gain of each amplifier block reduces to 50% due to parameter variations, what is the percentage change in the gain of the complete feedback unit?

Solution $A = 100$ (given); forward gain $= A^2 = 10^4$

$$A_f = \frac{10^4}{1+\beta \times 10^4};\ A_f = 100 \text{ (given)}$$

Therefore, $$\beta = 0.0099$$

New value of $A = 50$, $A_f(\text{new}) = \dfrac{(50)^2}{(1 + 0.0099 \times 50^2)} = 97.09$

Reduction in overall gain = 100 – 97.09 = 2.91 or 2.91%

❑ **Observation** It is seen that a 50% reduction in forward gain causes only 2.91% reduction in gain of feedback amplifier. This means that sensitivity of feedback amplifier gain to change in component (forward) gain is quite low. This is one (important) reason for using feedback technique in amplifiers.

We will not pursue the feedback amplifiers any further but go ahead and discover how feedback can use to set up an oscillatory circuit.

Oscillators

Condition for Oscillation

Consider the schematic of the negative feedback amplifier of Fig. 19.3 without any input. As we shall be dealing with sinusoidal quantities voltages, currents would be treated as phasors and gains complex numbers. For the feedback amplifier of Fig. 19.3.

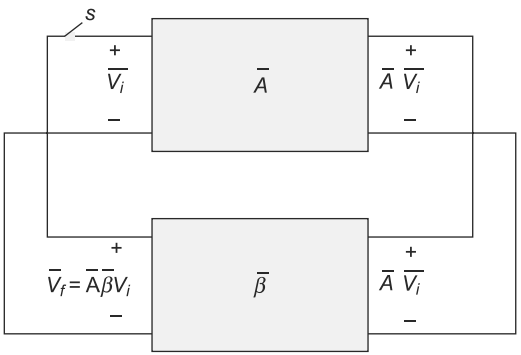


Fig. 19.3 *Pertaining to condition for oscillation*

Amplifier gain, $\dfrac{\bar{V}_o}{\bar{V}_{in}} = \bar{A}_F = \dfrac{\bar{A}}{1 + \bar{\beta}\bar{A}}$

If $\bar{\beta}$ is adjusted such that

$$\bar{\beta}\bar{A} = -1 = 1\angle -180° \tag{19.8}$$

The gain tends to become infinity. For $|\bar{\beta}\bar{A}|$ slightly more than unity, the circuit becomes self-oscillatory with no input $V_{\text{in}} = 0$.

The condition

$$\bar{\beta}\bar{A} = -1 \tag{19.9}$$

is known as Barkhausen condition for oscillation.

Let us consider the amplifier with no input shown in Fig. 19.3. If $\angle\bar{\beta}\bar{A} = -180°$, the polarity of $\bar{V}_f$ reverses and the feedback becomes positive. As the switch *S* is closed, a small voltage (may be due to noise) will begin to build up. The oscillation increases in amplitude till steady conditions are reached with non-sinusoidal oscillations due to saturation as shown in Fig. 19.4.

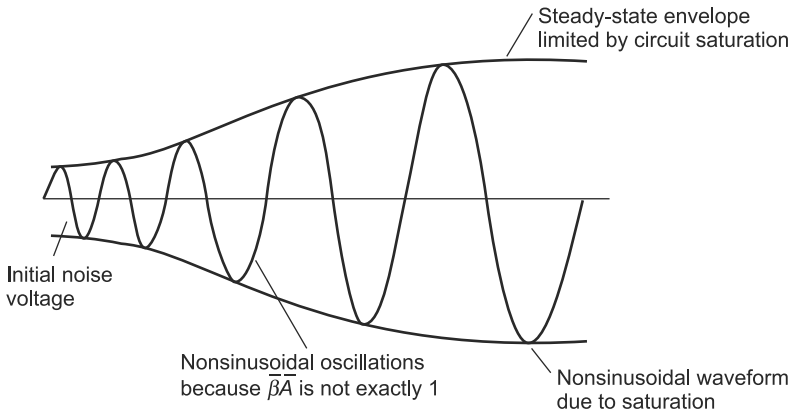


Fig. 19.4 *Oscillation build-up with phase reversal of feedback voltage*

In practical oscillator circuits, the amplifier gain will be a negative constant at oscillation frequency. For oscillations to occur, $\angle\bar{\beta} = -180°$ and $|A\bar{\beta}| > 1$. We will now study various types of oscillators depending upon the circuits to achieve $\angle\bar{\beta} = -180°$. For an amplifier, we shall use op-amp in inverting mode. For BJT based oscillators, the gain can be formed by the method studied in amplifiers.

Phase-shift Oscillator

The phase shift is achieved by *RC*-network. Because of loading effect, three *RC*-stages are needed as shown in Fig. 19.5. By writing three nodal equations in phasor form, we can express

$$\bar{\beta} = \frac{\bar{V}_1(j\omega)}{\bar{V}_0(j\omega)}$$

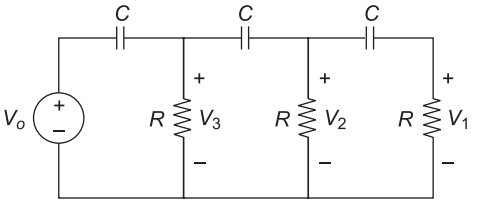


Fig. 19.5 *RC phase shifting network*

By equating the *j*-part of it, in the denominator, we find the frequency at which β is negative (180° phase shifts). The results we get are,

Frequency of oscillation

$$\omega_o = \frac{1}{RC\sqrt{6}} \tag{19.10}$$

And $$\beta(\omega_o) = -\frac{1}{29}\text{ ; 180° phase shift} \tag{19.11}$$

For oscillations to occur,

$$A\bar{\beta} > 1 \text{ or } A > \frac{1}{29} \tag{19.12}$$

The phase-shift oscillator with op-amp is drawn in Fig. 19.6 wherein

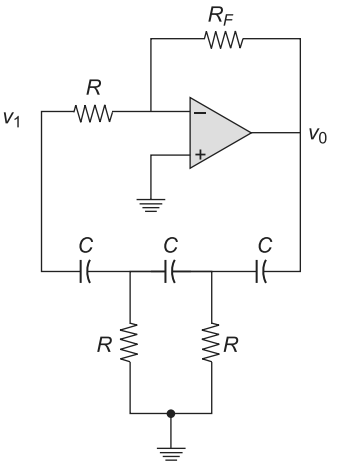


Fig. 19.6 *Phase-shift oscillator*

Frequency of oscillation, $\omega_o = \dfrac{1}{RC\sqrt{6}}$ (19.13)

$$A = -\frac{R_F}{R}$$

$$A\bar{\beta} = -\frac{1}{29}\left(-\frac{R_F}{R}\right)$$

$$= \frac{R_F}{29R} > 1; \text{ by about } 5\%$$

$$R_F > 29R \tag{19.14}$$

Example 19.3

For the feedback op-amp circuit of Fig. 19.7, determine the condition for oscillation and the oscillation frequency.

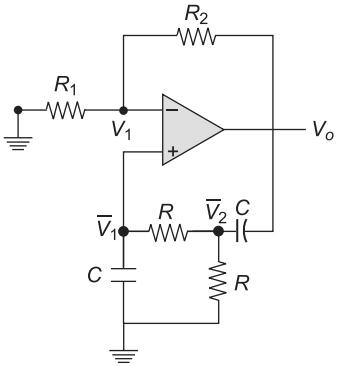


Fig. 19.7

Solution

At the node 2,

$$j\omega C\,(\bar{V}_2 - \bar{V}_o) + \frac{\bar{V}_2}{R} + \frac{\bar{V}_2 - \bar{V}_1}{R} = 0 \tag{i}$$

At the node 1,

$$\frac{\bar{V}_1 - \bar{V}_2}{R} + j\omega C\bar{V}_1 = 0 \tag{ii}$$

or

$$V_2 = (1 + j\omega RC)V_1 \tag{iii}$$

Substituting in Eq. (i) and rearranging, we get

$$\beta = \frac{\bar{V}_1}{\bar{V}_o} = \frac{1}{3 + j(\omega RC - 1/\omega RC)}$$

For β to be real, the j-term should be zero. This happens when

$$\omega_o = \frac{1}{RC} \text{ or } f_o = \frac{1}{2\pi RC} \quad \text{(iv)}$$

Then

$$\beta = +\frac{1}{3} \text{ positive feedback}$$

Forward gain

$$A = \frac{\bar{V}_o}{\bar{V}_1} = \left(1 + \frac{R_2}{R_1}\right) \quad \text{(v)}$$

For oscillations to occur,

$$A\beta = \frac{1}{3}\left(1 + \frac{R_2}{R_1}\right) > 1$$

$$\frac{R_2}{R_1} > 2$$

19.4 OTHER OSCILLATOR CIRCUITS

The details of these circuits is beyond the scope of this book. However, these are listed below:

1. Wein–Bridge Oscillator
2. Tuned Oscillator
   (a) Colpitts: 2C and one L
   (b) Hartely: 2L and one C
3. Crystal Oscillator: precise oscillation frequency same as of the crystal

Summary

➢ Various types of feedback amplifiers and oscillators have been introduced. Gain and bandwidth analysis has been presented.

Exercises

Review Questions

1. State the Barkhhausen criterion, that is, the conditions necessary for sinusoidal oscillations to be sustained.
2. In feedback amplifiers, the gain-bandwidth product remains constant. Comment on this statement.
3. Sketch the phase-shift oscillator using (a) an op-amp, and (b) a JFET.
4. By what factor does the feedback reduce the gain of an amplifier?
5. How does negative feedback stabilise the gain of an amplifier?
6. How does negative feedback affect the bandwidth of the amplifier?

Problems

1. A FET oscillator uses the phase-shifting network as shown in Fig. 19.8
   (a) What is the frequency of oscillation?
   (b) What is the minimum gain necessary for oscillation?

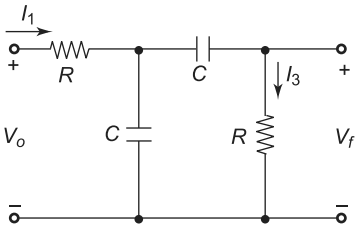


Fig. 19.8

2. An FET phase-shift oscillator has $g_m = 6000$ μs, $r_d = 36$ kΩ, feedback resistance $R = 6$ kΩ. Calculate C for oscillation frequency of 3 kHz.
3. A BJT phase-shift oscillator has the following data: $R = 6$ kΩ, $C = 1600$ pF, $R_C = 20$ kΩ. Calculate the oscillation frequency. What should be the current gain of the BJT?
4. For the lag-lead network of Fig. 19.9, determine $\frac{\overline{V}_o}{\overline{V}_i}$.

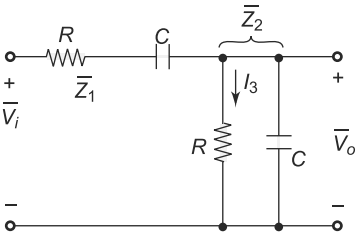


Fig. 19.9

Multiple-Choice Questions

1. In a current-series feedback amplifier, the output resistance
   (a) decreases (b) increases (c) remains same (d) none of these
2. The only drawback of using negative feedback in amplifier is that it involves
   (a) gain stability (b) frequency stability
   (c) temperature sensitivity (d) gain sacrifice
3. An amplifier with no feedback has a gain-bandwidth product of 4 MHz. Its closed-loop gain is 40. The new bandwidth is
   (a) 20 kHz (b) 160 MHz (c) 10 MHz (d) 100 kHz
4. Negative feedback in an amplifier
   (a) lowers its lower 3 dB frequency (b) raises its upper 3 dB frequency
   (c) increases its bandwidth (d) all of these
5. For sustaining oscillations in an oscillator
   (a) feedback factor should be unity (b) phase shift should be unity
   (c) feedback should be negative (d) both (a) and (b)

6. A Hartley oscillator uses
   (a) inductive feedback (b) opacitive feedback (c) resistive feedback (d) none of these
7. A Colpitts oscillator uses
   (a) tapped coil (b) inductive feedback (c) tapped capacitance (d) no tuned *LC* circuit
8. The primary advantage of a crystal oscillator is that
   (a) it operates on a very low dc supply voltage
   (b) its frequency of oscillation remains constant
   (c) it gives a high output voltage
   (d) it can oscillate at any frequency
9. In *RC* phase shift oscillator circuits,
   (a) feedback factor is less then unity
   (b) there is no need for feedback
   (c) pure sine-wave output is possible
   (d) transistor parameters determine oscillation frequency
10. The Barkhausen criterion for sustained oscillation is given by
   (a) $AB = 1$ (b) $|AB| \geq 1$ (c) $|AB| \leq 1$ (d) $AB = 180°$

Answers

Problems

1. (a) $1/2\pi RC$, $A(\text{min}) = 3$
2. 433 μF
3. 5.4 kHz, more than 45
4. $\dfrac{j\omega RC}{1 - \omega^2 RC \rightarrow 3j\omega RC}$

Multiple-Choice Questions

1. b 2. d 3. d 4. d 5. d 6. a 7. c 8. b 9. c 10. a

Regulated Power Supplies

chapter 20

Goals & Objectives

- Block diagram and explanation of regulated power supplies
- Types of regulators—series voltage, shunt voltage and monolithic linear regulators

20.1 INTRODUCTION

In Chapter 15, we have studied diode full-wave rectifiers with output filter to reduce the ripple. In spite of that, the voltage regulation is unacceptable as dc power supply for electronic circuits, in particular electronic gates, draws peak current. Therefore, special voltage regulators are needed at the output of the power supply. There are two types of regulators–discrete transistor type and IC type.

20.2 SERIES VOLTAGE REGULATOR

The regulator is placed in between (series) the supply and load. The regulator block diagram is drawn in Fig. 20.1.

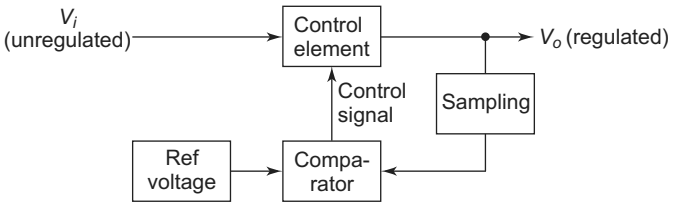


Fig. 20.1 *Regulator block diagram*

Series Regulator Circuits

Single Transistor

The circuit is drawn in Fig. 20.2. As V_1 varies, V_2 remains constant as by design

$$V_i \text{ (min)} > V_z$$

$$V_o = V_z - V_{BE} \tag{20.1}$$

As V_o changes, V_{BE} changes slightly, but there is a large change in $I_E = I_L$ restricting the change in V_o.

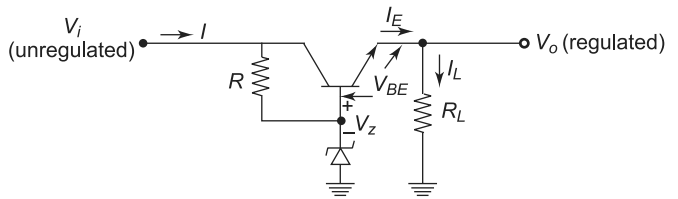


Fig. 20.2 *Linear regulator*

The operation is in linear range and so it is called *linear regulator*. The efficiency of this regulator is high, 50–70%, and it is used for 10 W load.

$I_E = I_1$ is called *pass-current*.

Protection

The circuitry is suitably modified with additional components for limiting the current, thereby providing short-circuit protection. One of these techniques is 'foldback' current limiting.

20.3 SHUNT VOLTAGE REGULATOR

The schematic block diagram of the shunt regulator is drawn in Fig. 20.3.

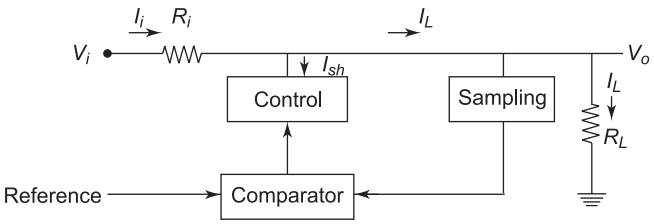


Fig. 20.3 *Shunt regulator, block diagram*

If V_o is high, the control action is to draw shunt current I_{sh} from the input current. $I_L = I_i - I_{sh}$, reduces causing V_o to maintain the desired value. If V_o is low, I_{sh} is added to I_i, and the reverse action takes place.

20.3.1 Shunt Regulator Circuit (Fig. 20.4)

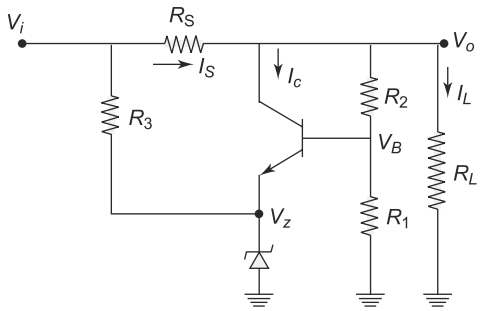


Fig. 20.4 *Shunt regulator*

The potential divider (R_1, R_2) has high resistance and so the current drawn by it can be ignored. The collector current is the shunt current, which controls the load current.

$$I_L = I_S - I_C$$

to regulate V_o

$$V_B = \frac{R_1}{R_1 + R_2} V_o \tag{20.2}$$

Also, $$V_B = V_z + V_{BE}$$

Thus, $$V_o = 1 + \frac{R_2}{R_1}(V_z + V_{BE}) \tag{20.3}$$

which is higher than $V_z - V_o$, and is well regulated except for small variations in V_{BE}.

20.3.2 OP-AMP Shunt Regulator

This circuit is drawn in Fig. 20.5. Because of the feedback gain of op-amp, there is better control over I_c and therefore over V_o.

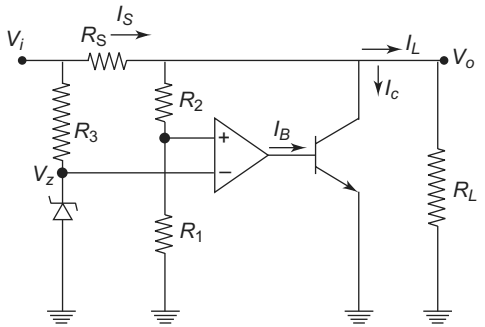


Fig. 20.5 *Op-amp shunt regulator*

$$V_o = \left(\frac{R_1}{R_1 + R_2}\right) V_z$$

or
$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_z \tag{20.4}$$

V_o is higher than V_z.

It is to be observed that V_o in Eq. (20.4) compared to Eq. (20.3) is independent of V_{BE} and so unaffected by its variations.

Short-Circuit Protection

The shunt regulators are protected against short circuit as such. If output is shorted in Figs. 20.4 and 20.5, no component will be affected. The input current increases to

$$I_s(\text{sc}) = \frac{V_i}{R_s}$$

❑ **Remark** Series regulators have better efficiency than shunt regulators, so these are preferred.

Example 20.1

Calculate the approximate output voltage of Fig. 20.6. What is the power dissipation of the pass transistor (Q_2)?

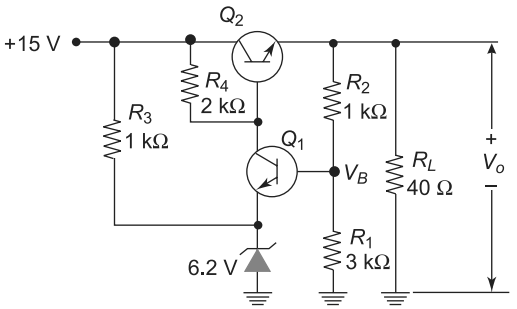


Fig. 20.6

Solution

$$V_B = 6.2 + 0.7 = 6.9 \text{ V}$$

$$V_o = 6.9 \left(\frac{1+3}{3} \right) = 9.2 \text{ V}$$

Pass-transistor dissipation

$$P_D = V_{CE} I_C$$

$$I_C \approx \frac{V_o}{R_L} = \frac{9.2}{40} = 230 \text{ mA}$$

$$V_{CE} = 15.0 - 9.2 = 5.8 \text{ V}$$

$$P_D = 5.8 \times 230 = 1.334 \text{ mW or } 1.334 \text{ W}$$

Reader: What is the approximation in V_o as calculated?

Example 20.2

Calculate the approximate efficiency of the regulator of Fig. 20.6.

Solution

$$P_{\text{out}} = 9.2 \times 230 = 2.12 \text{ W}$$

Current drawn by R_3

$$I(R_3) = \frac{15 - 6.2}{1} = 8.8 \text{ mA}$$

$$I_{\text{in}} = I_c + I(R_3) = 230 + 8.8 = 239 \text{ mA}$$

$$P_{\text{in}} = 15 \times 239 = 3.585 \text{ W}$$

$$\eta = \frac{2.12}{3.585} \times 100 = 59.1\%$$

Example 20.3

Explain the operation of the two-transistor regulator of Fig. 20.7. What is the expression for V_o?

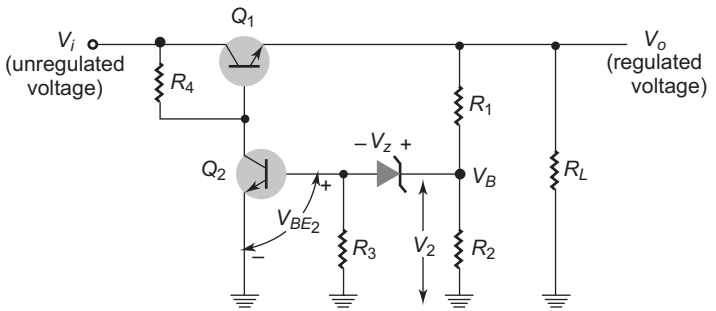


Fig. 20.7

Solution If V_o goes up, V_p increases.

$$V_B = V_z + V_{BE2},\ V_z = \text{constant}$$

As BE_2 increases, the collector current of Q_2 increases and the base current of Q_1 reduces, decreasing the pass current. So V_o returns to regulated value.

$$V_o = V_B\left(\frac{R_1 + R_2}{R_2}\right) = \left(1 + \frac{R_1}{R_2}\right)(V_z + V_{BE_2})$$

Changes in BE_2 are of negligible order.

20.4 MONOLITHIC LINEAR REGULATORS

There is a wide variety of linear **IC voltage regulators** with pin counts from 3 to 14. All are series regulators because they are more efficient than the shunt regulator. Some IC regulators are used in special applications in which external resistors can set the current, limiting the output voltage, and so on. By far, the most widely used IC regulators are those with only three pins: one for the unregulated input voltage, one for the regulated output voltage, and one for ground.

Available in plastic or metal packages, the three-terminal regulators have become extremely popular because they are inexpensive and easy to use. Aside from two optional bypass capacitors, three-terminal IC voltage regulators require no external components.

20.4.1 Basic Types of IC Regulators

Most IC voltage regulators have one of these types of output voltage: fixed positive, fixed negative, or adjustable. IC regulators with fixed positive or negative outputs are factory-trimmed to get different fixed voltages with magnitudes from about 5 to 24 V. IC regulators with an adjustable output can vary the regulated output voltage from less than 2 to more than 40 V.

IC regulators are also classified as standard, low power and low drop-out. *Standard IC regulators* are designed for straightforward and non-critical applications. With heat sinks, a standard IC regulator can have a load current of more than 1 A.

If load currents up to 100 mA are adequate, *low-power IC regulators* are available in TO-92 packages, the same size used for small-signal transistors like the 2N3904. Since these regulators do not require heat sinking, they are convenient and easy to use.

The **drop-out voltage** of an IC regulator is defined as the minimum headroom voltage needed for regulation. For instance, standard IC regulators have a drop-out voltage of 2 to 3 V. This means that the input voltage has to be at least 2 to 3 V, which is greater than the regulated output voltage, for the chip to regulate to specifications. In applications in which 2 to 3 V of headroom is not available, *low drop-out IC regulators* can be used. These regulators have typical drop-out voltages of 0.15 V for a load current of 100 mA and 0.7 V for a load current of 1 A.

20.4.2 On-Card Regulation versus Single-Point Regulation

With *single-point regulation*, we need to build a power supply with a large voltage regulator and then distribute the regulated voltage to all the different *cards* (printed-circuit boards) in the system. This creates problems. To begin with, the single regulator has to provide a large load current equal to the sum of all the card currents. Second, noise or other **ElectroMagnetic Interference (EMI)** can be induced on the connecting wires between the regulated power supply and the cards.

Because IC regulators are inexpensive, electronic systems that have many cards often use *on-card regulation*. This means that each card has its own three-terminal regulator to supply the voltage used by the components on that card. By using on-card regulation, we can deliver an unregulated voltage from a power supply to each card and have a local IC regulator take care of regulating the voltage for its card. This eliminates the problems of the large load current and noise pick-up associated with single-point regulation.

20.4.3 Load and Line Regulation Redefined

Up to now, we have used the original definitions for load and line regulation. Manufacturers of fixed IC regulators prefer to specify the change in load voltage for a range of load and line conditions. Here are definitions for load and line regulation used on the data sheets of fixed regulators:

Load regulation = ΔV_{out} for a range of load current

Line regulation = ΔV_{out} for a range of input voltage

For instance, the LM7815 is an IC regulator that produces a fixed positive output voltage of 15 V. The data sheet lists the typical load and line regulation as follows:

Load regulation = 12 mV for I_L = 5 mA to 1.5 A

Line regulation = 4 mV for V_{in} = 17.5 V to 30 V

The load regulation will depend on the conditions of measurement. The foregoing load regulation is for T_J = 25°C and V_{in} = 23 V. Similarly, the foregoing line regulation is for T_J = 25°C and I_L = 500 mA. In each case, the junction temperature of the device is 25°C.

20.4.4 The LM7800 Series

The LM78XX series (where XX = 05, 06, 08, 10, 12, 15, 18, or 24) is typical of the three-terminal voltage regulators. The 7805 produces an output of +5 V, the 7806 produces +6 V, the 7808 produces +8 V, and so on, up to 7824, which produces an output of +24 V.

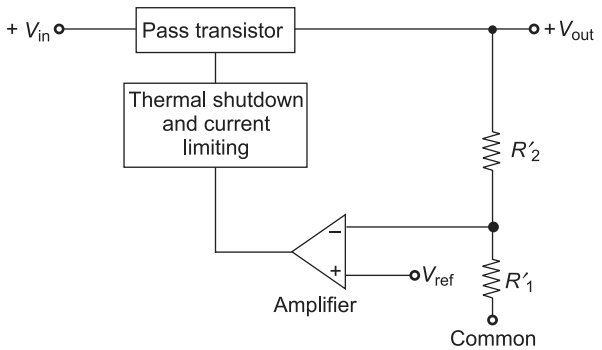


Fig. 20.8 *Functional block diagram of three-terminal IC regulator*

Figure 20.8 shows the functional block diagram for the 78XX series. A built-in reference voltage V_{ref} drives the non-inverting input of an amplifier. The voltage regulation is similar to our earlier discussion. A voltage divider consisting of R'_1 and R'_2 samples the output voltage and returns a feedback voltage to the inverting input of a high-gain amplifier. The output voltage is given by

$$V_{\text{out}} = \frac{R'_1 + R'_2}{R'_1} V_{\text{ref}}$$

In this equation, the reference voltage is equivalent to the zener voltage in our earlier discussions. The primes attached to R'_1 and R'_2 indicate that these resistors are inside the IC itself, rather than being external resistors. These resistors are factory-trimmed to get the different output voltages (5 to 24 V) in the 78XX series. The tolerance of the output voltage is ±4 percent.

The LM78XX includes a pass transistor that can handle 1 A of load current, provided that adequate heat sinking is used. Also included are thermal shutdown and current limiting. **Thermal shutdown** means that the chip will shut itself off when the internal temperature becomes too high, around 175°C. This is a precaution against excessive power dissipation, which depends on the ambient temperature, type of heat

sinking, and other variables. Because of thermal shutdown and current limiting, devices in the 78XX series are almost indestructible.

20.4.5 Fixed Regulator

Figure 20.9(a) shows an LM7805 connected as a fixed voltage regulator. Pin 1 is the input, Pin 2 is the output and Pin 3 is ground. The LM7805 has an output voltage of +5 V and a maximum load current over 1 A. The typical load regulation is 10 mV for a load current between 5 mA and 1.5 A. The typical line regulation is 3 mV for an input voltage of 7 to 25 V. It also has a ripple rejection of 80 dB, which means that it will reduce the input ripple by a factor of 10,000. With an output resistance of approximately 0.01 Ω, the LM7805 is a very stiff voltage source to all loads within its current rating.

When an IC is more than 6 in from the filter capacitor of the unregulated power supply, the inductance of the connecting wire may produce oscillations inside the IC. This is why manufacturers recommend using a bypass capacitor C_1 on Pin 1 [Fig. 20.9(b)]. To improve the transient response of the regulated output voltage, a bypass capacitor C_2 is sometimes used on Pin 2. Typical values for either bypass capacitor are from 0.1 to 1 μF. The data sheet of the 78XX series suggests 0.22 μF for the input capacitor and 0.1 μF for the output capacitor.

Any regulator in the 78XX series has a drop-out voltage of 2 to 3 V, depending on the output voltage. This means that the input voltage must be at least 2 to 3 V greater than the output voltage. Otherwise, the chip stops regulating. Also, there is a maximum input voltage because of excessive power dissipation. For instance, the LM7805 will regulate over an input range of approximately 8 to 20 V. The data sheet for the 78XX series gives the minimum and maximum input voltages for the other preset output voltages.

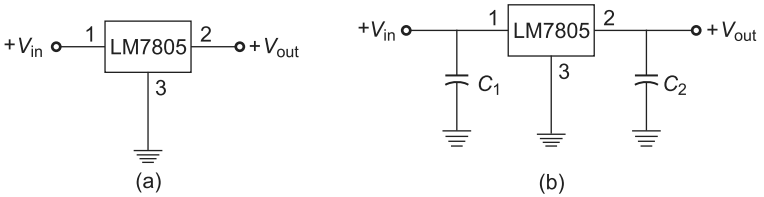


Fig. 20.9 *(a) Using a 7805 for voltage regulation (b) Input capacitor prevents oscillations and output capacitor improves frequency response*

Summary

➢ The regulated power supplies are explained and different types of regulators are discussed.

Exercises

Review Questions

1. Distinguish between analog and digital signals.
2. Draw an ideal digital waveform. Superimpose on it the actual wave. What is its rise and fall time?
3. Sketch the voltage level of a digital signal, which determines high and low.
4. When is the output of an AND gate 1?
5. When is the output of an OR gate 0?
6. Draw the symbol of an XOR gate and write its truth table.
7. Show that a bubbled AND gate is equivalent to NOR gate.
8. State the De Morgan theorems.

9. What is the meaning of universality of NAND and NOR gates?
10. How can you realise XOR gate by NAND gates?
11. Draw the symbol and write the truth table of the exclusive NOR gate.
12. Explain is an IC.
13. Describe the scheme of regulation of a series regulator. Why should it be less than the input voltage?
14. What is a pass transistor?
15. What determines the output voltage in a series regulator? Why should it be less than the input voltage?
16. Describe the scheme of regulation of a shunt regulator.
17. In applications why is a series regulator preferred over shunt regulator?
18. Draw the circuit diagram of a series regulator with a single transistor and also with op-amp.
19. Why is current-limiting protection essential for series regulator?
20. Draw the circuit of a series regulator with current limiting. Describe its operation.
21. Draw the circuit of a series regulator with feedback current limiting. Describe its operation. Why is it superior to ordinary current limiting?
22. For IC regulators:
    (a) What is dropout voltage?
    (b) Define line and load regulation.
    (c) What is meant by on-card regulation?
    (d) What is an adjustable regulator and its range of adjustment? What are its three terminals?
    (e) Explain the operation of a three-terminal regulator of Fig. 20.8.

Problems

1. For the series regulator of Fig. 20.10, calculate V_o and zener diode current. What will be these values if V_i reduces to 12 V?
2. Identify the kind of regulatoring in Fig. 20.11. Calculate V_o and I_z.

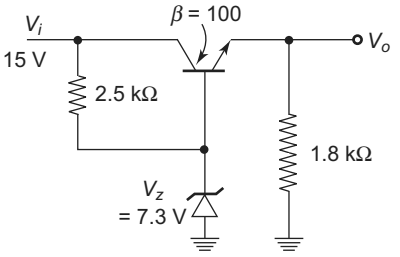


Fig. 20.10

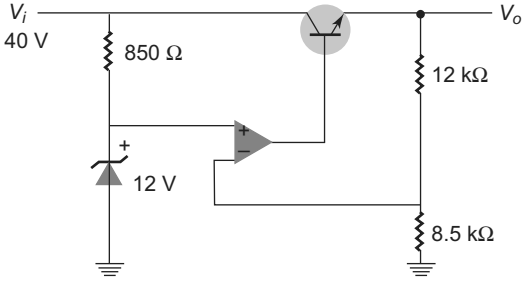


Fig. 20.11

3. For the regulator circuit of Fig. 20.12, calculate the approximate value of V_{out}. What is the power dissipation of the pass transistor?

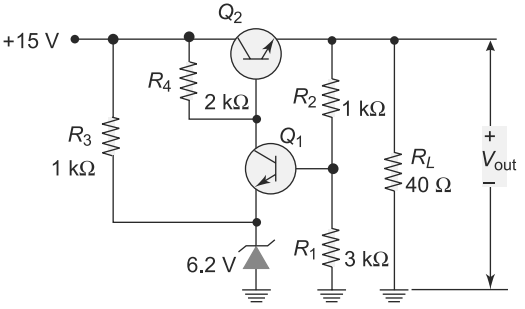


Fig. 20.12

Hint: I_c is approximately same as load current.

4. Calculate the efficiency of the regulator of Fig. 20.12.

Multiple-Choice Questions

1. A voltage regulator circuit is that which
   (a) smoothens the ac variation in dc output voltage
   (b) converts ac voltage to dc voltage
   (c) maintains a constant dc output voltage in spite of the fluctuations in ac voltage or load current
   (d) none of the above
2. Which of the following voltage regulators is preferred for providing large values of load current?
   (a) Transistor series regulator (b) Zener diode shunt
   (c) Transistor shunt regulator (d) None of these
3. An ideal voltage regulator has voltage regulation of
   (a) 50 (b) 1 (c) 100 (d) 0
4. The main job of a voltage regulator is to provide a nearly …….. output voltage.
   (a) fluctuating (b) smooth (c) constant (d) sinusoidal
5. The output voltage of a step-down-type switching voltage regulator depends on
   (a) input voltage (b) transistor on time (c) duty cycle (d) all of these
6. In a feedback series voltage regulator circuit, the output voltage is regulated by controlling the ….
   (a) reference voltage
   (b) magnitude of input voltage
   (c) gain of the feedback transistor
   (d) voltage drop across the series pass transistor
7. A switching voltage regulator can be of the following type:
   (a) Inverting (b) Step down (c) Step up (d) All of these
8. The power efficiency of a switching voltage regulator is much higher than that of a linear regulator because of
   (a) cut-off (b) saturation (c) high duty cycle (d) it is like a switch
9. Which of the following is not an essential element of dc power supply?
   (a) Filter (b) Voltage amplifier (c) Rectifier (d) Voltage regulator
10. As compared to voltage regulators made up of discrete components, IC regulators have the inherent advantage(s) of
   (a) Self-protection against over temperature (b) remote control
   (c) current limiting (d) all of these

Answers

Problems

1. $V_o = 8$ V, $I_Z = 3.034$ mA, V_o no change, $I_Z = 1.836$ mA
2. Series regulator, $V_o = 28.94$, $I_Z = 0.033$ mA
3. $V_{out} = 9.2$ V, $P_D = 1.33$ W
4. 61.4%

Multiple-Choice Questions

1. (c) 2. (a) 3. (d) 4. (c) 5. (d) 6. (d) 7. (d) 8. (d) 9. (b) 10. (d)

Digital Logic

chapter 21

Goals & Objectives

- Introduction to analog/discrete (digital) signal
- Switching and logic levels of digital waveforms
- Discussion of characterisation of digital ICs—speed operation, power description, current and voltage parameters, noise immunity and fan-out
- Description and functional operation of logic gates

21.1 INTRODUCTION

In an analog (continuous) form of information (signal), the signal may acquire any value in a range of the independent variable (say time). In a discrete (or digital) form, the signal can have any value but it would remain constant over periods of time (called *sampling periods*), which usually are of uniform duration. An audio signal (which is analog) can be recorded on a phonograph in the form of a continuous groove of depth varying in accordance with signal strength (at constant speed, which converts time to distance variable). Alternatively, discrete values of audio signal could be recorded on a laser disc in a pattern of flat areas of holes, which reflect or do not reflect light. Of course, discretisation must be over short-enough intervals so as to preserve the amplitude and frequency information of the original analog signal. Figure 21.1 shows the process of discretising (or sampling) an analog signal, which could also be reversed.

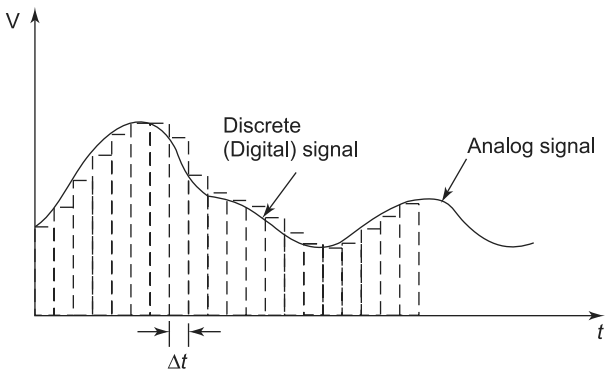


Fig. 21.1 *Analog/discrete (digital) signal*

Usually, nonphysical signals (generally called information) are inherently discrete in the form of numbers pertaining to intervals of time, e.g. monthly cash flow of a company. The information could also be a set of numbers pertaining to the value of a variable/parameter recorded (at usually uniform intervals) during say, an environmental study. Discrete signals, physical/nonphysical, are conventionally and speedily processed in digital form and so are also called *digital signals*. Digital signal could be processed independently disassociated from the original intervals called *off-line* processing, or may have to be processed, for example, in a digital control system within the constraint imposed by the time interval, called *on-line* processing.

Digital signals or numbers, in general, are processed by means of digital systems using the concept of binary numbers and Boolean algebra. A digital computer is a genera-purpose digital item. The numbers are coded in the form of binary (ON/OFF) electrical pulses and processed by means of logic gates and memory cells. The logic gates and memory cells exploit the controlled switch behaviour of electronic devices. *Binary signals* are used extensively in communication, control and instrumentation systems as well in computers. Binary signals have the great advantage of being far less susceptible to disturbance (noise) compared to analog signals.

Even in large-scale digital systems, only a few different operations need to be performed, although these have to be repeated many times at a very fast speed. Logic, arithmetic and memory in conjunction with input, output devices/circuits are the five constituents of a digital system. In this chapter, we shall begin by studying the basic logic gates and their electronic realisation. Appropriate concepts of binary numbers and *Boolean algebra* will be introduced simultaneously. Our focus will be on operation of fundamental building blocks of four major technologies—Transistor-Transistor Logic (TTL), Emitter-Coupled Logic (ECL), NMOS and CMOS. In this chapter, we will restrict ourselves to logic gates and simple combinational circuits.

21.2 SWITCHING AND LOGIC LEVELS

Consider the simple circuit of Fig. 21.2 with switch *S*. The switch can be in two distinct states—OFF/ON. With *S* in OFF state, the output voltage is $V_o = 5$ V (HIGH) and with *S* in ON state, $V_o = 0$ V (LOW). In digital circuits, variables which can acquire only two values are indicated as '0' and '1' invoking a branch of algebra known as *Boolean algebra* and these are known as *Boolean* or *binary variables*. We can identify OFF as '0' and ON as '1' at the input and LOW as '0' and HIGH as '1' at the output. We immediately see that input '0' results in output '1' and vice versa, i.e. the circuit (also called switching circuit) of Fig. 21.2 accomplishes state inversion. Such circuits are known as *logic gates*. This particular circuit is an inverter or a NOT gate. It is symbolically represented in Fig. 21.3(a) with the table of input-output relationship called *truth table* as in Fig. 21.3(b), and input-output waveform relationship as in Fig. 21.3(c).

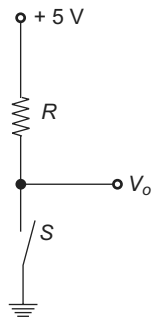


Fig. 21.2 *Switching circuit*

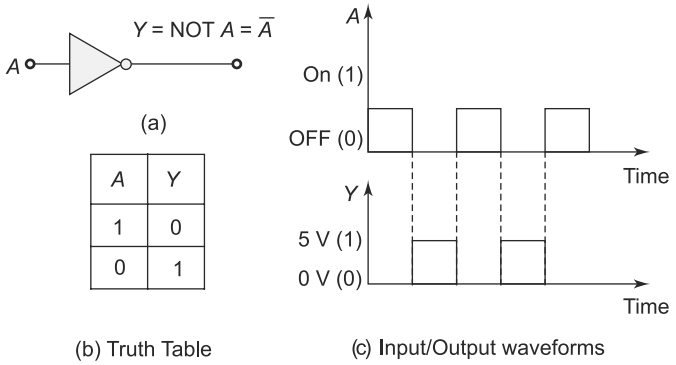


Fig. 21.3 *Inverter or NOT gate*

In Boolean algebra, output is expressed as

$$Y = \text{NOT } A = \overline{A} \text{ or complement of } A \tag{21.1}$$

A is known as a Boolean variable.

It can easily be recognised by a truth table that $\overline{\overline{A}} = A$.

In electronic switching circuits, 0 and 1 states are represented by voltage levels which are indeed a range of values with a clear margin between the high end of LOW and low end of HIGH. For example, if 0 is normally represented as 0 V and 1 as 5 V, their voltage ranges may be 0 to 0.3 V and 4.7 to 5 V with a margin of 4.4 V(4.7 – 0.3 = 4.4 V).

Buffer

When a larger current I_o has to the fed to a load than what can be provided by a gate, a buffer is connected between the gate and load. Its symbol and truth table are shown in Fig. 21.4.

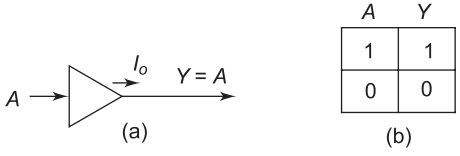


Fig. 21.4 *(a) Buffer symbol (b) Buffer truth table*

21.3 DIGITAL WAVEFORM

The digital waveforms shown in Fig. 21.5 are ideal where 5 V = high = 1 and 0 V = low = 0. Also the change over from H(1) to L(0) and vice versa is in zero time.

Actual Waveform (Voltage Level)

In high output, the digital circuit acts as a source which feeds the load. Therefore,

$$V_o(H) < 5 \text{ V (say)}$$

It can have minimum value

$$V_{oH\,\min} = 3.5 \text{ V (say)}$$

This is to be recognised that $H(1)$

$$V_o = +5 \text{ V to } 3.5 \text{ V}$$

In low state, the digital circuit acts as a sink receiving current from the source. So,

$$V_o(L) > 0$$

Its maximum value to be recognised as zero is

$$V_o = 0 \text{ to } V_{oL\max} = 0.2 \text{ V (say)}$$

The forbidden region is then

$$(V_{oH\min} - V_{oL\max}) = 3.5 - 0.2 = 3.3 \text{ V}$$

where the signal cannot be recognised as $H(1)$ or $L(0)$.

The above conclusions are illustrated in Fig. 21.5.

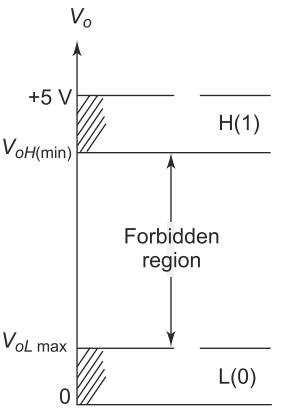


Fig. 21.5 *Logic level profile*

21.4 CHARACTERISATION OF DIGITAL ICs

The various characteristics of digital ICs that can be used to compare their performances are

1. Speed of operation
2. Power dissipation
3. Current and voltage parameter
4. Noise immunity
5. Fan-out

Speed of Operation

A pulse signal in getting through an inverter is not an exact inverted replica. Further, it gets delayed in time called propagation delay which includes the switching of the transistor. This delay is once again illustrated by somewhat idealised input/output waveforms of an inverter. Typical gate delays are 1–20 nanoseconds. This delay limits the frequency of the input signal, and the cycle time must be larger than the propagation delay.

Power Dissipation

The output voltage and current waveforms of a logic gate are shown in Fig. 21.6. As neither $V(0)$ nor I_{OFF} are zero, there is a power consumption under static condition (0 or 1). Also there is a power consumption during the switching intervals $T_1 < t < T_2$ and $T_3 \le t \le T_4$ which is the dynamic power. The dynamic power rises to a peak value and then falls off.

Both static and dynamic dissipation contribute to the total power consumption of a gate. Sometimes static dissipation is a dominant factor. In VLSI with CMOS fabrication technology, the dynamic power dissipation is the dominant factor as static dissipation is slow.

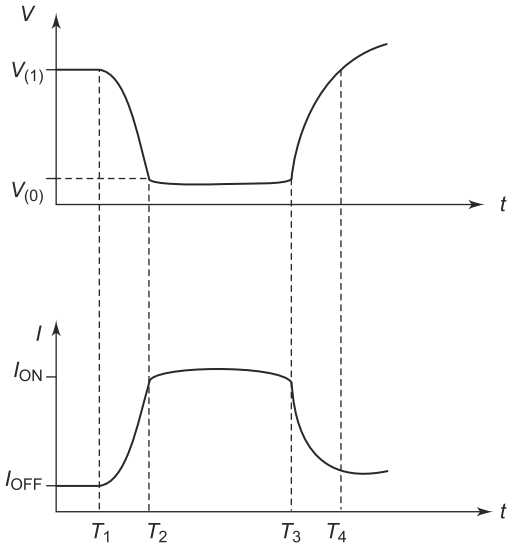


Fig. 21.6 *Voltage and current waveforms*

Noise Immunity

This is essentially a measure of how much stray noise voltage the device can handle without giving any error at the output level.

Fan-out

It is the number of gates that a gate in HIGH output state can feed without its output voltage dropping by more than the allowable noise margin $(NM)_H$.

Fan-in

It is the number of gates that can be allowed to sink their current into feeder gate in low state.

21.5 LOGIC GATES

Logic gate is an electronic circuit, which accepts a binary input and produces a binary output, namely 0 and 1. The inverter (NOT) logic gate in general accepts one or more inputs and produces one output. Apart from the NOT gate considered in Section 21.2, it has one input and one output, but a logic gate in general accepts one or more inputs and produces one output. There are six other types of logic gates.

Input to a gate will be designated by binary variables *A*, *B*, *C*, etc. and the output will be indicated by the binary variable *Y*. As stated earlier, binary variables can take on values 0 and 1 which are electronically represented by LOW and HIGH voltage levels. In terms of Boolean algebra, the function of a logic gate will be represented by a binary expression. Boolean algebra will be dealt with in detail in Chapter 23.

21.5.1 AND Gate

Consider the diode circuit of Fig. 21.7. Assuming the diodes to be ideal, it is immediately obvious that the output will be HIGH only if both the inputs are HIGH and so both diodes are OFF. Such a logic operation is called AND and is represented by the Boolean expression

$$Y = A \text{ AND } B = A \cdot B \tag{21.2}$$

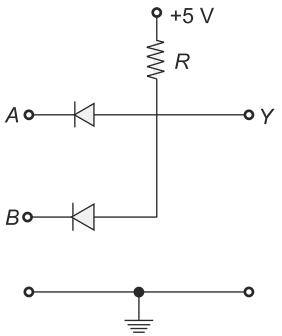
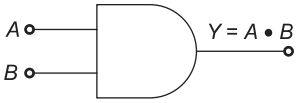


Fig. 21.7 *An AND gate*

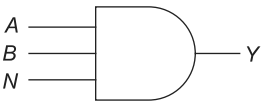
Here dot indicates ANDing. The logic symbol for an AND gate is drawn in Fig. 21.8(a) with its truth table is given in Fig. 21.8(b).



(a) Symbol

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(b) Truth table



(c) AND gate with N inputs

Fig. 21.8 *AND gate*

Additional information that can be drawn from the truth table are the Boolean relations

$A \cdot 0 = 0$; $B = 0$
$A \cdot 1 = A$; $B = 1$
$A \cdot A = A$; $B = A$

In general, an AND gate can accept more than one input, which is symbolically represented in Fig. 21.8(e) and whose Boolean expression is

$$Y = A \cdot B \cdot C \cdot \cdots \cdot N \tag{21.3}$$

Note: In an AND gate, output is 1 only when all inputs are 1(HIGH).

21.5.2 OR Gate

Consider the diode circuit of Fig. 21.9. The output will be HIGH, if A or B (or both) are HIGH. Such a logic operation is called OR and is expressed by the Boolean expression

$$Y = A \text{ OR } B = A + B$$

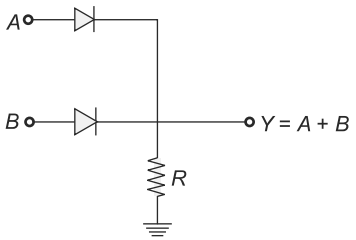


Fig. 21.9 *An OR gate*

The symbolic representations of OR and its truth table are given in Figs. 21.10(a) and (b). It is evident from the truth table that

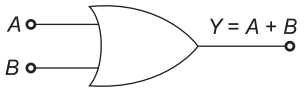
$$A + 0 = A;\ B = 0 \tag{21.4}$$

$$A + 1 = 1;\ B = 1$$

$$A + A = A$$

An N-input OR gate is represented in Fig. 21.10(c) whose Boolean expression is

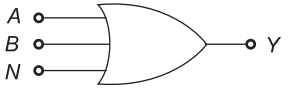
$$Y = A + B + C + \cdots + N \tag{21.5}$$



(a) Symbol

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table



(c) OR gate with N inputs

Fig. 21.10 *OR gate*

Note: Output of OR gate is 0 only when both (all) inputs are 0 (low).

Bubbled (Small Circle) Notation

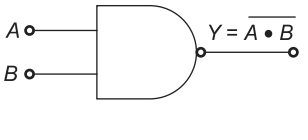
A bubble at the output and/or input of a gate means *inversion*. This notation has already been used in NOT gate (inverter).

21.5.3 NAND Gate

It is an AND gate followed by a NOT gate represented by the symbol of Fig. 21.11(a), wherein the small circle (bubble) indicates NOT operation. The NAND truth table is shown in Fig. 21.11(b). Its Boolean expression is

Y = NOT (A AND B) = $\overline{A \cdot B}$; complement of AND (21.6)

A NAND gate could have more than two inputs.



(a) Symbol

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(b) Truth table

Fig. 21.11 *NAND gate*

Note: The output is 0 only when both inputs are 1 (High).

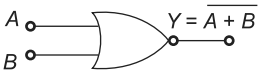
21.5.4 NOR Gate

Logically, a NOR is expressed as

Y = NOT (A OR B) = $\overline{A + B}$; complement of OR (21.7)

The symbolic representation of NOR gate and its truth table are shown in Fig. 21.12(a) and (b). There could be more than two inputs.

Note: Output is 1 only when both inputs are 0 (Low).



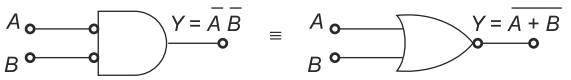
(a) Symbol

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

(b) Truth table

Fig. 21.12 *NOR gate*

21.5.5 Bubbled AND Gate

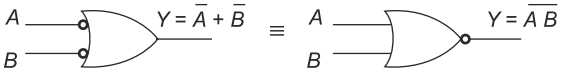


Bubbled AND ≡ NOR

Truth table proof

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}\cdot\overline{B}$	A + B	$\overline{A + B}$
0	0	1	1	1	0	1
0	1	1	0	0	1	0
1	0	0	1	0	1	0
1	1	0	0	0	1	0

Similarly



Bubbled OR ≡ NAND

Fig. 21.13

The above results directly follow from *De Morgan theorems:*

1. $$Y = \overline{A + B} = \overline{A}\,\overline{B} \tag{21.8}$$

2. $$Y = \overline{AB} = \overline{A} + \overline{B} \tag{21.9}$$

21.5.6 Universality of NAND/NOR Gates

NAND and NOR gates are called universal logic gates, because any logic operation can be realised by using these gates. This is illustrated by some examples.

Consider the NAND gate of Fig. 21.14(a) with input A at both ports. Then

$$Y = \overline{A \cdot A} = \overline{A} = \text{NOT } A$$

Similarly for the NOR gate of Fig. 21.13(b),

$$Y = \overline{A + A} = \overline{A} = \text{NOT } A$$

The reader should verify these by writing the truth tables.

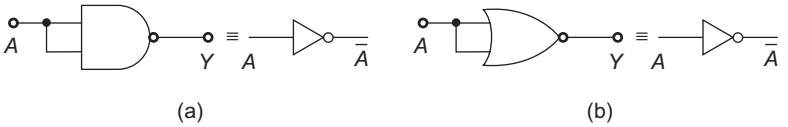


Fig. 21.14 *NOT gate realisation by NAND/NOR*

21.5.7 OR Realisation by NAND/NOR

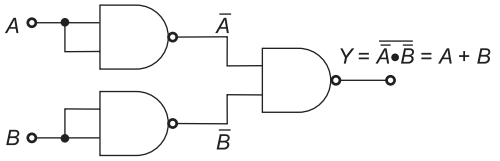
Consider the logic circuit of Fig. 21.15(a) composed of NANDs. Here,

$$Y = \overline{\overline{A} \cdot \overline{B}}$$

Its truth table is given in Fig. 21.15(b). It immediately follows that[1]

$$Y = \overline{\overline{A} \cdot \overline{B}} = A + B = A \text{ OR } B$$

Thus, the logic circuit of Fig. 21.14(a) is an OR realisation by NAND gates.



A	$\overline{A}$	B	$\overline{B}$	$\overline{A}\cdot\overline{B}$	$\overline{\overline{A}\cdot\overline{B}}$	$A+B$
0	1	0	1	1	0	0
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	0	1	0	0	1	1

(b)

Fig. 21.15 *OR realisation by NANDs*

1. This indeed is application of De Morgan's theorems.

OR realisation by NOR gates is given in Fig. 21.16 whose operation is obvious.

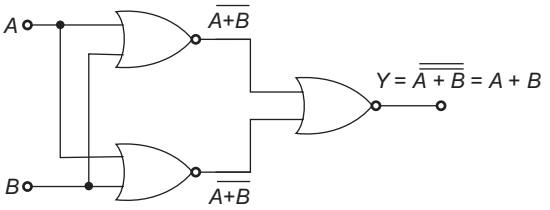


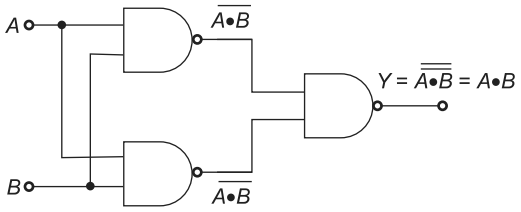
Fig. 21.16 *NOR realisation of OR*

Example 21.1

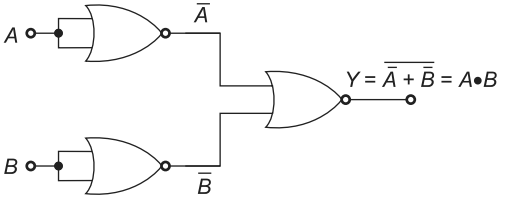
Consider the logic circuits of NAND/NORs of Figs 21.17(a) and (b) respectively. Find the output in each case.

Solution NAND circuit of Fig. 21.17(a) and NOR circuit of Fig. 21.17(b) are two realisations of AND. While the operation is obvious for the NAND circuit of Fig. 21.17(a), for the NOR circuit of Fig. 21.17(b), the AND operation is proved in the truth table of Fig. 21.17(c).

Observe that circuits of NAND realisation of OR [Fig. 21.17(a)] and NOR realisation of AND [Fig. 21.17(b)] have the same structure; vice versa also applies. See Figs 21.16 and 21.17(a).



(a) NAND realisation of AND



(b) NOR realisation of AND

A	$\bar{A}$	B	$\bar{B}$	$\bar{A} + \bar{B}$	$\overline{\bar{A} + \bar{B}}$	$A \cdot B$
0	1	0	1	1	0	0
0	1	1	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	1

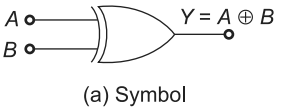
(c) Truth table of the circuit

Fig. 21.17

21.5.8 Exclusive OR (EXOR) Gate

The output of this gate is high only when either of the inputs is high but not when both inputs are high, i.e. either, but not both. The gate, symbol, truth table are shown in Figs 21.18(a), (b) and (c) respectively. In terms of Boolean algebra,

$$Y = A \text{ XOR } B = A \oplus B \tag{21.10}$$



(a) Symbol

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(b) Truth table

Fig. 21.18 *EXOR gate*

NAND implementation of Exclusive OR is shown in Fig. 21.19.

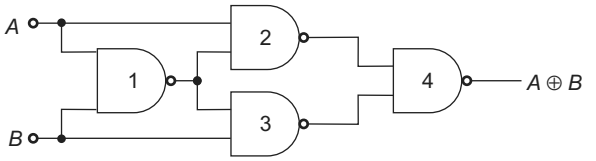


Fig. 21.19 *NAND implementation of EXOR*

Output gate 1 $\overline{AB}$

Output gate 2 $\overline{\overline{AB}A}$

Output gate 3 $\overline{\overline{AB}B}$

Output gate 4 $Y = \left[\overline{\overline{AB}A} \cdot \overline{\overline{AB}B}\right]$

Applying De Morgan's theorem repeatedly,

$$Y = \overline{(AB + \overline{A})(AB + \overline{B})} = \overline{AB + \overline{A}} + \overline{AB + \overline{B}}$$

or $$Y = \overline{AB} \cdot A + \overline{AB} \cdot B = \overline{A}B(A + B)$$

or $$Y = (\overline{A} + \overline{B})(A + B)$$

or $$Y = \overline{A}B + A\overline{B}$$

Its truth table is given below.

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}B$	$A\overline{B}$	Y
0	0	1	1	0	0	0
0	1	1	0	1	0	1
1	0	0	1	0	1	1
1	1	0	0	0	0	0

Thus,

$$Y = A \oplus B, \text{ exclusive } OR$$

Note: For multiple inputs, EXOR output will be 1 if the number of 1 inputs is odd.

21.5.9 Exclusive NOR Gate

It is the gate complementary to EXOR gate. Its symbol and truth table are shown in Figs 11.20(a) and (b) respectively. The output (Y) is 1 only when both inputs are same (0, 0) or (1, 1)

(a) Symbol

A	B	Y
0	0	1
0	1	0
0	1	0
1	1	1

(b) Truth table

Fig. 21.20 *Exclusive NOR gate*

21.5.10 AND-OR-Invert (AOI) Circuit

And-OR-Invert circuit is drawn in Fig. 21.21. Its output is

$$Y = \overline{AB + CD}$$

Each of the AND gates could have more than two inputs.

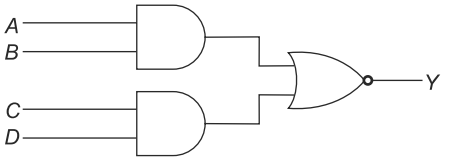


Fig. 21.21 *AOI circuit*

Inhibit (Enable) Operation

Consideration a two-input AND gate with an additional *Strobe* (S) terminal through an inverter represented by a bubble.

The output

$$Y = AB\overline{S}$$

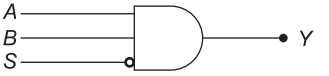


Fig. 21.22 *AND gate with Strobe*

If $A = 1, B = 1$, output $Y = 1$ only if $S = 0$, the gate is enabled. However, if $S = 1$.

$$Y = AB\overline{S} = 0$$

The gate is inhibited.

The above applies to AND gate with any number of inputs.

Two-input Gate

Input B through bubble (inverted) is

$$B = 1$$

Gate is inhibited and

$$Y = 0$$

Fig. 21.23 *Two-input gate*

Example 21.2

Realise the following gates using universal NAND gate combinations:

(a) NOT gate (b) AND gate (c) OR gate

(d) NOR gate (e) XOR gate

Solution

(a) NOT gate using NAND

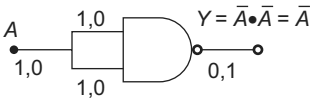


Fig. 21.24

(b) AND gate using NAND

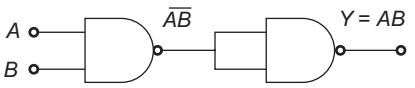


Fig. 21.25

(c) OR gate using NAND

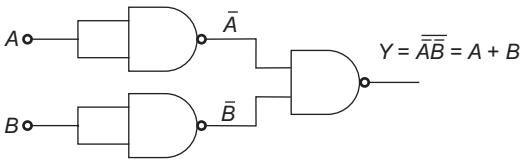


Fig. 21.26

(d) NOR gate using NAND

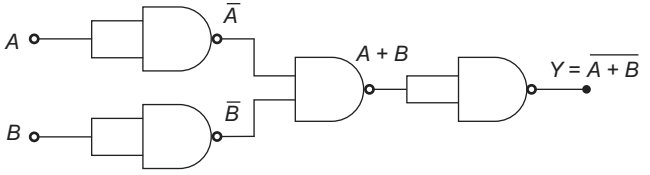


Fig. 21.27

(e) XOR gate using NAND

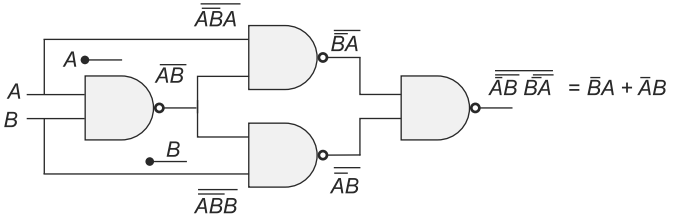


Fig. 21.28

Example 21.3

Realise following gates using universal NOR gate combinations:

(a) NOT gate (b) OR gate (c) AND gate (d) NAND gate (e) XOR gate

Solution

(a) NOT gate using NOR

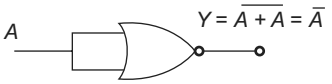


Fig. 21.29

(b) OR gate using NOR

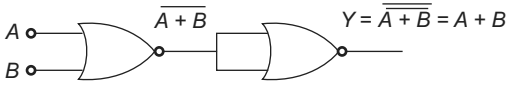


Fig. 21.30

(c) AND gate using NOR

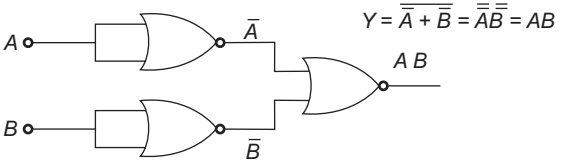


Fig. 21.31

(d) NAND gate using NOR

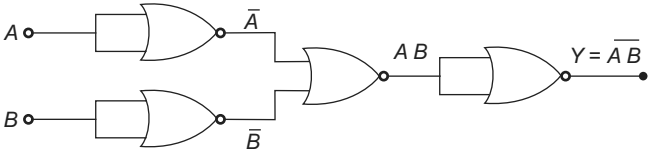


Fig. 21.32

(e) XOR gate using NOR

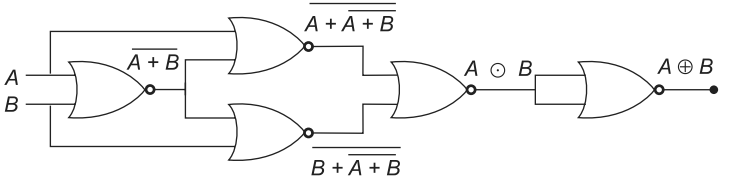


Fig. 21.33

Example 21.4

Enlist the Basic Boolean laws.

Solution

1. Commutative law
   (a) $A + B = B + A$
   (b) $AB = BA$
2. Associative law
   (a) $(A + B) + C = A + B\,(B + C)$
   (b) $(AB)C = A\,(BC)$
3. Distributive law
   (a) $A(B + C) = AB + AC$
   (b) $A + (BC) = (A + B)\,(A + C)$
4. Identity law
   (a) $A + A = A$
   (b) $AA = A$
5. Redundance law
   (a) $A + AB = A$
   (b) $A(A + B) = A$
6. Inverse law
   (a) $A + \overline{A} = 1$
   (b) $A \cdot \overline{A} = 0$

Example 21.5

In brief, explain the characteristics of logic gates and mention the number for TTL.

Solution

Fan-out: The measure of the maximum number of logic gates that can be driven by a single logic gate without affecting the specified operation characteristics of the driving gate is called fan-out. A standard fan-out for TTL is ten (10).

Fan-in: The measure of the maximum number of inputs that can be connected to a logic gate without affecting the specified operational characteristics of the driven logic gate is called fan-in. A standard fan-in for TTL is ten(10).

Example 21.6

Prove De Morgan's theorem.

Solution Using basic logic gates, we prove (a) $\overline{AB} = \overline{A} + \overline{B}$ (b) $\overline{A + B} = \overline{A} + \overline{B}$

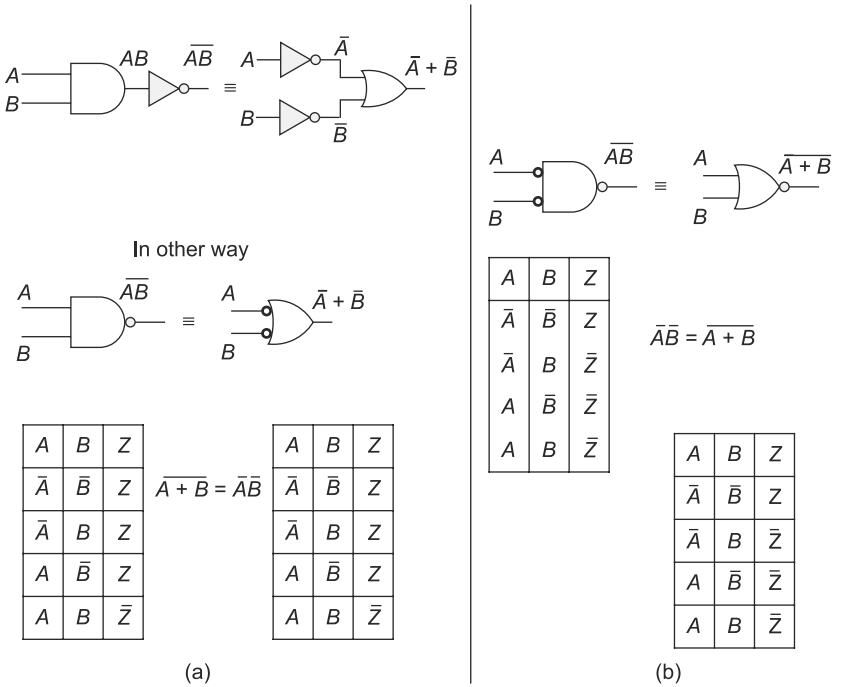


Fig. 21.34

Example 21.7

Simplify the following Boolean expressions.

(a) $\boldsymbol{A + AC}$

$$A + AC = A\,(1 + C)$$
$$= A\,1$$
$$= A$$

(b) $\boldsymbol{A + \overline{A}B}$

$$A + \overline{A}B = (A + \overline{A})(A + B)$$
$$= 1(A + B)$$
$$= (A + B)$$

(c) $\boldsymbol{A + \overline{A}B + AB\overline{C}}$

$$A + \overline{A}B + AB\overline{C} = A(1 + B\overline{C}) + \overline{A}B$$
$$= A1 + \overline{A}B$$
$$= A + \overline{A}B$$
$$= (A + \overline{A})\,(A + B)$$
$$= 1(A + B)$$
$$= (A + B)$$

(d) $\boldsymbol{A + \overline{A}B + ABC + A\overline{C}}$

$$\begin{aligned} A + \overline{A}B + ABC + A\overline{C} &= (A + \overline{A})(A + B) + C(AB + \overline{A}) \\ &= 1(A + B) + C(A + \overline{A}) \\ &= (A + B) + C \\ &= A + B + C \end{aligned}$$

(e) $\boldsymbol{AC + \overline{A}\,\overline{C}}$

$$\begin{aligned} \overline{A}C + \overline{A}\overline{C} &= \overline{A}C + \overline{A} + \overline{C} \\ &= \overline{A}(C + 1) + \overline{C} \\ &= \overline{A} + \overline{C} \end{aligned}$$

(f) $\boldsymbol{(B + \overline{C})(\overline{B} + C) + \overline{\overline{A} + \overline{B} + \overline{C}}}$

$$\begin{aligned} (B + \overline{C})(\overline{B} + C) + \overline{\overline{A} + B + \overline{C}} &= B\overline{B} + \overline{B}\overline{C} + C\overline{C} + BC + \overline{\overline{A}}\,\overline{B}\,\overline{\overline{C}} \\ &= \overline{B}\overline{C} + BC + A\overline{B}C \\ &= \overline{B}\overline{C} + (B + A\overline{B})C \\ &= \overline{B}\overline{C} + (B + \overline{B})(B + A)C \\ &= \overline{B}\overline{C} + (B + A)C \\ &= \overline{B}\overline{C} + BC + AC \end{aligned}$$

(g) $\boldsymbol{\overline{\overline{\overline{A} + B} + \overline{C}}}$

$$\begin{aligned} \overline{\overline{\overline{A} + B} + \overline{C}} &= \overline{\overline{\overline{A} + B}}\,\overline{\overline{C}} \\ &= (A + B)C \\ &= AC + BC \end{aligned}$$

(h) $\boldsymbol{\overline{AB + \overline{A\overline{B}} + A}}$

$$\begin{aligned} \overline{AB + \overline{A\overline{B}} + A} &= \overline{AB}\,\overline{A}\,\overline{\overline{A\overline{B}}} \\ &= (\overline{A} + \overline{B})ABA \\ &= AB(\overline{A} + \overline{B}) \\ &= A\overline{A}B + AB\overline{B} \\ &= 0 + 0 \\ &= 0 \end{aligned}$$

(i) $\boldsymbol{AB + \overline{A} + \overline{AB}}$

$$\begin{aligned} AB + \overline{A} + \overline{AB} &= AB + \overline{A} + \overline{A} + \overline{B} \\ &= AB + \overline{A} + \overline{B} \\ &= AB + \overline{AB} \\ &= 1 \end{aligned}$$

(j) $\overline{(\bar{A}+C)(B+\bar{D})}$

$$\overline{(\bar{A}+C)(B+\bar{D})} = \bar{\bar{A}} + \bar{C} + \bar{B} + \bar{\bar{D}}$$

$$= A\bar{C} + \bar{B}D$$

Example 21.8

Prove the following equalities.

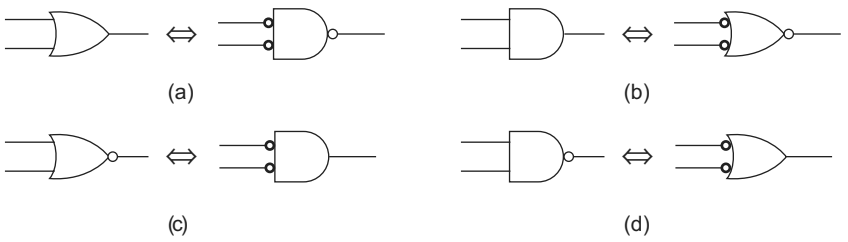


Fig. 21.35

Solution Let inputs be A, B and output be Y. We will use De Morgan's theorems.
Left = Right

(a) $Y = A + B = \overline{\bar{A}\cdot\bar{B}} = A + B$

(b) $Y = AB = \overline{\bar{A} + \bar{B}} = AB$

(c) $Y = \overline{A + B} = \bar{A}\bar{B}$

(d) $Y = \overline{AB} = \bar{A} + \bar{B}$

Example 21.9

For the NAND-NAND circuit of Fig. 21.36, write the truth table given if the change from each step of the truth table needs 1μs time; draw the timing diagram.

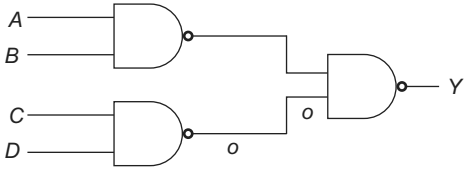


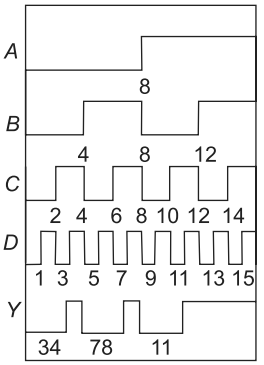
Fig. 21.36

Solution In a NAND, output is zero only if both inputs are 1. The truth table is given in Fig. 21.37(a) and timing diagram in Fig. 21.37(b). It is to be noted that the inputs change in synchronism at each circuit time.

$$Y = \overline{\overline{AB}\cdot\overline{CD}} = AB + CD$$

A	*B*	*C*	*D*	*Y*
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(a) Truth table



(b) Timing diagram

Fig. 21.37

Summary

- Analog and digital signals have been introduced. Digital ICs are discussed.
- Resumption and functional operation of logic gates is presented.

Exercises

Review Questions

1. How can you convert octal numbers to binary and vice versa?
2. How can you convert hexadecimal to binary and vice versa?
3. Write the basic rules for addition and subtraction of binary numbers.
4. Take any two 8-bit binary numbers. Illustrate how to add and subtract the two.
5. What are signed numbers? What is their range? How do they compare with unsigned numbers?
6. What is 2's complement of a negatives number? How is it found?
7. How is 2's complement in subtraction? If the answer is negative, how can you find its magnitude?
8. State De Morgan's laws.
9. What is the ASCII Code?
10. What is BCD?
11. What is a BCO to decimal converter? What gates are used at the output end?
12. What is the input and output of a half adder?
13. Draw the circuit for a full adder using two half adders.
14. In a full adder, the sum is obtained as the output of an XOR gate. Show how.
15. What is the input and output of a full adder?

Problems

1. Draw the logic circuit whose Boolean equation is

   $Y = \overline{A + B} + \overline{C}$

2. Draw the logic circuit described by

   $Y = (\overline{ABC})\overline{D}$

3. Draw the logic circuit given by the Boolean equation

   $Y = \overline{A}BC + A\overline{B}C + \overline{A}B\overline{C}$

   You may use triple-input ANDs.

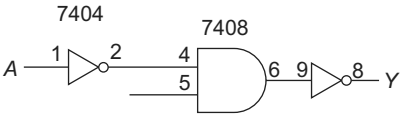


Fig. 21.38

4. Write the truth table for Fig. 21.38
5. In Fig. 21.39, determine Y if (i) both switches are open, and (ii) both switches are closed.

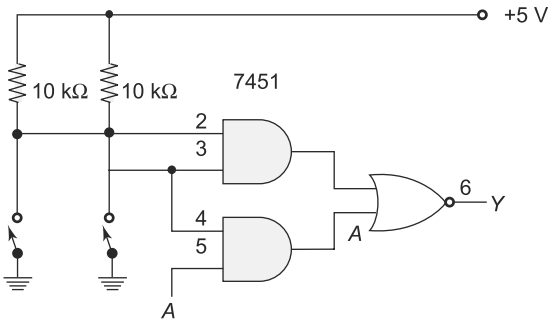


Fig. 21.39

6. For Figs 21.40(a) and (b), sketch the output (Y) waveforms.

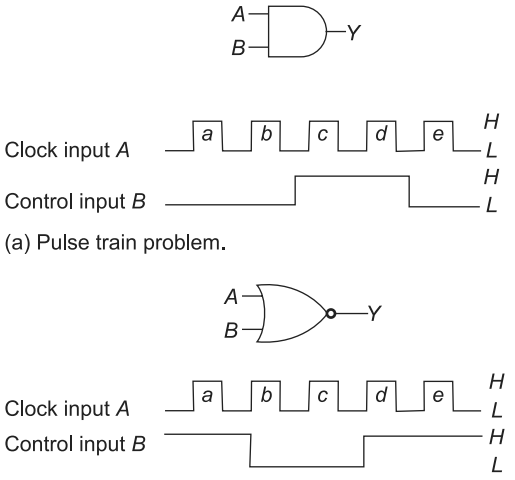


Fig. 21.40

7. Prove that the figures below are logically equivalent:

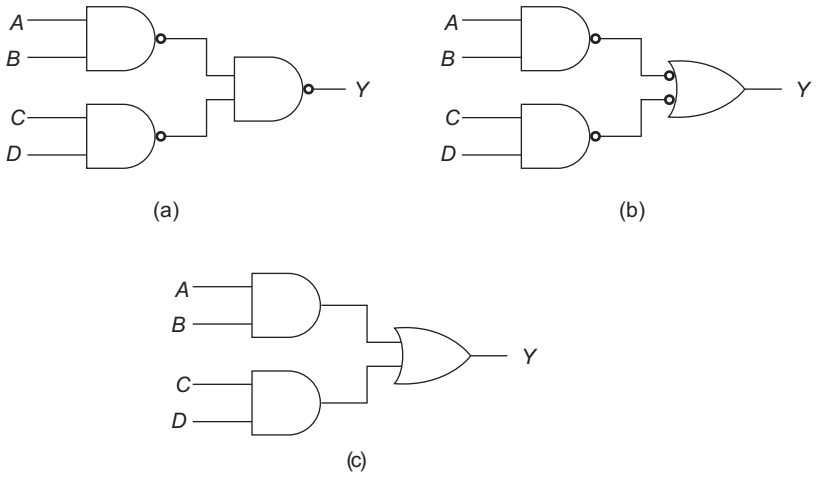


Fig. 21.41

8. Assume that the switch in Fig. 21.42 is controlled by a voltage, such that $V_i(0)$ makes the switch open and $V(1)$ closes it. Let the switch have an ON resistance of 20 Ω. Find the value of R that ensures $V_o(0) > 4$ V and $V_o(1) < 0.5$ V.
9. The waveforms shown in Fig. 21.43 are applied to the logic circuit shown therein. Plot the output waveform.

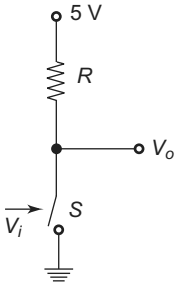


Fig. 21.42

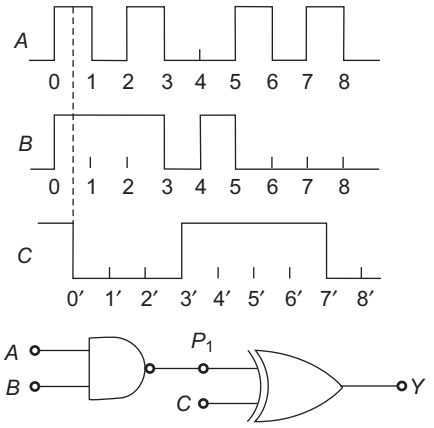


Fig. 21.43

10. Sketch an EXOR gate. Connect its input terminals to High(1). Show that it gets on as an inverter.

Multiple-Choice Questions

1. The universal gates are
   (a) NAND gate (b) AND gate (c) NOR gate (d) EX-OR gate
2. The output of a two-input EX-OR gate is
   (a) $\overline{a}\,b + a\,\overline{b}$ (b) $\overline{ab + bc}$ (c) $\overline{a}\,\overline{b} + a\,b$ (d) none of these
3. How many NAND gates will require to implement an AND gate?
   (a) 2 (b) 3 (c) 4 (d) 5
4. The equation $\overline{a \cdot b}$ represents
   (a) X-OR gate (b) X-NOR gate (c) NAND gate (d) NOR gate
5. NAND and NOR are called universal gates because
   (a) they have least propagation delay
   (b) they are available every where
   (c) all the other gates can be implemented using these gates
   (d) they are easy to process
6. A three-variable input can have how many compilations of input?
   (a) 8 (b) 9 (c) 3 (d) None of these
7. According to commutative law,
   (a) $A + B = B + A$ (b) $AB = BA$ (c) $\overline{A + B} = \overline{A} \cdot \overline{B}$ (d) both (a) and (b)
8. The fan-in par standard TTL is
   (a) 100 (b) 10 (c) 1 (d) 12
9. $A + \overline{A}B + ABC + \overline{A}C$ can be reduced as
   (a) $A + B + C$ (b) $\overline{A} + B + C$ (c) $A + B + \overline{C}$ (d) none of these
10. $AB + \overline{A} + A\overline{B}$ is
    (a) 1 (b) 0 (c) A (d) $\overline{A}$

Answers

Problem

4. (i) $\overline{A}$ (ii) 1

Multiple-Choice Questions

1. (a) and (c) 2. (a) 3. (b) 4. (a) 5. (c) 6. (a) 7. (d) 8. (b) 9. (a) 10. (a)

Digital Electronics

chapter 22

Goals & Objectives

- Introduction to number systems—decimal number, binary number, hexadecimal number and complement of binary number system
- Introduction and explanation of binary number system and number conversion
- Conversion of octal number system—octal to binary and binary to octal conversion
- Conversion of hexadecimal number system—hexadecimal to binary and binary to hexadecimal
- Introduction and implementation of codes, Boolean relations and algebraic simplifications
- Explanation of Boolean algebra theorems and their operations
- Classification of digital circuits—logic gates, combinational circuits, multiplexers and decoders
- Introduction of sequential circuits and general model of sequential circuits

22.1 INTRODUCTION

The term *digital* refers to any process that is accomplished using discrete units. Each of these could be used as a unit or group of units to express a whole number. In contrast with digital numbers, analog numbers are represented as directly measurable quantities such as volts, speed and distance. It means analog numbers represent real things. Both the analog and digital methods are used for computing. The abacus was the first computing device; the word "*abacus*" means making *marks in the dust*. From this early beginning, the Greeks and Romans developed a system of counting involving beads on a marble table. The beads were grouped for units, tens, hundreds, and so on. Since then, we have come a long way. Today computers have been developed which can perform millions of operations per second.

22.2 NUMBER SYSTEMS

There are four number systems of arithmetic that are used in the digital systems:

1. Decimal
2. Binary
3. Hexadecimal
4. Octal

22.2.1 Decimal Number System

The decimal number system has ten symbols, and any number of any magnitude can be expressed by using this system of positional weighting. For example, 6841 can be broken down as

$$6841 = 6000 + 800 + 40 + 1$$

$$= 6 \times 10^3 + 8 \times 10^2 + 4 \times 10^1 + 1 \times 10^0$$

The principle of positional weighting can be extended to any number system. A number can be represented by the equation

$$N = d_n * r^n + d_{n-1} * r^{n-1} + \ldots d_2 * r^2 + d_1 * r^1 + d_0 * r^0 \tag{22.1}$$

where N is the value of the entire number,
d_n is the value of the n^{th} digit from the decimal point, and
r is the *radix* or *base*.

Number of digitals $(n + 1)$; $(0, 1, 2, \ldots, n)$

22.2.2 Binary Number System

In this, each position in a number can take only one of two values: 0 or 1. These positions are called *bits*, a contraction of the words *binary digits*. The primary advantage of using this binary counting system as opposed to the 10-discrete line method in the decimal number system is that it minimises the number of lines required to two. Binary numbers are used extensively throughout all digital systems because of the very nature of electronics. A "1" can be represented by a saturated transistor, a light turned on, a relay energised or a magnet magnetised in a particular direction. A "0" can be represented as a cut-off transistor, a light turned off, a de-energised relay, or the magnet magnetised in the opposite direction. We will study the binary number system in detail for the above reasons. Table 22.1 gives the binary representations of decimal numbers from 0 to 15.

Table 22.1 *Binary representations of decimal numbers from 0 to 15*

Binary	*Decimal*
0000	0
0001	1
0010	2
0011	3
0100	4
1101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

From the table it is clear that using 4 bits we can represent decimal numbers from 0 to 15. Like the decimal system, the binary is also positionally weighted. Each position represents a particular value of 2^n.

$$1_2 = 0 \times 2^0 = 1$$

$$1010_2 = 1 * 2^3 + 0 * 2^2 + 1 * 2^1 + 0 * 2^0 = 8 + 0 + 2 + 0 = 10$$

The base is indicated by the subscript. Because of this property of positional weighting, the procedure for converting a binary number to decimal is very similar to that of breaking a decimal number into its weighted values. In Eq. (22.1), *d*'s will all be 0s or 1's, the *r*'s will all be 2, and the radix and the *n*'s will be various powers of 2, depending on the position of the digit with reference to the binary point.

Example 22.1

Convert 1101101_2 to decimal.

Solution

$$\begin{aligned} N &= d_6 * r^6 + d_5 * r^5 + d_4 * r^4 + d_3 * r^3 + d_2 * r^2 \_ d_1 * r^1 + d_0 * r^0 \\ &= 1 * 2^6 + 1 * 2^5 + 0 * 2^4 + 1 * 2^3 + 1 * 2^2 + 0 * 2^1 + 1 * 2^0 \\ &= 64 + 32 + 0 + 8 + 4 + 0 + 1 \\ &= 109_{10} \end{aligned}$$

Example 22.2

Convert 101010101 to decimal; the radix may not be always indicated.

Solution

$$N = d_8 \times r^8 + d_7 \times r^7 + d_6 \times r^6 + d_5 \times r^5 + d_4 \times r^4 + d_3 \times r^3 + d_2 \times r^2 + d_1 \times r^1 + d_0 \times r^0$$
$$= 1x2^8 + 0x2^7 + 1x2^6 + 0x2^5 + 1x2^4 + 0x2^3 + 1 \times 2^2 + 0x2^1 + 1x2^0$$
$$= 256 + 0 + 64 + 0 + 16 + 0 + 4 + 0 + 1$$
$$= 341_{10}$$

The above example provides the way for converting binary numbers to decimal numbers. However, in digital circuits, it is necessary to convert from decimal to binary also.

Converting Decimal to Binary

This is the reverse process of the previous section. The first method requires the table of powers of 2. Starting with the decimal number to be evaluated, obtain the largest power of 2 from the table without exceeding the original number. Then subtract this number obtained from the table from the original number. Repeat this process for the remainder and continue until the remainder is zero. Finally, add the binary numbers obtained from Table 22.2. The result will give the corresponding binary number.

Table 22.2 *Decimal-to-binary conversion*

	Powers of 2	
2^n	N	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.0625
32	5	0.03125
64	6	0.015625
128	7	0.0078125
256	8	0.00390625
512	9	0.001953125
1024	10	0.0009765625
2048	11	0.00048828125
4096	12	0.000244140625
8192	13	0.0001220703125
16348	14	0.00006103515625
32768	15	0.000030517578125
65536	16	0.0000152587890625

Example 22.3

Convert 69_{10} to binary.

Solution From the above table, 64 is the largest number without exceeding 69.

$64 = 1000000_2$; $69 - 64 = 5$; from the table, 4 is the largest number without exceeding 5.

$4 = 100_2$; $5 - 4 = 1$, one is the largest number in the table

$1 = 1_2$; Adding the binary numbers

$$\begin{array}{r} 1000000 \\ 100 \\ 1 \\ \hline \end{array}$$

Therefore, $69_{10} = 10000101_2$

The second method is successive division by 2 and the remainders recorded. In this, the last remainder is the *most significant* bit (*MSB*).

Example 22.4

Convert 69 to binary.

Solution

$$\begin{array}{l|l} 2) \underline{69} & \uparrow \\ 2) \underline{34 - 1} & \\ 2) \underline{17 - 0} & \\ 2) \underline{\ 8 - 1} & \\ 2) \underline{\ 4 - 0} & \\ 2) \underline{\ 2 - 0} & \\ \quad 1 - 0 & \\ \hline \end{array}$$

Read the remainders from bottom to top.

$69_{10} = 1000101_2$. This is same as the result of Example 22.3.

Binary Addition and Subtraction

Addition is accomplished in a similar manner to that in decimal, addition.

Example 22.5

Add 101111_2 and 10111_2.

Solution

$$\begin{array}{ll} \text{Number 1} & 1\ 0\ 1\ 1\ 1\ 1 \\ \text{Number 2} & \quad 1\ 0\ 1\ 1\ 1 \\ \hline & 1\ 0\ 0\ 0\ 1\ 1\ 0_2 \end{array}$$

During the addition, 1 + 1 = 10 and 1 + 1 + carry(1) = 11, and so on.

Example 22.6

Add 1111 and 1111.

Solution

Number 1:		1	1	1	1
Number 2:		1	1	1	1
Carry:		1	1	1	
	1	1	1	1	0_2

Binary subtraction is performed in a manner similar to that in decimal subtraction. Because there are only two digits in binary, its subtraction often requires more borrowing operation than decimal numbers.

Example 22.7

Subtract 1110 from 1000.

Solution

$$\begin{array}{r} 10000 \\ 1110 \\ \hline 00010_2 \end{array}$$

we find that in the second column 1 cannot be subtracted from 0. So a 1 must be borrowed the from third column but it is a 0. In this example, 1 is available at the fifth column. So borrow this 1, leaving behind a 0. Then 1 is (1 + 1) in the fourth column. We borrow 1 leaving behind 1 in the fourth column. Finally, successive borrowing makes (1 + 1) in the second column from which we subtract 1, yielding 1 as answer in the second column. At this stage, we have the answers for zeroth and first column. The third, fourth and fifth columns are

Column	5	4	3
	0	1	1
		1	1
	0	0	0

Thus, the complete answer is

$$00010_2 = 2_{10}$$

Example 22.8

Subtract 10101 from 101010.

Solution

$$\begin{array}{r} 101010 \\ 10101 \\ \hline 10101_2 \end{array}$$

Binary Multiplication

Example 22.9

Multiply 1111_2 by 101_2.

Solution

$$
\begin{array}{r}
1111 * 101 \\
\hline
1111 \\
0000 \\
1111 \\
\hline
1001011_2 \\
\hline
\end{array}
$$

The above method is a paper method and cannot be used by a computer. Multiplying a 4-bit number by another 4-bit number yields an eight-bit number results.

Binary Division

Like multiplication, division can be accomplished by two methods: Paper and computer method. The paper method is long-division procedures.

Example 22.10

Divide 110110_2 by 110_2.

Solution

$$
\begin{array}{r}
1001 \\
110\overline{)110110} \\
110 \\
\hline
0110 \\
110 \\
\hline
0
\end{array}
$$

The computer method uses successive subtraction. Assume the above example with 8-bit representation; dividend is to be divided by the divisor in 4-bit representation. That is, dividend is 00110110, and divisor is 0110. The quotient will be formed in the right half of the *MQ* register and the remainder in the left half. The dividend is first placed in the *MQ* register and divisor in the *D* register. The divisor is then subtracted from the dividend. The result is considered positive if the most significant bit (the far left bit or the ninth bit) is a 0, and negative if it is a 1. If the result is positive then the error has occurred for the quotient would be greater than four bits.

Computer Division Method

MQ	0011 0110	
Subtract *D*	0110	
M*Q*	1101 0110	Result is negative; the division is valid
Add *D*	0110	
MQ	0011 0110	
Shift *MQ* left	0110 1100	
Subtract *D*	0110	
	0000 1100	Result is positive
Add 1 to quotient	1	
MQ	0000 1101	
Shift *MQ* left	0001 1010	
Subtract *D*	0110	

	1111 1010	Result is negative
Add *D*	0110 ____	
MQ	0001 1010	Put a zero quotient
Shift *MQ* left	0011 0100	
Subtract *D*	0110 ____	
	1101 0100	Result is negative
Add *D*	0110 ____	
	0011 0110	Put a zero quotient
Shift *MQ* left	0110 1000	
Subtract	0110 ____	
	0000 1000	Result is positive
	0000 1000	
Add I to quotient	_____ 1	
	0000 1001	Final answer
	Remainder Quotient	

If the result is negative then the quotient will be four or less bits sufficiently small to be contained in a 4-bit register. The *MQ* register is next shifted left one bit and the divisor subtracted from it. If the result is positive, 1 is added to the *Least Significant Bit* (*LSB*) of the *MQ* register, where the quotient is accumulated. If it is negative, the divisor is added to *MQ* and the *MQ* shifted left one bit. This effectively puts a 0 in this bit of the quotient. The process is continued until the *MQ* register has been shifted left four bits the number of bits in the D register. The remainder is then in the left half of the *MQ* register and the quotient in the right half.

22.2.3 Hexadecimal Number System

The hexadecimal number system was born out of the need to express binary numbers concisely and is by far the most commonly used number system in computer literature. The hexadecimal number is formed from a binary number (word) by grouping bits in groups of four bits each, starting at the binary point. This is a logical way of grouping since computer words come in 8 bits, 12 bits, 16 bits, 32 bits, and so on. In a group of 4 bits, the decimal number 0–15 can be represented by a unique symbol. So 10–15 is represented by symbols A, B, C, D, E and F.

Converting Binary to Hexadecimal

Binary numbers can be easily converted to hexadecimal by grouping in groups of four starting at the binary point.

Example 22.11

Convert 1010111011110101_2 to hexadecimal.

Solution

1010	1110	1111	0101	Group in four = from LSB
A	E	F	5	Convert each number

Table 22.3 *Conversion table*

Decimal	*Hexadecimal*	*Binary*
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111
16	10	10000
32	20	100000
64	40	1000000
100	64	01100100
255	FF	1111 1111
511	1FF	1 1111 1111
1024	400	100 0000 0000

Converting Hexadecimal to Binary

It can be converted to binary by converting each digit.

Example 22.12

Convert $FA876_{16}$.

Solution

F	A	8	7	6
1111	1010	1000	0111	0110

Thus, the solution is 1111, 1010, 1000, 0111, 0110_2.

Converting Hexadecimal to Decimal

Hexadecimal number is also a positionally weighted system, where the radix is 16.

$$N = d_4 * 16^4 + d_3 * 16^3 + d_2 * 16^2 + d_1 * 16^1 + d_0 * 16^0$$

Example 22.13

Convert $FA27D_{16}$.

Solution

$$F * 16^4 + A * 16^3 + 2 * 16^2 + 7 * 16^1 + D * 16^0$$

$$= 15 * 65536 + 10 * 4096 + 2 * 356 + 7 * 16 + 13$$

$$= 10,24,637$$

Converting Decimal to Hexadecimal

Any decimal number can be converted to hex by successively dividing by 16. The remainders can then be converted to hex, and read up from the bottom to obtain the hexadecimal results.

Example 22.14

Convert 57345.

Solution

16) 57345 ↑
16) 3584 – 1
16) 224 – 0
14 – 0

14 00 1 ⟶ Convert decimal to hexadecimal notation.
↓
E 0 0 1_{16}

The result is $E001_{16}$.

22.2.4 Octal Numbers

This was used extensively by early minicomputers. The octal system is formed by grouping bits in groups of 3, starting at the binary point.

Binary to Octal Conversion

Example 22.15

Convert 111110101101_2 to octal.

Solution

Split the number into group of three	111	110	101	101
	7	6	5	5

The result is 7655_8

Example 22.16

Convert 6754_8 to binary.

Solution

6 7 5 4
110 111 101 100

The result is 110111101100_2.

Example 22.17

Convert 867_{10} to octal number. It is simply a successive division by 8.

Solution

8) 867
8) 108 – 3
8) 13 – 4
1 – 5

The result is $(1543)_8$

22.2.5 Complement of Binary Numbers

The computer arithmetic process is done not only with positive numbers; it is also done with negative numbers. In such a condition, signed and unsigned numbers are dealt by the processors. The 1's and 2's complement operation is useful for this type of arithmetic process.

1's complement of a binary number is just an inversion of individual bits. For example, the 1's complement of 1010101 is found by inversion of each bit, i.e. 0 to 1 and 1 to zero conversion.

1's complement of $(1010101)_2$
is $(0101010)_2$

The 2's complement of a positive binary number whose integral part has p digits is also found by subtracting the number from 2^p. For instance, 2's complement of 11010 is

$$2^5 - 11010 = 100000 - 11010 = 00110$$

2's complement of 101100001 is

$$2^4 - 1011.001 = 10000 - 1011.001$$

$$= 0100.111$$

The 2's complement of 0 is defined to be 0.

The 2's complement of a given binary number is also found by adding 1 to the least significant bit of the 1's complement of that binary number. The 2's complement of the number $(10101011)_2$ is found by two steps. First, convert the given number into its 1's complement by inversion.

$1010101 \rightarrow 0101010$ is the 1's complement of the number. Then add one to the least significant bit (LSB). So

0101010
1

0101011_2 – 2's complement of the number is $(1010101)_2$. 2's complement is used to represent negative numbers.

The above procedure also applies for a decimal binary number. For example,

To find 2's complement of	0.1110100
1's complement	0.0001011
	+1
2's complement	0.0001100
To find 2's complement of	1011.001
1's complement	0100.110
	+1
2's complement	0100.111

Difference of Two Positive Binary Numbers (m – n)

1. To m add 2's complement of n.
2. If the sum has a carry at the left end, delete it. The result is $(m - n)$.
3. If the sum has no carry at the left end, take 2's complement of the sum. Attach a negative sign. The result is $(m - n)$.

Example 22.18

Given m = 11010110, n = 01000101

Determine (a) $(m - n)$ and (b) $(n - m)$

Solution

(a) 2's complement of n

	01000101
1's complement	10111010
	+1
2's complement	10111011
Add in	11010110
Delete carry →1	10010001
$(m - n)$	10010001

(b) 2's complement of m

	11010110
1's complement	00101001
	+1
2's complement	00101010
Add n	01000101
No carry	01101111
1's complement	10010000
	+1
2's complement $(n - m)$	–10010001

22.3 BOOLEAN ALGEBRA THEOREMS

A Boolean algebra is a set of binary operations, + and *, and a unary operation, –, and elements 0, 1 such that the following laws hold: commutative and associative laws for addition and multiplication, distributive laws both for multiplication over addition and for addition over multiplication. The applications of digital logic involve functions of the AND, OR, and NOT operations.

In Boolean algebra, a variable A called *bilateral*, can take on two values, 1/0. Three basic binary operations are defined here before proceeding further.`

AND—Multiplication Symbol (.)

$Y = A$ AND $B = A \cdot B$

Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

In AND operation, the output is 1 only if both A and B are 1; otherwise it is zero.

OR—Addition Symbol (+)

$Y = A + B$

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

In OR operation, the output is '1' if either A or B or both are 1.

NOT—Complement, Symbol (super –, super', may also be used)

$Y = \overline{A}$

Truth Table

A	Y
0	1
1	0

In a NOT operation, the output is the reverse of input.

❑ Special Case

AND Operation

$A \cdot 0 = 0, \quad A \cdot 1 = A$

$A \cdot A = A, \quad A \cdot \overline{A} = 0$

OR Operation

$A + 0 = A, A + 1 = 1, A + A = A, A + \overline{A} = 1$

These results follow from the truth tables by replacing B with 0, 1 or $\overline{A}$

$$\overline{\overline{A}} = A$$

Boolean identities of common use are presented in Table 22.4.

Table 22.4 *Some identities of Boolean algebra*

Name	*AND form*	*OR form*
Identity law	$1 \cdot A = A$	$0 + A = A$
Null law	$0 \cdot A = 0$	$1 + A = 1$
Idempotent law	$A \cdot A = A$	$A + A = A$
Inverse law	$A \cdot \overline{A} = 0$	$A + \overline{A} = 1$
Commutative law	$A \cdot B = B \cdot A$	$A + B = B + A$
Associative law	$(A \cdot B) \cdot C = A \cdot (B \cdot C)$	$(A + B) + C = A + (B + C)$
Distributive law	$A + BC = (A + B) \cdot (A + C)$	$A(B + C) = AB + AC$
Absorption law	$A \cdot (A + B) = A$	$A + AB = A$
De Morgan's law	$\overline{A \cdot B} = \overline{A} + \overline{B}$	$\overline{A + B} = \overline{A}\,\overline{B}$

As the AND operation is unambiguous, we may omit the dot(.). Thus, we can write $A \cdot B \cdot C$ as ABC.

De Morgan's Theorem

$\overline{A + B} = \overline{A} \cdot \overline{B}$ and $\overline{A \cdot B} = \overline{A} + \overline{B}$

This is the most important logic theorem for digital electronics, which states that any logical binary expression remains unchanged if we

1. Change all variables to their complements,
2. Change all AND operations to ORs,
3. Change all OR operations to ANDs, and
4. Take the complement of the entire expression.

A practical operational way to look at De Morgan's theorem is that the inversion bar of an expression may be broken at any point and the operation at that point is replaced by its opposite (i.e. AND replaced by OR or vice versa).

Proofs of Some Results of Table 22.4

❑ Distributive Law

$$(A + B)(A + C) = AA + AC + BA + BC$$
$$= A + A(B + C) + BC$$
$$= A[1 + (B + C)] + BC$$
$$= A + BC \quad \text{as} \quad 1 + (B + C) = 1$$

❑ Absorption Law

$$A(A + B) = AA + AB = A + AB$$
$$A(1 + B) = A$$

22.4 DIGITAL CIRCUITS

Digital circuits are classified into two major categories: Combinational circuits and Sequential circuits. *Combinational circuits* are the circuits where output depends on the present input only. The *sequential circuit* produces the output on the basis of both present and previous inputs. It shows that sequential circuits have memory. Before studying these two types, first let us study the basic logic gates which will form the digital circuits.

22.4.1 Logic Gates

Logic gates are the building blocks of digital circuits. They are used to create digital circuits and even complex integrated circuits. Complex integrated circuits are complete circuits ready to perform several functions—microprocessors and microcontrollers are the best examples—the inner sub-circuits are formed using several logic gates. Combinations of logic gates form circuits designed with specific tasks in mind. For example, logic gates are combined to form circuits to add binary numbers (adders), set and reset bits of memory (flip-flops), multiplex multiple inputs, etc. The following section will give a brief idea of the different gates.

❑ **Representation of 0 and 1 in Logic Gates** In an electronic logic gate, 0 is represented by *low voltage* and 1 by *high voltage*.

NOT Gate

The NOT gate is also known as an *inverter*, because it changes the input to its opposite (inverts it). The NOT gate accepts one input and the output is the opposite of the input as shown in Fig. 22.1 and its truth table below it. In other words, a low-voltage input (0) is converted to a high-voltage output (1).

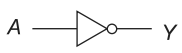


Fig. 22.1 *Inverter*

Table 22.5 *Truth table of NOT gate*

A (Input)	*Y (Output)*
0	1
1	0

AND Gate

As the name implies, an AND logic gate performs an "AND" logic operation, which is a logic multiplication. It has at least two inputs. So, if A and B are its inputs, at the output we will find $Y = A \cdot B$ AND gate symbol is shown in Fig. 22.2.

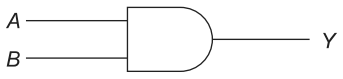


Fig. 22.2 *AND logic gate*

Table 22.6 *Truth table of AND gate*

A	*B*	*Y*
0	0	0
0	1	0
1	0	0
1	1	1

Another way to express AND logic gate is that its output will only be at "1" when all its inputs are also at "1". Otherwise, its output will be "0".

OR Gate

As its name implies, an OR logic gate performs an "OR" logic operation, which is logic addition. It has at least two inputs. So, if A and B are its inputs, at the output we will find $Y = A + B$. The OR gate symbol is drawn in Fig. 22.3 and its truth table besides it.

Fig. 22.3 *OR logic gate*

Table 22.7 *Truth table of OR gate*

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Another way to express OR logic gate is that its output will only be at "0" when all its inputs are also at "0". Otherwise, its output will be "1".

XOR Gate

XOR stands for *Exclusive-OR*. An XOR gate compares two values and if they are different, its output will be "1". The XOR operation is represented by the symbol ⊗. So $Y = A \otimes B$. The XOR logic gate symbol is given in Fig. 22.4 and its truth table along its side.

Fig. 22.4 *XOR logic gate*

Table 22.8 *Truth table of XOR gate*

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

So its output will only be at "0" when all its inputs have the same value. Otherwise, its output will be "1".

NAND Gate

This is an AND gate with the output inverted. The output is high when either of inputs A or B is high, or if neither is high. In other words, it is high, going low only if both A and B are high. Its symbol is presented in Fig. 22.5 with the truth table.

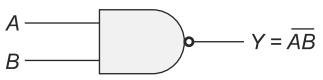


Fig. 22.5 *NAND logic gate*

Table 22.9 *Truth table of NAND gate*

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

This is an OR gate with the output inverted. The output is high only when neither *A* nor *B* are high. That is, it is normally high but any kind of nonzero input will make it low. Its symbol and truth table are presented in Fig. 22.6 and in Table 22.10, respectively.

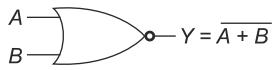


Fig. 22.6 *NOR logic gate*

Table 22.10 *Truth table of NOR gate*

A	*B*	*Out*
0	0	1
0	1	0
1	0	0
1	1	0

XNOR Gate

It is the complement of XOR gate. Its output is 1 when both inputs are equal, i.e. (0, 0) or (1,1). XNOR operation is represented as $Y = A \cdot B$. The symbol of XNOR gate and its truth table are given in Fig. 22.7 and Table 22.11

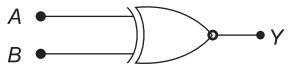


Fig. 22.7 *XNOR logic gate*

Table 22.11 *Truth table of XNOR gate*

A	*B*	*Y*
0	0	1
0	1	0
1	0	0
1	1	1

Non-inverter or Buffer

At a non-inverter, also known as a buffer, the value entered on its input will be found on its output. You may think that this is a crazy logic gate, since it does nothing. That's not true; it has several important applications in digital electronics, as we will explain below. Its symbol and truth table are presented in Fig. 22.8 and Table 22.12.

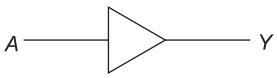


Fig. 22.8 *Non-inverter or buffer*

Table 22.12 *Truth table*

A	*Y*
0	0
1	1

A typical application for a buffer is to increase the *fan-out* of a given logic gate. Fan-out is the maximum number of gates a given integrated circuit is capable of being connected to. For example, if a given logic gate has a fan-out of three gates, its output can be only connected directly to three other logic gates. If you need to connect its output to more logic gates, you can use a buffer to increase the number of logic gates you can connect this output to.

22.4.2 Examples of Combinational Circuits

The half adder is an example of a simple functional digital circuit built from two logic gates. The half adder adds two one-bit binary numbers (*A* and *B*). The output is the sum of the two bits (*S*) and the carry (*C*). Figure 22.9 shows the schematic of half-adder circuit.

Note that the same two inputs are directed to two different gates. The inputs to the XOR gate are also the inputs to the AND gate. The input "wires" to the XOR gate are tied to the input wires of the AND gate.

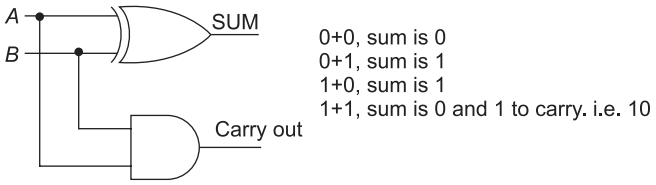


Fig. 22.9 *Half adder*

Table 22.13 *Half-adder truth table*

$S = A \oplus B$

$C = AB$

Row	*A*	*B*	*C*	*S*
0	0	0	0	0
1	0	1	0	1
2	1	0	0	1
3	1	1	1	0

The full-adder circuit adds three one-bit binary numbers ($A\ B\ C_i$) and outputs two one-bit binary numbers, a sum (*S*) and a carry (C_0), If you look at Fig. 22.10 closely, you'll see the full adder is simply two half adders joined by an OR.

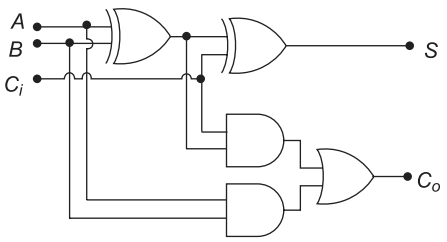


Fig. 22.10 *Full adder*

Table 22.14 *Full-adder truth table*

Row	*A*	*B*	C_{in}	C_{out}	*Out*
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	1

The full adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers. The carry input for the full-adder circuit is from the carry output from the circuit "above" itself in the cascade. The carry output from the full adder is fed to another full adder "below" itself in the cascade.

An *n*-bit adder can then be designed by connecting the carry out and carry in lines of *n* full adders. Figure 22.11 shows a 4-bit adder. This design is called a *ripple-carry* adder. Similarly, four 4-bit adders can be connected to form a 16-bit adder, etc.

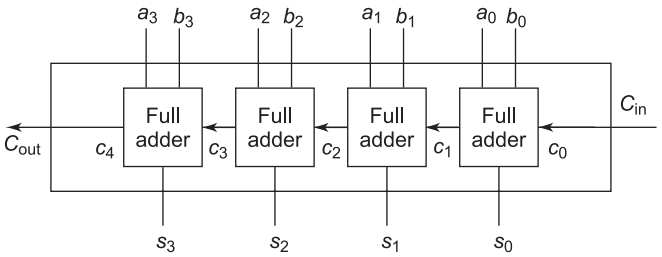


Fig. 22.11 *4-bit adder*

22.4.3 Multiplexers

The objective of a multiplexer is to select one signal from a group of 2^n inputs, to be an output on a single output line. For example, an 8-to-1 multiplexer (mux) is diagramed as a black box as shown in Fig. 22.12. Lines D_0, …D_7 are the data input lines and F is the output line. Lines A, B, and C are called the select lines. They are interpreted as a three-bit binary number, which is used to choose one of the D lines to be output on the line F.

Implementation

Design of an 8-to-1 multiplexer using traditional minimisation techniques would require minimising a Boolean function of 11 variables. Instead, a mux can be designed with a regular pattern of AND and OR gates, as shown in Fig. 22.13.

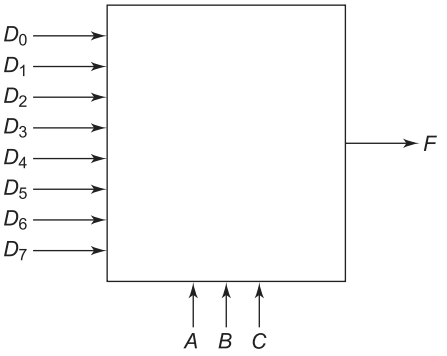


Fig. 22.12 *8-to-1 multiplexer*

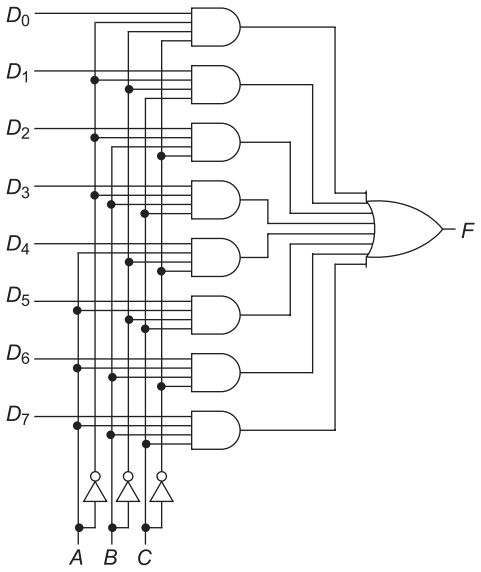


Fig. 22.13 *Implementation of an 8-to-1 multiplexer*

Any literal $A = 1, \overline{A} = 0$

Suppose we want to output $Y = D_5$, then the three inputs to the corresponding AND gate should be 111. Then

$$\left.\begin{aligned} D_5 = 0, \quad Y = 0 \\ D_5 = 1, \quad Y = 1 \end{aligned}\right\} \rightarrow Y = D_5$$

The corresponding select inputs are

$$5 \rightarrow 101 \text{ or } A\overline{B}C$$

And the output is $A\overline{B}C\ D_5$

Similarly to output D_6

$$6 \rightarrow 110 \rightarrow AB\overline{C}$$

Output is $AB\overline{C}D_6$

The output Y will be sum (+) of all eight (2^3) outputs.

Application

Choose one of several registers to be used as ALU input. A 2^n-to-1 multiplexer can be used to implement an arbitrary Boolean function of n variables, by associating each input line of the multiplexer with a row of the truth table for the function.

22.4.4 Decoders

The objective of the decoder is to decode an n-bit binary number, producing a signal on one of 2^n output lines. Figure 22.14 shows an 3-to-8 decoder.

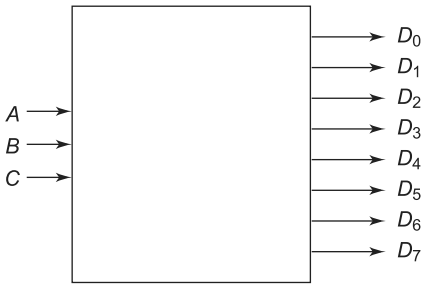


Fig. 22.14 *3-to-8 decoder*

Implementation

A decoder is often implemented with an additional input called an "enable" line. When the line is enabled, the circuit is a decoder. When it is disabled, all the outputs are 0. The same circuit can be used as a de-multiplexer, which directs a single data input line to one of 2^n output lines, depending on the values of n select lines. Figure 22.15 shows the 3-to-8 decoder implementation.

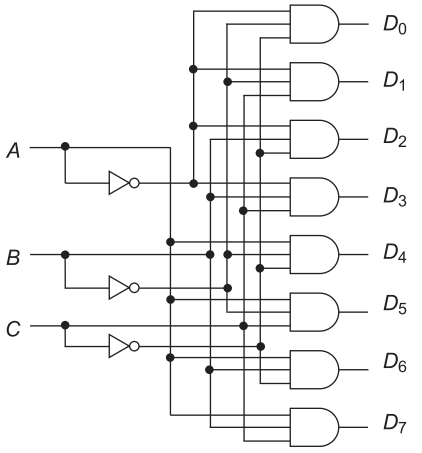


Fig. 22.15 *3-to-8 decoder implementation*

To Produce Output 1 at D_5

$5 \rightarrow 101$

If input is $A = 1$, $B = 0$, $C = 1$ or $A\bar{B}C$, the output is 1 and D_5. It can be checked that all other outputs are 0.

To produce 1 at D_3 we input $3 \rightarrow 011$ or $\bar{A}BC$

❑ **Reader** Find the input to produce 1 at D_7.

❑ **Application** Decode memory address for reads and writes to random access memory.

22.5 INTRODUCTION TO SEQUENTIAL CIRCUITS

The circuits we have studied so far (gates, multiplexers, decoders, adders) are all examples of combinational circuits. They have the property that their outputs depend only on the current input values (after some delay). Because of this property, combinational circuits are memoryless. Their outputs cannot depend on past input values which are no longer present. How can our logic design theory be extended to introduce memory elements? The simplest memory circuit is called an *SR* latch, as shown in Fig. 22.16.

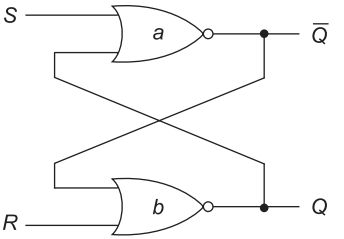


Fig. 22.16 *SR flip-flop*

Operation

We remind ourselves here that a NOR gate produces output 1 only when both inputs are 0, otherwise the output is 1.

❑ **Set State** Output $Q = 1$, $\overline{Q} = 0$

❑ **Reset State** Output $Q = 0$, $\overline{Q} = 1$

Let the *SR* FF be in set state. We make $S = 0$ and $R = 0$. The inputs to '*a*' NOR are (0, 1); so $\overline{Q} = 0$, and inputs to '*b*' NOR are (0, 0); so $Q = 1$. Therefore, *SR* F/F remains in set state, i.e. no state change.

It similarly shows that when the *SR* F/F is in reset state and we make $S = 0$, $R = 0$, it remains in reset.

Thus, if both inputs are zero ($S = R = 0$), the output state does not change.

If output is in set state ($Q = 1$, $\overline{Q} = 0$), we input $S = 1$, $R = 0$, F/F remains in set state. Let us input S = 0, $R = 1$. The inputs to '*b*' NOR are (0, 1) causing $Q = 0$. This in turn makes the input to '*a*' NOR as (0, 0) and so $\overline{Q}$ changes to 1. Thus, the state changes from set state to reset state.

Similarly, if the output is in reset state ($Q = 0$, $\overline{Q} = 1$), it remains so if $S = 0$ and $R = 1$. But changes to set state if $S = 1$ and $R = 0$.

Both $S = 1$ and $R = 1$ are not permitted as this would cause a conflict, and outcome would be uncertain.

The above operations of *SR* F/F are summarised in Table 22.15.

Table 22.15 *Truth table for SR flip-flop*

Inputs		*Present state*	*Next state*
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Not allowed	

It is seen that the output (Q and $\overline{Q}$) depends on the *S, R* inputs and the previous state. Thus, the latch holds one bit of data. Circuits involving latches are *called sequential* circuits. They include memory elements.

Within a digital computer, a clock is used to synchronise changes in the contents of memory elements. A clock is a signal which oscillates between 0 and 1, as shown in Fig. 22.17.

Fig. 22.17 *Clock signal*

The clock can be applied to a latch so that change in the latch's value can only occur when the clock is in the "1" (high) state. The result is a clocked *SR* latch shown in Fig. 22.18.

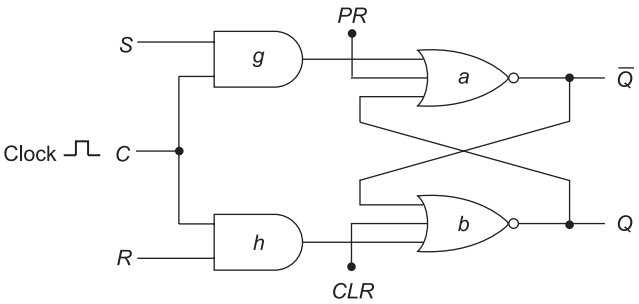


Fig. 22.18 *Clocked SR flip-flop*

When $C = 0$, the output of both AND gates is zero. So Q cannot change: the latch is non-operational.

When $C = 1$, output of gate g is $1.S = S$ and output of gate h is $1 \cdot R = R$, the latch is now operational.

The term *level-triggered* is applied to this type of latch to indicate that its ability to change value depends on the level (low or high) of the clock signal.

Clear and Preset

In Fig. 22.18, one additional input is provided to each NOR gate; CLR on Q side NOR and PR on $\overline{Q}$ side NOR. When CLR and PR are 0, the circuit behaves as an *SR* flip-flop as in Fig. 22.19. In the absence of a clock pulse ($C = 0$), the outer inputs to NOR gates are zero. Making CLR (clock) = 1, results in $Q = 0$ and $\overline{Q} = 1$, thereby clearing the flip-flop. Instead making PR (preset) = 1, results in $Q = 1$ and $\overline{Q} = 0$; thereby presetting the flip-flop. These are asynchronous inputs as their action does not need a clock pulse. The symbol of an *SR* flip-flop is sketched in Fig. 22.19. It may not be necessary to always label CLR and PR.

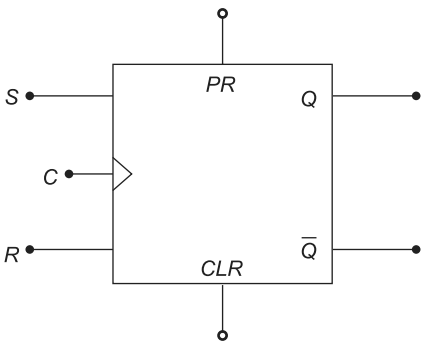


Fig. 22.19 *Symbol of SR flip-flop*

22.6 FLIP-FLOPS

For more precise synchronisation, "flip-flops" are used. They are edge-triggered which means that they can change only as a result of a change in the value of the clock signal; that is, on its rising or falling edge. One way to accomplish this is by the use of a small circuit, called a *pulse generator*, shown in Fig. 22.20.

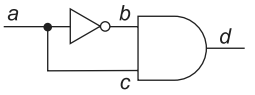


Fig. 22.20 *Pulse generator (edge triggering)*

When a is connected to a clock signal, a short pulse will be generated on d, wherever a makes a transition from 0 to 1 and 1 to 0.

There are four commonly used types of flip-flops: D, T, RS and JK. The behaviour of each of them can be described by a state table. The state table (Table 22.16) shows how the value of the flip-flop changes in response to its inputs.

Table 22.16 *The state table of various flip-flops*

RS (reset-set)		
R	S	Q_{next}
0	0	Q
0	1	1
1	0	0
1	1	undefined

D (data)	
D	Q_{next}
0	0
1	1

JK		
J	K	Q_{next}
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

T (toggle)	
T	Q_{next}
0	Q
1	$\overline{Q}$

JK Flip-Flop (FE) (Fig. 22.21)

SR, *FE* is converted to *JK*, *FE* by feeding $\overline{Q}$ to the upper *AND* and Q to lower *AND*. It also takes of illegal inputs of *SR* ($S = R = 1$).

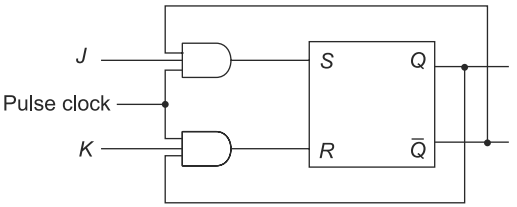


Fig. 22.21 *JK Flip Flop*

As the basic flip-flop is *SR*, we will consult Table 22.16 for each set *SR* to determine the output of the *JK* flip-flop. The values of *S*, *R* are governed by inputs *J*, *K* and *Q* (and so $\bar{Q}$ to the two AND gates). The outputs for various combinations of inputs, (*J*, *K*) when a pulse is applied, i.e. *PT* or *NT* are given below.

- $J = 0, K = 0, Q = 0 \Rightarrow S = 0, R = 0 \Rightarrow Q_{next}$, no change
  $J = 0, K = 0, Q = 1 \Rightarrow S = 0, R = 0 \Rightarrow Q_{next}$, no change
- $J = 0, K = 1, Q = 0 \Rightarrow S = 0, R = 0 \Rightarrow Q_{next} = 0$, no change
  $J = 0, K = 1, Q = 1 \Rightarrow S = 0, R = 1 \Rightarrow Q_{next} = 0$, State resets
- $J = 1, K = 0, Q = 0 \Rightarrow S = 1, R = 0 \Rightarrow Q_{next} = 1$, State sets
  $J = 1, K = 0, Q = 1 \Rightarrow S = 0, R = 0 \Rightarrow Q_{next} = 1$, no change

The above results confirm the first of the truth table of *JK* flip-flop (Table 22.16).

Consider now (1, 1) inputs which were entries not permitted in an *SR* flip-flop.

- $J = 1, K = 1, Q = 0 \Rightarrow S = 1, R = 0 \Rightarrow Q_{next} = 1 = \bar{Q}$, State sets
  $J = 1, K = 1, Q = 1 \Rightarrow S = 0, R = 1 \Rightarrow Q_{next} = 0 = \bar{Q}$, State resets

The above results confirm the *JK* truth table (Table 22.16).

It is also concluded from above that as long as *JK* flip-flop inputs are $J = K = 1$, the state changes from 0 to 1, or 1 to 0, that is it toggles. However, this causes a problem. If any clock pulse is too long, the output state will change more than once and the final state of the flip-flop will be indeterminate. To avoid this problem, a *JK* flip-flop is constructed with two *SR* flip-flops in master-slave connection as in Fig. 22.22.

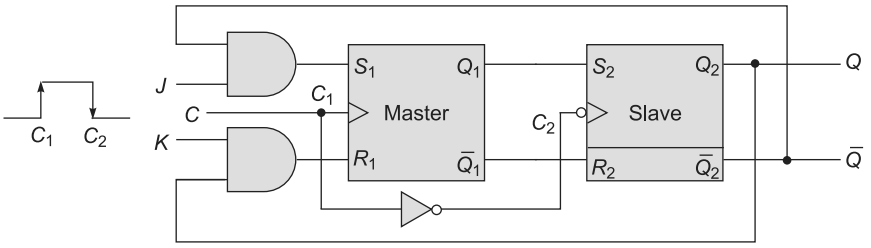


Fig. 22.22 *JK master slave flip-flop*

Operation

By virtue of master to slave connection,

$S_2 = Q_1, R_2 = \bar{Q}_1$

It means that input to the slave is always 0/1 or 1/0. Therefore, as pulse *C* goes low, $C_2 = 1$ and the slave transfers the output of the master to the system output $Q = Q_2 = Q_1$.

When $C_1 = 1$, the master produces output Q_1 as per the *JK* action so long as $J = K \neq 1$. Consider one case.

$$J = 1, K_1 = 0, Q = 0 \Rightarrow S_1 = 1, R_1 = 0, \xrightarrow{C = C_1 = 1} \cdot Q_1 = 1 = S_2, \xrightarrow{C = 0, C_2 = 1} Q_2 = Q = 1$$

This agrees with the *JK* truth table 22.16. The *JK* action occurs for all input combinations other than $J = K = 1$.

For $J = K = 1$, toggling should happen at output without any indeterminate solution.

$$J = 1, K = 1, Q = 1 \Rightarrow S_1 = 0, R_1 = 1 \xrightarrow{C = C_1 = 1} Q_1 = 0 \Rightarrow S_2 = 0\ , R_2 = 1 \xrightarrow{C = 0, C_2 = 1} Q = 0 = \bar{Q}$$

$$J = 1, K = 1, Q = 0 \Rightarrow S_1 = 1, R_1 = 0 \xrightarrow{C = C_1 = 1} Q_1 = 1 \Rightarrow S_2 = 1\ , R_2 = 0 \xrightarrow{C = 0, C_2 = 1} Q = 1 = \bar{Q}$$

Thus confirms the toggle operation of the *JK* master-slave flip-flop. It is to be noted that the master flip-flop operates when $C = 1$ whereas the slave operation flows when pulse goes low, i.e. $C = 0$. When the slave operation occurs, the master is inoperative and so unwanted toggling cannot occur, which was the case in *JK* flip-flop of Fig. 22.19. Because of this sequential action of slave (after master has become inoperative) after *C* goes low, the *JK* master-slave flip-flop is also referred to as *trailing edge triggered flip-flop*.

A *D* flip-flop action is achieved by a *JK* flip-flop by connecting to *K* through a NOT gate as in Fig. 22.23(a). The input (1/0) is reproduced at the output (1/0).

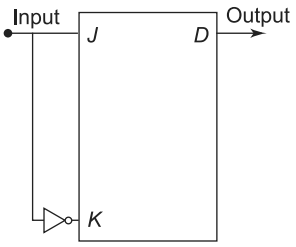


Fig. 22.23(a) *D flip-flop*

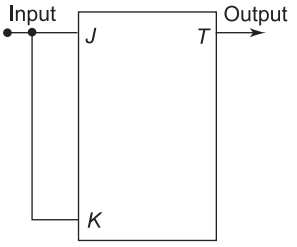


Fig. 22.23(b) *T flip-flop*

The reader may check from the *JK* truth table.

A *T* flip-flop function is obtained from a *JK* flip-flop by connecting *J* to *K* and input at *J* as in Fig. 22.23(b). The reader may check against *JK* truth table.

22.6.1 Shift Register

For example, consider the following circuit shown in Fig. 22.24 containing two *RS* flip-flops. When a clock pulse occurs, the value of the left flip-flop is copied to the right flip-flop. This circuit is known as a *shift register*.

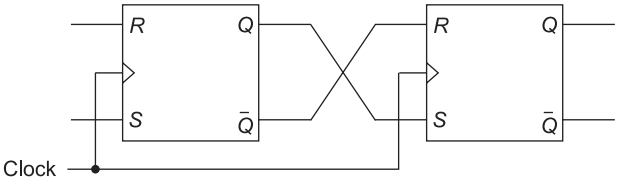


Fig. 22.24 *Shift (right) register*

Flip-flops are used within a CPU to implement registers. A register is an ordered group of *n* flip-flops. For example, in the Intel architecture, EAX is a 32-bit register. It can hold a 32-bit binary integer.

The working principle of a shift register has already been introduced in Fig. 22.19 using *SR* flip-flop. In Fig. 22.25, we present a four-bit shift register employing *D* has flip-flops, which trailing edge triggered indicated by a small circle at the back of the clock triangle.

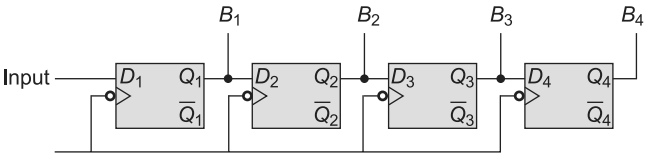


Fig. 22.25 *Shift register*

Let the input sequence be A_1, A_2, A_3, A_4 and the initial state of the register be $Q_1 = Q_2 = Q_3 = Q_4 = 0$. Before the first pulse arrives, the four data (D) bits are $D_1 = A_1$, $D_2 = Q_1 = 0$, $D_3 = Q_2 = 0$. And $D_4 = Q_3 = 0$. After the first pulse arrives, date (D) in all the flip-flops shifts to Qs and the state of the regular read from left to rights becomes A_1, 000. After the second pulse, the state of the register becomes A_2, A_1 00 and finally at the end of fourth pulse it is A_4, A_3, A_2, A_1. The register state can be read simultaneously at B_1 B_2 B_3 B_4. The register is named *serial-in, parallel-out* shift register.

By putting in four more pulses, the output can be read serially at B_4.

22.6.2 Binary Counter

A counter is a sequential circuit that counts the number of input pulses. A counter that counts in terms of binary is called a binary counter. The count output of an *n*-bit binary counter is 2^n states. Therefore, it can count from 0 to $(2^n - 1)$. The number of states of a counter is referred to as it modulus (m). For an *n*-bit counter, $m \leq 2^n$.

Depending on the manner in which flip-flops are triggered to count, there are two types of counters.

- Asynchronous counter
- Synchronous counter

In case of an asynchronous counter, the flip-flops are clocked sequentially, while in a synchronous counter, they are clocked simultaneously. Therefore, time delays of each flip-flop get added and their count action is much slower than in synchronous counters.

Asynchronous Counters (Ripple Counters)

T-flip-flops are used in these counters. A 3-bit binary ripple counter is shown in Fig. 22.26. The small circles at the back of the clock input stand for the fact that these are triggered by the trailing edge of the input pulse (1 going 0). For toggling, all *T* inputs are kept high (1). From left to right, the first *T* flip-flop receives pulses from the counter. The other two receive pulses from the output of the preceding *T* flip-flop. The pulses kind of ripple through and hence, the name ripple counter.

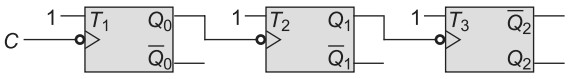


Fig. 22.26 *3-bit (modules 8) ripple counter*

The truth table of a 3-bit ripple counter is presented in Table 22.17.

Table 22.17

Q_2	Q_1	Q_0	*Input pulse count*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	8

At 8th pulse, the counter resets to 0.

The timing diagram of the counter is presented in Fig. 22.27. It is seen that pulse frequency gets divided by 2 at each stage.

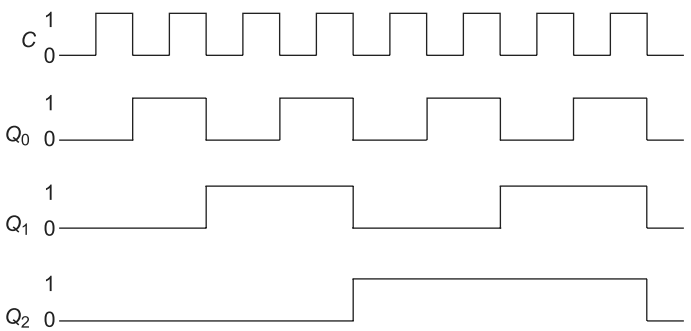


Fig. 22.27 *Timing diagram of a 3-bit ripple counter*

❑ **Modulo-5 Ripple Counter** As $2^3 = 8 > 5$, we need 3 *T* flip-flops. The counter circuit is drawn in Fig. 22.28, where the CLR (clear) terminals are also shown. As the pulse count reaches

$5 \rightarrow 1\ 0\ 1$

The counter must reset to zero (000). As outer 1's combination is unique to count 5, these are fed to a NAND gate, which produces 0 output to clear the three flip-flops. The counter is now ready for 0 recount.

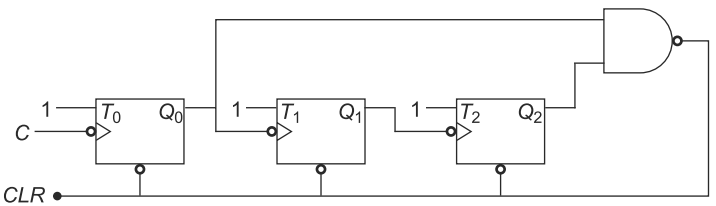


Fig. 22.28 *Modulo 5-ripple counter*

Synchronous Counter

In an asynchronous counter, as the pulse ripples through all the flip-flops, their time delay adds up. In synchronous counters, the clock pulse is applied to all the flip-flops simultaneously and so the time delay is that of one counter. Therefore, these are fast in operation.

For a modulo-16 synchronous counter, four-flip-flops are needed. We shall use the T flip-flop.

The truth table for output sequence for Q_3, Q_2, Q_1, Q_0 is listed in Table 22.18. We find from this table that

Q_0 continuously toggles, therefore $T_0 = 1$

Q_1 toggles when $Q_0 = 1$, therefore $T_1 = Q_0$

Q_2 toggles when $Q_0 = Q_1 = 1$, therefore $T_2 = Q_1Q_0$

Q_3 toggles when $Q_0 = Q_1 = Q_2 = 1$, therefore $T_3 = Q_2\, Q_1\, Q_0$.

The corresponding $T = 1$ are indicated in the same table. To generate T_2 and T_3, two AND gates are needed. To meet these requirements, the circuit diagram of the synchronous counter is drawn in Fig. 22.29.

Table 22.18 *Truth table*

Input (Clock)	Q_3	Q_2	Q_1	Q_0	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1	1
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	1	1	1
4	0	1	0	0	0	0	0	1
5	0	1	0	1	0	0	1	1
6	0	1	1	0	0	0	0	1
7	0	1	1	1	1	1	1	1
8	1	0	0	0	0	0	0	1
9	1	0	0	1	0	0	1	1
10	1	0	1	0	0	0	0	1
11	1	0	1	1	0	1	1	1
12	1	1	0	0	0	0	0	1
13	1	1	0	1	0	0	1	1
14	1	1	1	0	0	0	0	1
15	1	1	1	1	1	1	1	1
0	0	0	0	0				

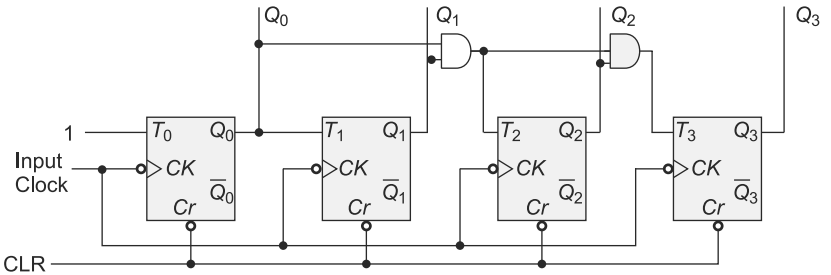


Fig. 22.29 *Modulo-16 synchronous counter*

22.7 GENERAL MODEL OF A SEQUENTIAL CIRCUIT

The circuit shown in Fig. 22.30 gives a general idea of a sequential circuit. During one clock cycle,

1. Flip-flops (may) change state,
2. Changes propagate through combinational logic, and
3. Combinational logic gates and flip-flop inputs become stable.

This cycle repeats indefinitely as long as the clock is running.

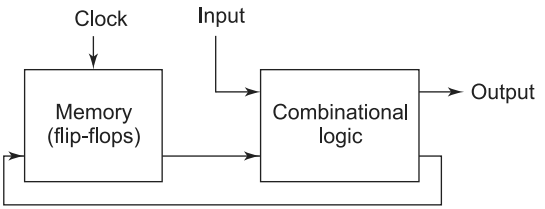


Fig. 22.30 *Model sequential circuit*

Summary

- Number systems have been introduced. Digital and analog systems are compared.
- Digital circuits are classified. Sequential circuits have been introduced and discussed.

Exercises

Review Questions

1. Convert the given decimal numbers to binary:
   (i) $(258)_{10}$ (ii) $(137)_{10}$ (iii) (11.6875
2. Convert the hexadecimal $(8F6)_{16}$ to a decimal number.
3. Multiply $(11011)_2$ with $(101010)_2$.
4. Divide $(8EC2)_{16}$ by $(2F2)_{16}$.

Problems

1. Find the decimal equivalents of the following binary numbers.
   (a) 1111111 (b) 11001.0101
2. Perform the following operations.
   (a) 10101.10101 + 110011 (b) 01110.1001 – 00011.1110
   Use 2's complement method.
3. Subtract in binary form:
   $(47)_{10} - (23)_{10}$
4. Express the following in 8-bit sign magnitude form:
   (a) +123 (b) –56
5. Decode the following into decimal form (H stands for Hexadecimal):
   (a) FCH (b) 9 AH
6. Add the following decimal numbers in 8-bit 2's complement form:
   (a) +45 –56 (b) + 67 –98
7. Find the 8-bit subtraction of the following decimal number in 2's complement form:
   (a) +54, +65 (b) –25, –66
8. Convert the following sign-magnitude numbers into decimal form:
   (a) 1001100110 (b) 100 1100, 01110101
9. Perform the following conversions:
   (a) 279 from decimal to octal number.
   (b) 36.125 from decimal to octal number.
   (c) 11000111.1101 from binary to octal number.
10. Convert the numbers given in Problem 9 to hexadecimal numbers.
11. Perform the indicated operations in binary:
    (a) $(32)_8 + (73)_8$ (b) $(175)_8 - (114)_8$ (c) $(7E)_{16} + (AD)_{16}$ (d) $(BC)_{16} - (F4)_{11}$
12. Encode the decimal numbers 43 and 295 in binary form:
    (a) Binary code (b) BCD code (c) Octal code (d) Hexadecimal code
13. Check the identity by truth table: $\overline{A + B} \pm \overline{A} \cdot \overline{B}$
14. Show that $(A + B) \cdot (A + \overline{B}) = A$
15. Using 2's complement, find
    1110.1001 – 0011.1110
16. Convert 1100 0111, 1101 to octal number.
17. Consider the Boolean expression
    $Y = AB + CD + E$
    Implement it using NAND gates
    Hint: Take complement, apply De Morgan's theorem and take complement again.
18. Design a circuit which can give AND operation of two variables with only a NAND gate.
19. Write the Boolean expression for the given circuit in Fig. 22.31; E = ?

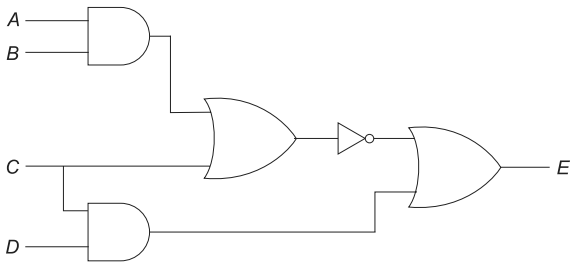


Fig. 22.31

20. For the logic circuit of Fig. 22.32, write the Boolean expression for Y in simple form.

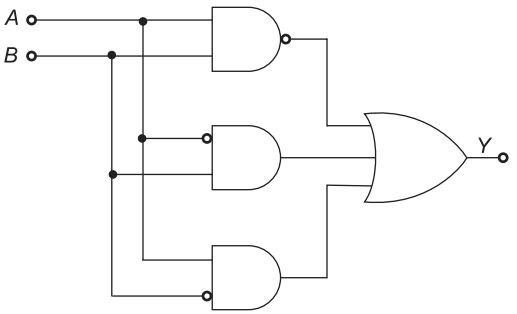


Fig. 22.32

21. Realise the following logic function using NAND gates only:

$Y = \overline{AB + \bar{A}\bar{B}} + \bar{A}B$

Hint: Use De Morgan's theorem.

22. Probe the following identities:
    (a) $A + \bar{A}B = B$
    (b) $(A + B)(\bar{A} + C) = AC + \bar{A}B$
    (c) $(A + C)(A + D)(B + C)(B + D) = AB + CD$
23. Draw the logic circuit for
    $Y = A\bar{B}C + ABC$
    And then simplify and draw the simplified circuit.
24. Simplify the Boolean equation and then draw its logic circuit with appropriate gates.
    $Y = (\bar{A} + B + C)(A + B + \bar{C})$
25. Write the truth table for the given circuit:

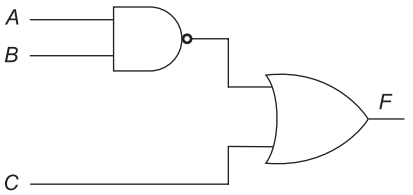


Fig. 22.33

26. Draw the output waveform for the following waveform input to the *SR* flip-flop.

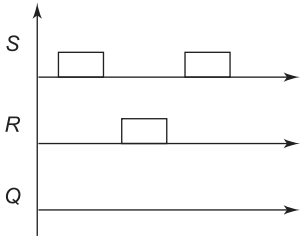


Fig. 22.34

27. Implement the 4:1 multiplexer using basic gates.

28. In the sequential circuit of Fig. 22.15, the NOR gates are replaced by NAND gates. Check that its operation agrees with the *SR* flip-flop truth table (Table 22.15).
Hint: In the NAND gate, the output is 0 only if both inputs are 1.
29. In an *SR* flip-flop (Fig. 22.19), *S* is connected to *R* through NOT gate and input (1/0) is given to *S*. Using the truth table 22.15, show that it acts as a *D*-flip-flop. Identify the output terminal.
30. A 1-to-4 de-multiplexer with one input, two selection lines and four outputs is given in Fig. 22.35.
Find the outputs (D_1 to D_4) for all possible combinations of selector inputs Present it in the form of a truth table. What conclusion can you draw?
31. For the de-multiplexer of Fig. 22.35, '*E*' is held at 1. Prepare a truth table linking *AB* to output. Is it a decoder. If $E = 0$, what would be the outputs? Are these dependent on *A*, *B*?
32. For the logic circuit of Fig. 22.36, prepare the truth table for various combinations (except $R = S = 1$) linking to Q_n and Q_{n+1}.
33. For the multiplexer of Fig. 22.37, prepare the truth table for *AB* and F. Write the logic expression for F for input (0, 1).
Hint: $F = \overline{A}$, $BI_2 = \overline{A}B\overline{C}$

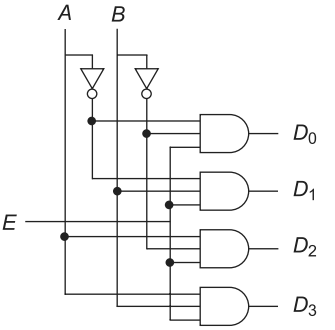


Fig. 22.35

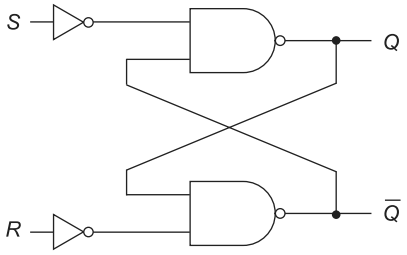


Fig. 22.36

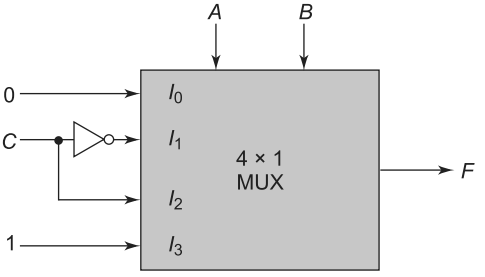


Fig. 22.37

For all possible inputs, all outputs are connected by OR. Thus, $Y = \overline{A}\overline{B}I_0 + \overline{A}BI_1 + A\overline{B}I_2 + A\overline{B}I_3$ or $Y = \overline{A}B\overline{C} - A\overline{B}C + AB$

Multiple-Choice Questions

1. Binary representation of the decimal number 25 is
(a) 10001 (b) 11001 (c) 11101 (d) 10110
2. 2's complement representation is obtained by
(a) complementary the binary representation two times
(b) subtracting 1 from the 1's complement representation
(c) adding 1 to the 1's complement representation
(d) none of the above
3. According to De Morgan's theorem,
(a) $\overline{A+B} = \overline{A}\cdot\overline{B}$ (b) $\overline{A+B} = \overline{A}+\overline{B}$ (c) $\overline{A\cdot B} = \overline{A}\cdot\overline{B}$ (d) $\overline{A+B} = A+B$
4. In a combinational circuit the output
(a) depends upon the past output
(b) depends upon the present input and past output
(c) depends upon the combination of present input only
(d) does not depend upon any present or past input

5. A multiplexer is
   (a) one-to-many converter (b) many-to-one converter
   (c) a sequential circuit (d) all of these
6. The race-around condition is avoided by using
   (a) *JK* flip-flop (b) *D* flip-flop
   (c) *SR* flip-flop (d) master-slave *JK* flip-flop
7. Asynchronous counters are also known as
   (a) ring counters (b) Johnson counters (c) BCD counters (d) ripple counters
8. The sequential circuits are circuits whose output depends upon
   (a) the present combination of input and past output (b) on past output only
   (c) on present input only (d) none of the above
9. ABCD counter is
   (a) Mod-10 counter (b) a combinational circuit
   (c) Mod-12 counter (d) all of these
10. In toggling,
   (a) the output remains same (b) the state changes occur
   (c) the output is invalid (d) none of the above

Answers

Problems

1. (a) $(127)_{10}$ (b) $(25375)_{10}$
2. (a) 111100.00001 (b) $(10.6875)_{10}$
3. 00011000
5. (a) $15 \times 16^1 + 12 \times (16)^0 = 245$, (b) $9 \times 16^1 + 10 \times 16^0 = 156$
9. (a) $(427)_8$ (b) $(44.1)_8$ (c) (307.64)
10. (a) $(117)_{16}$ (b) $(24.2)_{16}$ (c) $(C7.D)_{16}$
11. (a) 1010.101 (b) 00011000 (c) 10010101 (d) $-(38)_{16}$
12. (a) 00101011 (b) 010.10, 0011 (c) 53 (d) 2B
13. (a) 00000001001001111
    (b) 01001001.0101 (c) $1.447)_8$ (d) $(127)_{16}$
17. $(307.64)_8$ 21. $\overline{AB}$
33. *SR* flip-flop

Multiple-Choice Questions

1. (b) 2. (c) 3. (b) 4. (c) 5. (b) 6. (d) 7. (d) 8. (a) 9. (a) 10. (b)

Boolean Algebra and Combinational Circuits

chapter 23

Goals & Objectives

- Explanation of Boolean algebra
- Presentation of combinational circuits
- Discussion of binary functions

23.1 INTRODUCTION

Basic logic gates, their associated Boolean algebra, etc. were the subject matter of Chapter 22. The combination of logic gates to perform a certain logic function is known as a *combinational circuit*. The desired logic may be specified in the form of a truth table from which various Boolean logic functions can be written down and converted to reduced forms needing the least number of gates or even specified gates (say NAND gates only) for their implementation. All these techniques and also the specified binary functions like addition, subtraction will be taken up in the chapter.

In order to prepare the reader for the above task, the chapter begins by discussing binary and other number systems employed in digital systems. Further details of Boolean algebra, basic theorems and function reduction techniques will then be exposed to the reader.

Memory cells (flip-flops) which can also be constructed from basic gates and the sequential circuits, which employ memory cells, will be the subject matter of the next chapter.

23.2 BINARY NUMBER SYSTEM

All of us are familiar with the decimal number system in which the symbols 0 through 9, known as *digits*, are used to specify any number. For example, the number 496.27 is nothing but

$$400 + 90 + 6 + 2/10 + 7/100$$

or

$$4 \times 10^2 + 9 \times 10^1 + 6 \times 10^0 + 6 \times 10^{-1} + 7 \times 10^{-2}$$

The *base* of this number system is 10 and each position to the left or right of the decimal point corresponds to a power of 10.

When we speak of digital systems like computers, microprocessors, etc. it is the binary number system, which is employed. The word *binary* means two. As mentioned in the previous chapter, a digital system consists of only two distinct logic levels, 0 and 1. These are the two digits in the binary number system. Each digit is called a bit. Thus, binary numbers are merely strings of 0s and 1s. A string or sequence of 4 bits is called a *nibble*, an 8-bit sequence is a *byte* and a 16-bit sequence is a *word*. The binary number system, like decimal number system assigns a specific weight in n of 2. For example, the binary number 11011.101 can be written as

$$1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3}$$

Here, the *base* is 2 and each digit corresponds to a power of 2.

23.2.1 Number Conversion

Binary-to-decimal Conversion

To convert a binary number to its decimal equivalent, add the decimal equivalent of each position occupied by a 1.

For example,

$$\begin{aligned}(111001)_2 &= 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 \\ &= 2^5 + 2^4 + 2^3 + 0 + 0 + 1 \\ &= 32 + 16 + 8 + 1 = (57)_{10}\end{aligned}$$

$$\begin{aligned}(101.01)_2 &= 2^2 + 0 + 2^0 + 0 + 2^{-2} \\ &= 4 + 1 + 0.25 = (5.25)_{10}\end{aligned}$$

The subscripts 2 and 10 respectively identify the base of binary and decimal number systems.

Decimal-to-binary Conversion

A decimal number can be converted to its equivalent binary form by the inverse process, i.e. by expressing the decimal number as the sum of powers of 2. The *double-dabble* is a very popular method for decimal-to-binary conversion, in which the integers and the decimals are handled separately. It can be summarised as follows:

- To convert a decimal number to its binary equivalent, progressively divide the decimal number by 2, noting the remainders; the remainders taken in reverse order form the binary equivalent.
- To convert a decimal fraction to its binary equivalent, progressively multiply the fraction by 2, removing and noting the carries; the carries taken in forward order form the binary equivalent.

The double-dabble procedure is illustrated below:

Example 23.1

Convert the decimal number 25.375 to its binary equivalent.

Solution Using double-dabble method on the integer part,

2	25	
2	12	1 ↑
2	6	0 | remainders—read up
2	3	0
	1	1 ↓

Therefore, the binary equivalent of 25 is 11001. Now consider the fraction,

$0.375 \times 2 = 0.75$	0
$0.75 \times 2 = 1.5$	1
$0.5 \times 2 = 1.0$	1
$0.0 \times 2 = 0$	0

carries—read down

The binary equivalent of 0.375 is 0110 = 011. Therefore, the binary equivalent of 23.375 is 11001.011.

23.2.2 Binary Arithmetic

We are all familiar with the arithmetic operations like addition, subtraction, multiplication and division using decimal numbers. Such operations can be performed on binary numbers also and in fact, binary arithmetic is much simpler than decimal arithmetic, because here only two digits 0 and 1 are involved. We shall first take up the rules of binary addition before discussing other operations.

Binary Addition

The rules for binary addition are

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

$$1 + 1 + 1 = 1 + 10 = 11$$

It is important to note that the sign "+" used here corresponds to arithmetic addition and not logical operation.

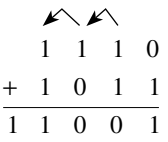
For large numbers, we add column by column, carrying where necessary into higher position columns.

Example 23.2

Add the binary numbers: (a) 1110 and 1011 (b) 1111 and 0101

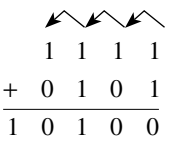
Solution

(a)



$$\begin{array}{r} \overset{\curvearrowleft}{1}\ \overset{\curvearrowleft}{1}\ 1\ 0 \\ +\ 1\ 0\ 1\ 1 \\ \hline 1\ 1\ 0\ 0\ 1 \end{array}$$

(b)



$$\begin{array}{r} \overset{\curvearrowleft}{1}\ \overset{\curvearrowleft}{1}\ \overset{\curvearrowleft}{1}\ \overset{\curvearrowleft}{1} \\ +\ 0\ 1\ 0\ 1 \\ \hline 1\ 0\ 1\ 0\ 0 \end{array}$$

Arrows indicate carry operation.

Binary Subtraction

The rules of binary subtraction are

$$0 - 0 = 0$$

$$1 - 0 = 1$$

$$1 - 1 = 0$$

$$10 - 1 = 1$$

In subtraction, we subtract column by column, borrowing wherever necessary from higher position columns. In subtracting a large number from a smaller one, we can subtract the smaller from the larger and change the sign just as we do with decimals.

Example 23.3

Subtract (a) 10 from 28, and (b) 11 from 6 using binary arithmetic.

Solution

(a)

$$\begin{array}{r} 28 \\ -10 \\ \hline 18 \end{array} \qquad \begin{array}{r} 1\ 1\ 1\ 0\ 0 \\ -0\ 1\ 0\ 1\ 0 \\ \hline 1\ 0\ 0\ 1\ 0 \end{array}$$

(b)

6	0 1 1 0
−11	−1 0 1 1
−5	−0 1 0 1

Here, we subtract 6 from 11 and simply add a '–' sign to it.

23.2.3 Signed Numbers

In the decimal number system, we use '+' sign for denoting positive numbers and '–' sign for denoting negative numbers. (The absence of any sign indicates that the number is positive). As these signs are not available in the binary system, we shall see below how signs are attached to numbers.

There are three binary signed number systems. These are

1. Sign-magnitude representation
2. One's complement representation
3. Two's complement representation

Sign Magnitude

In sign-magnitude representation, the most significant bit (MSB) is used to represent the sign (0 for positive and 1 for negative) and the remaining bits are used to represent the magnitude of the number. For example, the binary 6-bit number 011010 represents a positive number and its value is 26, whereas 111010 represents a negative number written as –26. In general, the maximum positive number that can be represented using sign-magnitude form is $+(2^{n-1}-1)$ and the maximum negative number that can be represented is $-(2^{n-1}-1)$, where n is the number of bits.

Unsigned n-bit numbers are 2^n

$$\text{Ratio}\left(\frac{\text{Signed}}{\text{Unsigned}}\right)\text{numbers} = \frac{2^{n-1}-1}{2^n} \approx \frac{1}{2}$$

It is seen that signed numbers are nearly ½ of unsigned numbers. Therefore, signed numbers should be used only when necessary.

For instance, the consider 8-bit number.

Unsigned range

00000000 → 0
11111111 → 255

Signed range

These reduce from 255 to 127.

Negative numbers

10000001 → –1
11111111 → –127

Positive numbers

00000001 → +1
01111111 → +127

One's Complement Notation

In a binary number, if we replace each 0 by 1 and each 1 by 0, we obtain another binary number, which is the one's complement of the first binary number. In fact, both the numbers are complements of each other. For example, while $(0111)_2$ represents $(+7)_{10}$, $(1000)_2$ represents (–7). Here again, we note that the MSB

denotes the sign of the number (0 for positive and 1 for negative). But, the magnitude of a negative number is obtained by taking the one's complement of the number. Thus, the maximum positive and negative numbers, that can be represented are = $(2^{n-1} - 1)$ and $-(2^{n-1} - 1)$ respectively. The major disadvantage here is that the number zero has two different representations, 0000 = + 0 and 1111 = – 0.

Two's Complement Notation

By adding a 1 to the one's complement of a binary number, we get the two's complement of that binary number. This can also be used for representing negative numbers. For example, 0101 represents + 5, whereas its 2's complement 1011 (1's complement +1) represents –5. In this representation also, if the MSB is 0, the number is positive. Whereas if the MSB is 1, the number is negative and its magnitude is obtained after taking its 2's complement. Here, for an n-bit number, the maximum positive number that can be represented is + $(2^{n-1} - 1)$ and the maximum negative number that can be represented is $-(2^{n-1})$. The reader may verify this by considering a 4-bit number.

Binary Subtraction using Two's Complement

Two's complement representation is usually preferred over other representations because of the ease in binary subtraction using two's complement. It is based on the fact that adding the 2's complement of a number is equivalent to subtracting the number. For example, in evaluating ($A - B$) (A and B are binary numbers of course), we subtract B from A, adding the 2's complement of B to A. If a final carry is generated, it is discarded and the answer is given by the remaining bits, which is positive (A is greater than B). If the final carry is 0, the answer is negative (B is greater than A) and is in the 2's complement form.

Example 23.4

(a) Represent $(-17)_{10}$ and $(-22)_{10}$ in 8-bit 2's complement notation.

(b) Perform (22 − 17) and (17 − 22) directly by 2's complement notation.

Solution

(a) By adding 1 to the one's complement, we get

$-17 \rightarrow -10001 \rightarrow -00010001 \rightarrow 11101110 + 1$
$\rightarrow 11101111$

$-22 \rightarrow -10110 \rightarrow -00010110 \rightarrow 11101001 + 1$
$\rightarrow 11101010$

Thus, 11101111 is the 2's complement representation of –17 in 8 bits. Similarly, 11101010 is the 2's complement representation of – 22. One important thing that can be observed is that the 2's complement is same as the number itself except that while scanning from LSB to MSB, we find that after the occurrence of the first 1, all the bits have been complemented. Based on the above observation, we can use the following rule for finding the 2's complement of a binary number: Scan the number from LSB to MSB and write the bits as they are up to and including the occurrence of the first 1 and complement all other bits.

(b) (i) 22 = 00010110
17 = 00010001
2's complement of 17 = 11101111

22	00010110	
–17	11101111	
+5	100000101	$\rightarrow (+5)_{10}$
Discard 1	↑	

MSB is 0. Therefore, the answer is positive.

(ii) 2's complement of 22 = 11101010

17	00010001
–22	11101010
–5	11111011

No carry.

MSB is 1. Therefore, the answer is negative and is in 2's complement form. Two's complement of 11111011 = 00000101 = $(5)_{10}$. Therefore, the answer is –5 in decimal representation.

Outflow

In 8-bit (or in general *n*-bit) arithmetic, it must the ensured that the result does not go beyond the range of numbers, i.e. it should be within the range of –127 to +127. If it exceeds this range, an outflow will occur into the sign bit, thereby changing it to incorrect sign. Two cases are illustrated below.

❑ **Case I** Let us add + 100 and + 50; the answer should be +150.

100	0110	0100
+ 50	+0011	0010
+150	1001	0110

It is seen that sign bit has changed from 0 to 1, which means that the sum is negative.

❑ **Case II** Let us add two negative numbers.

–85	1010	1011	
+(–97)	+1001	1111	
	1 0100	1010	→ 0100 1010

carry ignore ↑ ↑ positive sign

The sum has a positive sign but it should be negative.

Binary Multiplication

Binary multiplication is similar to decimal multiplication. In binary multiplication, say $A \times B$, each partial product is either 0 or A itself (i.e. the multiplicand) as the multiplication is either by 0 or by 1 respectively. An example of binary multiplication is given below.

Example 23.5

Multiply 1101 by 1010.

Solution

1101	Multiplicand
×1010	
0000	Partial products
1101	
0000	
1101	
10000010	Product

Binary Division

Binary division is again performed in a way very similar to decimal division. An example of binary division is given below.

Example 23.6

Divide 1011011 by 111.

Solution

$$111\overline{)1011011}\ 1101 \leftarrow \textit{Ans.}$$

$$\begin{array}{r} 0111 \\ \hline 1000 \\ 0111 \\ \hline 000111 \\ 111 \\ \hline 0 \end{array}$$

23.3 OCTAL NUMBER SYSTEM

Another popular number system is the octal number system. There are $8(2^3)$ combinations of 3-bit binary numbers. Therefore, sets of 3-bit binary numbers can be conveniently represented by octal numbers with base 8. These numbers are 0, 1, 2, 3, 4, 5, 6 and 7. This also is a positional number system and has two parts, integer and fractional. For example, $(1062 \cdot 403)_8$ is an octal number and can be written as

$$(1062 \cdot 403)_8 = 1 \times 8^3 + 0 \times 8^2 + 6 \times 8^1 + 2 \times 8^0 + 4 \times 8^{-1} + 0 \times 8^{-2} + 3 \times 8^{-3}$$

$$= 512 + 482 + 4/8 + 3/512$$

$$= (562 \cdot 50586)_{10}$$

The above procedure gives the decimal equivalent of an octal number.

Example 23.7

Convert $(294 \cdot 6875)_{10}$ into octal.

Solution First, consider the integer part.

$$\begin{array}{rrl} 8 \mid 294 & & \\ 8 \mid 36 & 6 & \uparrow \\ 8 \mid 4 & 4 & \text{remainders—read up} \\ 0 & 4 & \downarrow \end{array}$$

Therefore, $(294)_{10} = (446)_8$

Now, coming to the fraction

$$\begin{array}{lll} 0.6875 \times 8 = 5.50 & 5 & \downarrow \\ 0.5000 \times 8 = 4.00 & 4 & \text{carries—read down} \end{array}$$

Therefore, $(0.6875)_{10} = 1054)_8$

From the above, it follows that $(294 \cdot 6875)_{10} = (446 \cdot 54)_8$

Octal-to-Binary and Binary-to-Octal Conversion

Octal numbers can be converted to equivalent binary numbers by replacing each digit by its 3-bit binary equivalent. Table 23.1 gives octal and binary equivalents for decimal numbers 0-7. For example,

$$(642 \cdot 71)_8 = (110100010 \cdot 111001)_2$$

Similarly, binary numbers can be converted into equivalent octal numbers by making groups of 3 bits starting from LSB and moving towards MSB for integer part. For example,

$$(101110011)_2 = 101110011 = (563)_8$$

For fractional parts, we start grouping from the bit next to the binary point and move towards right. For example,

$$(0.101010110)_2 = 0.101010110 = (0.526)_8$$

In forming the 3-bit groupings, sometimes, we may have to add 0's to complete the most significant digit group in the integer part and the least significant digit group in the fractional part.

Table 23.1 *Binary and octal equivalents of decimal numbers*

Decimal	*Binary*	*Octal*
0	000	0
1	001	1
2	010	2
3	011	3
4	100	4
5	101	5
6	110	6
7	111	7

Octal Arithmetic

Octal arithmetic rules are similar to the decimal or binary arithmetic. But in computing system's arithmetic operations, using octal numbers are performed by converting the octal numbers to binary numbers and then by using the rules of binary arithmetic. The result so obtained can be converted again to octal form.

23.4 HEXADECIMAL NUMBER SYSTEM

Hexadecimal numbers are extensively used in association with microprocessors. Hexadecimal means 16. There are 16 combinations of 4-bit binary numbers and sets of 4-bit binary numbers can be entered in the microprocessor in the form of hexadecimal digits. The base (or radix) of a hexadecimal number is 16. This means that it uses 16 symbols to represent all numbers. These are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, *A*, *B*, *C*, *D*, *E*, *F*. Since both numbers as well as alphabets are used to represent the digits in a hexadecimal number system, it is also called the alphanumeric number system.

Table 23.2 shows the equivalences between hexadecimal, binary and decimal digits.

Table 23.2 *Binary and hexadecimal equivalences of decimal numbers*

Decimal	*Binary*	*Hexadecimal*
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	*A*
11	1011	*B*
12	1100	*C*
13	1101	*D*
14	1110	*E*
15	1111	*F*

Since 16 digits are used, the weights are in powers of 16. The decimal equivalent of a hexadecimal string equals the sum of all hexadecimal digits multiplied by their weights. For example,

$$(F8E.\,28)_{16} = F \times 16^2 + 8 \times 16^1 + E \times 16^0 + 2 \times 16^{-1} + B \times 16^{-2}$$

$$= 15 \times 16^2 + 8 \times 16^1 + 14 \times 16^0 + 2 \times 16^{-1} + 11 \times 16^{-2}$$

$$= 3840 + 128 + 14 + 2/16 + 11/256$$

$$= (3982.16796875)_{10}$$

Conversion from decimal to hexadecimal is similar to the procedure used in binary and octal conversion except that, here 16 is used in dividing for integer part and multiplying for fractional part.

Example 23.8

Convert the following numbers to their hexadecimal equivalents.

(a) $(49.5)_{10}$ (b) $(972.625)_{10}$

Solution

(a) Integer part

$$\begin{array}{r|l} 16 & 49 \\ 16 & 3 \quad 1 \\ \hline 0 & 3 \end{array}$$

Thus, $(49)_{10} = (13)_{16}$

Fractional part

$$0.5 \times 16 = 8.0$$

Thus, $(0.5)_{10} = (0.8)_{16}$

Therefore, $(49.5)_{10} = (13.8)_{16}$

(b) Integer part

16	972	
16	60	$12 = C$
16	3	$12 = C$
	0	3

Thus, $(972)_{10} = (3CC)_{16}$

Fractional part

$0.625 \times 16 = 10.00$. The integral part is $10 \rightarrow A$.

Thus, $(0.625)_{10} = (0.A)_{16}$

Therefore, $(972.625)_{10} = (3CC.A)_{16}$

23.4.1 Hexadecimal-to-Binary and Binary-to-Hexadecimal Conversions

Hexadecimal numbers can be converted into equivalent binary by replacing each hexadecimal digit by its equivalent 4-bit binary number. For example,

$$(20E.CA)_{16} = (0010\ 0000\ 1110.1100\ 1010)_2$$
$$= (001000001110.11001010)_2$$

Similarly, binary numbers can be converted into hexadecimal numbers by making groups of four bits starting from LSB and moving towards MSB, for integers, and then replacing each group of four bits by its hexadecimal equivalents. Sometimes, in forming 4-bit groupings, 0's may be required to complete the most significant digit group in the integer part. For example,

$$(10100110111110)_2 = (0010\ 1001\ 1011\ 1110)_2$$
$$= (29BE)_{16}$$

For the fractional part, the above procedure is repeated starting from the bit next to the hexadecimal point and moving towards the right. Here again, in forming 4-bit groupings, 0's may be required to complete the least significant digit group. For example,

$$(0.00111110111101)_2 = (0.0011\ 1110\ 1111\ 0100)_2$$
$$= (0.3EF4)_{16}$$

23.4.2 Hexadecimal Arithmetic

The rules for hexadecimal arithmetic operations are similar to the rules for decimal, binary and octal systems. Since information can be handled only in binary form by a digital circuit, hexadecimal numbers are first converted into binary numbers and arithmetic operations are performed using rules for binary arithmetic.

23.5 CODES

Computers and other digital systems are required to handle data, which may be numeric, alphabets or special characters. Since digital circuits work only with binary digits; therefore, the numerals, alphabets and other special characters are to be converted into binary format. There are several ways of achieving this, and this particular process is called *encoding*. Numerous codes are in existence and different codes serve different purposes. At this stage, it is important to realise that a series of 1's and 0's in a digital system may sometimes represent a binary number and at other times represent some other discrete information like alphabets, etc. as specified by a given binary code. Some commonly used binary codes are given in Table 23.3.

Table 23.3 *Binary codes*

Decimal number	*Binary*	*BCD*
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	0101
6	0110	0110
7	0111	0111
8	1000	1000
9	1001	1001
10	1010	
11	1011	
12	1100	
13	1101	
14	1110	
15	1111	

Binary Code

This is obtained by converting decimal numbers to their binary equivalents. The CPUs of computers process only binary numbers.

BCD Code

This is a binary code in which decimal digits 0 through 9 are represented by their binary equivalents using four bits. As the weights in the BCD code are 8, 4, 2, 1, it is also known as 8421 code. For instance, the decimal 257 converts to BCD as follows:

2	5	7
↓	↓	↓
0010	0101	0111

Therefore, 0010 0101 0111 is the BCD equivalent of $(257)_{10}$. The reverse conversion is similar. For instance,

1001 1000 0110 = $(986)_{10}$

BCD numbers are very useful for input and output operations in digital circuits. They are used to represent decimal digits in systems like digital calculators, digital voltmeters, digital clocks, electronic counters, etc.

The ASCII Code

To get information into and out of a computer, we need to use some kind of *alphanumeric* code (one for letters, numbers and other symbols). At one time, manufacturers used their own alphanumeric codes, which led to all kinds of confusion. Eventually, the industry settled on an input-output code known as the *American Standard Code for Information Interchange* (ASCII, pronounced ask'-ee). This code allows manufacturers to standardise computer hardware such as keyboards, printers and video displays.

❑ **Using the Code** The ASCII code is a 7-bit code whose format is

$$X_6X_5X_4X_3X_2X_1X_0$$

Table 23.4 *ASCII Code*

$X_3X_2X_1X_0$	010	011	100	101	1.0	111
0000	SP	0	@	P		p
0001	!	1	A	Q	a	q
0010	"	2	B	R	b	r
0011	#	3	C	S	c	s
0100	$	4	D	T	d	t
0101	%	5	E	U	e	u
0110	&	6	F	V	f	v
0111	‘	7	G	W	g	w
1000	(	8	H	X	h	x
1001	)	9	I	Y	i	y
1010	*	:	J	Z	j	z
1011	+	;	K	-	k	
1100	,	<	L	-	l	
1101	–	=	M	-	m	
1110	*	>	N	-	n	
1111	/	?	O	-	o	

where each X is a 0 or a 1. Use Table 23.4 to find the ASCII code for the uppercase and lowercase letters of the alphabet and some of the most commonly used symbols. For example, the table shows that the capital letter A has an $X_6X_5X_4$ of 100 and an $X_3X_2X_1X_0$ of 0001. The ASCII code for A is, therefore,

1000001

For easier reading, we can leave a space as follows:

100 0001 (A)

The letter 'a' is coded as

110 0001 (a)

23.6 BOOLEAN RELATIONS

As mentioned earlier, George Boole invented two-state algebra to solve logic problems. Today, Boolean algebra is the backbone of computer circuit analysis and design.

In other words, it may be stated that to obtain the inverse of any Boolean function, invert all variables and replace all OR's by AND's and vice versa.

Table 23.5 *Truth table to prove De Morgan's theorems*

A	B	$\overline{A}$	$\overline{B}$	$\overline{A \cdot B}$	$\overline{A} + \overline{B}$	$\overline{A + B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1	1	1
0	1	1	0	1	1	0	0
1	0	0	1	1	1	0	0
1	1	0	0	0	0	0	0

Table 23.6 *Some identities of Boolean algebra*

Name	*AND form*	*OR form*
Identity law	$1 \cdot A = A$	$0 + A = A$
Null law	$0 \cdot A = 0$	$1 + A = 1$
Idempotent law	$A \cdot A = A$	$A + A = A$
Inverse law	$A \cdot \overline{A} = 0$	$A + \overline{A} = 1$
Commutative law	$A.B = BA$	$A + B + B + A$
Associative law	$(A \cdot B) \cdot C = A \cdot (B \cdot C)$	$(A + B) + C = A + (B + C)$
Distributive law	$A + BC = (A + B)(A + C)$	$A(B + C) = AB + AC$
Absorption law	$A(A + B) = A$	$A + AB = A$
De Morgan's law	$\overline{AB} = \overline{A} + \overline{B}$	$\overline{A+B} = \overline{A}\,\overline{B}$

$Y = A$ AND $B = A \cdot B$

Table 23.7 *Truth table*

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

In AND operation, the output is 1 only if both A and B are 1. Otherwise, it is zero.

OR—Addition symbol +

$Y = A + B$

Table 23.8 *Truth table*

A	*B*	*Y*
0	0	0
6	1	1
1	0	1
1	1	1

23.7 ALGEBRAIC SIMPLIFICATION

Sometimes it is possible to simplify the circuit obtained from the sum-of-products equation. One way to do this is with Boolean algebra. Starting with the sum-of-products equation, try to rearrange and simplify the equation to the extent possible using the Boolean rules of Section 23.6. The simplified Boolean equation means a simpler logic circuit. Thus, hardware for designing the circuit can be minimised.

The following examples clarify this procedure.

Example 23.9

Factorise the following Boolean equations:

(a) $Y = A\bar{B} + AB$

(b) $Y = AB + AC + BD + CD$

(c) $Y = (B + CA)(C + \bar{A}B)$

(d) $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$

Solution

(a) $Y = A\bar{B} + AB$

$= A(\bar{B} + B)$

$= A \cdot 1$

$= A$

(b) $Y = AB + AC + BD + CD$

$= A(B + C) + D(B + C)$

$= (A + D)(B + C)$

(c) $Y = (B + CA)(C + \bar{A}B)$

$= B(C + \bar{A}B) + CA(C + \bar{A}B)$

$= BC + B\bar{A}B + CAC + CA\bar{A}B;\ A\bar{A} = 0,\ BB = B,\ CC = C$

$= BC + \bar{A}B + AC$

(d) $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$

$= \bar{B}\bar{C}(\bar{A}\bar{D} + \bar{A}D + A\bar{D} + AD)$

$= \bar{B}\bar{C}\,[\bar{A}\,(\bar{D} + D) + A(\bar{D} + D)]$

$$= \overline{B}\overline{C}\,[\overline{A} \cdot 1 + A \cdot 1]$$
$$= \overline{B}\overline{C}\,(\overline{A} + A)$$
$$= \overline{B}\overline{C} \cdot 1 = \overline{B}\overline{C}$$

Example 23.10

Compare the AND/OR gate realisation of the Boolean function of Example 23.9(b) and its reduced form.

Solution It is immediately observed from Figs 23.1(a) and (b), that the realisation of the original function needs 5 gates (4 AND's and 1 OR), while the simplified function needs only 3 gates (1 AND and 2 OR's). There is a considerable saving in realisation by carrying out simplification of the original function.

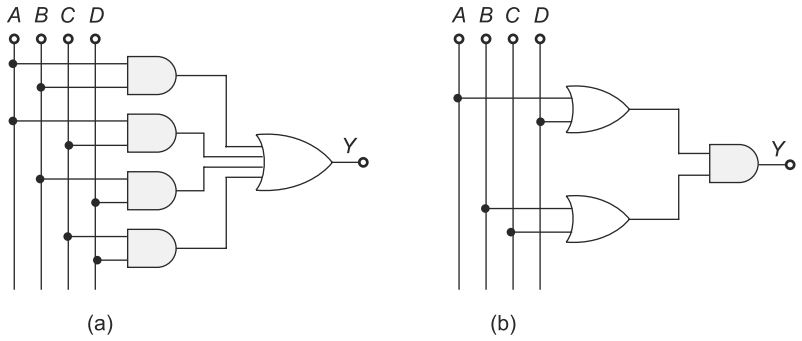


Fig. 23.1 *Logic circuits for expression (b) of Example 23.9*

Example 23.11

Analyse the logic circuit of Fig. 23.2 and show that it can be replaced by a single NAND gate.

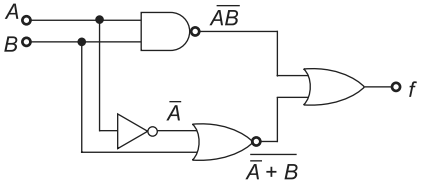


Fig. 23.2 *Logic circuit analysis*

Solution The sub-outputs are noted on the diagram. The simplification of the function is given below:

$$f = \overline{A\overline{B}} + \overline{\overline{A} + B}$$
$$= (\overline{A} + \overline{B}) + A\overline{B} \quad \text{(De Morgan's law)}$$
$$= \overline{A} + \overline{B}\,(1 + A)$$
$$= \overline{A} + \overline{B} \cdot 1$$
$$= \overline{A} + \overline{B}$$
$$= \overline{AB} \quad \text{(De Morgan's law)}$$

Thus, the above circuit is simply equivalent to a NAND gate.

23.8 NAND AND NOR IMPLEMENTATION

It is an attractive preposition to realise combinational circuits using NAND/NOR gates (universal gates; see Section 23.2, as only one type of gates would be needed).

23.8.1 NAND Implementation

NAND gates can be used to realise not only any combinational circuit but even sequential circuits can be constructed with three gates as we shall see in Chapter 27. The realisation of NOT, AND and OR using NAND's already discussed in Section 23.2, is illustrated in Fig. 23.3.

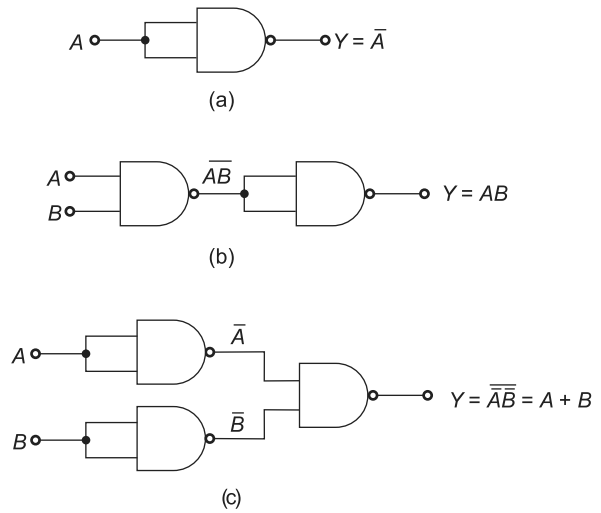


Fig. 23.3 *Realisation of (a) NOT, (b) AND, and (c) OR using NAND gates*

The implementation of a Boolean function with NAND gates requires that the function be simplified in the sum-of-products form. After this, we apply the De Morgan's theorem. For example, consider the function

$$Y = AB + CD + E$$

$$Y = \overline{AB} \cdot \overline{CD} \cdot \bar{E}$$

Therefore,

$$Y = \overline{\bar{A}\bar{B} \cdot \overline{CD} \cdot \bar{E}}$$

This can be implemented in two levels by using only NAND gates as shown in Fig. 23.4.

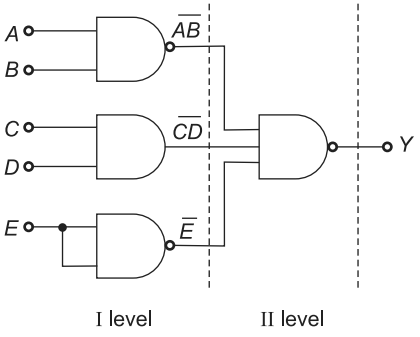


Fig. 23.4 *Realisation of Y = AB + CD + E*

Example 23.12

Given the Boolean function

$$F = (A + \bar{B})(CD + E)$$

Obtain AND-OR implementation and also its implementation using NAND gates only.

Solution We assume that signals corresponding to each literal are available, i.e. the variables are available in complemented as well as in the uncomplemented form.

The realisation of the function using AND and OR gates is shown in Fig. 23.5.

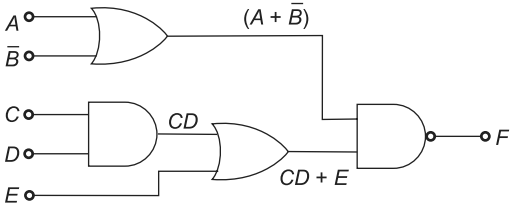


Fig. 23.5 *AND/OR implementation*

Consider again, the function

$$F = (A + \overline{B})(CD + E)$$

We can write

$$A + \overline{B} + \overline{\overline{A} \cdot \overline{B}}$$

And similarly,

$$CD + E = \overline{\overline{C}\,\overline{D} \cdot \overline{E}}$$

Therefore,

$$F = \overline{\overline{A} \cdot \overline{B} \cdot \overline{C}\,\overline{D} \cdot \overline{E}}$$

The NAND realisation of the above equation is shown in Fig. 23.6. The output of the NAND gate 4 is $\overline{F}$. So in order to obtain F, we invert the output of gate 4 by using an inverter NAND gate (5).

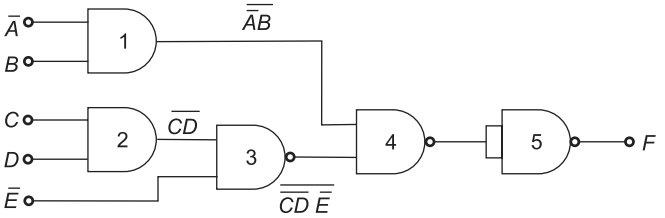


Fig. 23.6 *NAND implementation of Example 23.12*

The given function can also be realised using NAND gates after expressing it in sum-of-products form. Here again, 5 NAND gates are required; interested reader may verify this.

23.8.2 NOR Implementation

The NOR function is the dual of NAND function. Hence, all the procedures and rules for NOR logic are the dual of corresponding procedures and rules of NAND logic.

The implementation of NOT, OR and AND function using NOR gates is shown in Fig. 23.7.

The realisation of any Boolean expression using only NOR gates can be achieved by writing the equation in product-of-sums form, For example, the expression.

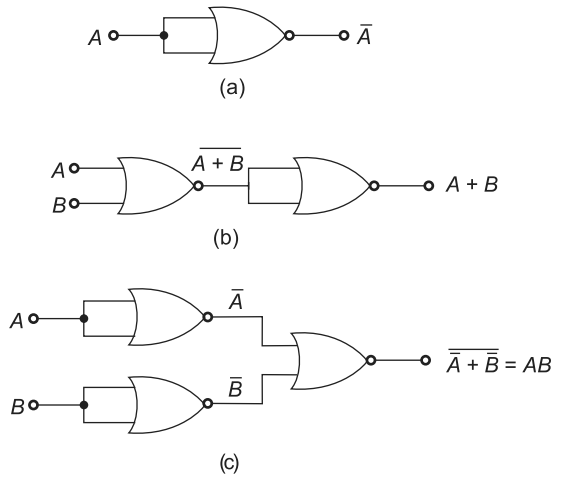


Fig. 23.7 *Implementation of (a) NOT, (b) OR, and (c) AND using NOR gates*

$$Y = (A + B)(C + D)\,(A + \overline{D}) \tag{23.1}$$

is in product-of-sums form. This can be realised using OR-AND gates as shown in Fig. 23.8.

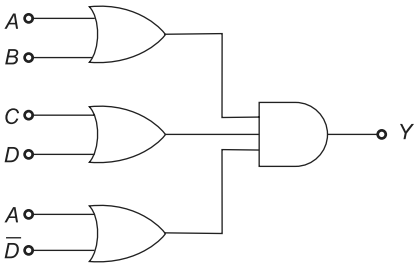


Fig. 23.8 *Realisation using OR-AND gates*

Using De Morgan's theorem, we can write the above equation as

$$\overline{Y} = \overline{(A + B)(C + D)(A + \overline{D})} \tag{23.2}$$

$$= \overline{(A + B)} + \overline{(C + D)} + \overline{(A + \overline{D})}$$

$$= Y_1 + Y_2 + Y_3 \tag{23.3}$$

where $Y_1 = \overline{A + B}$

$Y_2 = \overline{C + D}$

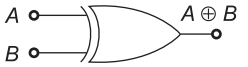
$Y_3 = \overline{A + \overline{D}}$

Therefore,

$$Y = \overline{Y_1 + Y_2 + Y_3} \tag{23.4}$$

XOR Gate

The symbol of XOR gate, its truth table are given in Fig. 23.9(a) and (b). It immediately follows that,



(a)

A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

(b) Truth table

Fig 23.9 *XOR gate*

$$A \oplus B = \overline{A}B + A\overline{B}$$

Half Adder (HA)

This circuit adds two binary variables, yields a carry but does not accept carry from another circuit (adder). The truth table of a half adder is given in Fig. 23.10(a) from which we can write

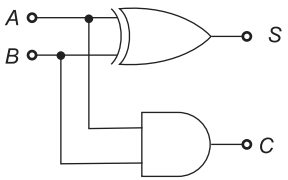
$$S = \overline{A}B + A\overline{B} = A \oplus B$$

$$C = AB$$

The half-adder logic circuit is drawn in Fig. 23.10.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(a) Truth table:
S = Sum; C = Carry



(b) Circuit using XOR

Fig. 23.10 *Half Adder (HA)*

Full Adder

This circuit can add two binary numbers, accept a carry and yield a carry. Such a circuit can easily be visualised by means of two half adders (HA) and an OR as in Fig. 23.11. The reader is advised to check against the truth table.

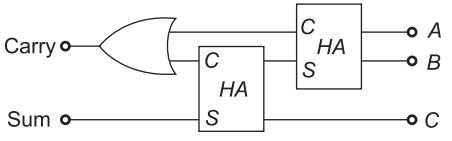


Fig. 23.11 *Full adder using two half adders*

❑ Full Adder Direct Synthesis

Table 23.9 *Full adder truth table*

S = Sum, C_i = Carry in , C_o = Carry out; Inputs are A, B, C

Outputs are S, C_o

Row No.	*A*	*B*	C_i	*S*	C_o
1	0	0	0	0	0
2	0	0	1	1	0
3	0	1	0	1	0
4	0	1	1	0	1
5	1	0	0	1	0
6	1	0	1	0	1
7	1	1	0	0	1
8	1	1	1	1	1

It is observed from the truth table that $C_o = 1$ for rows which have two 1's otherwise it is 0. Its Boolean equation is

$$C_o = AB + BC_i + C_iA$$

It can be implemented by three AND and one OR gates

We further observe that $S = 1$ for rows with one 1 and three 1's,
i.e. odd number of 1's. This is implemented by a three input XOR. Accordingly, the logic diagram is drawn in Fig. 23.12.

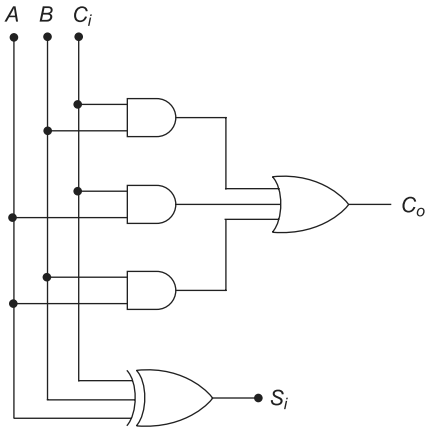


Fig. 23.12 *Full adder*

The reader is advised to verify.

Summary

➢ The principle of boolean algebra and various combinational circuits have been explained.

Exercises

Review Questions

1. Check the identity by truth table: $\overline{A + B} = \overline{A}\,\overline{B}$
2. Show that
   $(A - B) \cdot (A + \overline{B}) = A$
3. Using 2's complement, find
   01110.1001 – 0011.1110
4. Convert 11000111.1101 to octal number.
5. Consider the Boolean expression
   $Y = AB + CD + E$
   Implement it using NAND gates.
   Hint: Take complement, apply De Morgan's theorem and take complement again.

Multiple-Choice Questions

1. The binary equivalent of 24 is
   (a) 11001 (b) 11000 (c) 10110 (d) 10111
2. The total variables used in the hexadecimal system is
   (a) 15 (b) 14 (c) 16 (d) none of these
3. $(AB2)_H$ is represented in binary by
   (a) $(101010110010)_2$ (b) $(010111010110)_2$ (c) $(101011000010)_2$ (d) $(101101101010)_2$
4. According to the De Morgan's theorem,
   (a) $\overline{A \cdot B} = \overline{A} + \overline{B}$ (b) $\overline{A} \cdot \overline{B} = A + B$ (c) $\overline{A + B} = \overline{A} \cdot \overline{B}$ (d) both (a) and (c)
5. Which of the following is not true?
   (a) $a.0 = 0$ (b) $a.1 = 0$ (c) $a + 1 = 9$ (d) $a + 0 = a$
6. A full adder has
   (a) 2 inputs and 2 outputs
   (b) 3 inputs and 2 outputs
   (c) 3 inputs and 3 outputs
   (d) 3 inputs and 1 output
7. The Boolean expression for the circuit of Fig. 23.13 is
   (a) 0 (b) 1
   (c) $xy + z$ (d) $xy + z + z^{-}$

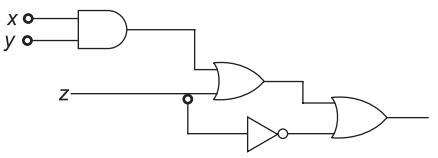


Fig. 23.13

8. According to distributive law,
   (a) $A + BC = (A + B) \cdot (A + C)$
   (b) $A(B + C) = AB + AC$
   (c) $\overline{AB} = \overline{A} + \overline{B}$ (d) both (a) and (b)
9. Which of the following is correct?
   (a) $a.0 = a$ (b) $a + 1 = 1$ (c) $a + \overline{a} = 0$ (d) $a.\overline{a} = 9$
10. A full adder is
    (a) a combinational circuit (b) a sequential circuit
    (c) made up of 2 half-adders (d) all of these

Answers

Multiple-Choice Questions

1. (b) 2. (c) 3. (a) 4. (d) 5. (c) 6. (b) 7. (b)
8. (d) 9. (b) 10. (a)

Flip-Flops

chapter 24

Goals & Objectives

- Introduction to flip-flops and their conversions
- IEEE logic symbols
- Operation of NAND gate latch/NOR gate latch and RS flip-flop
- Functional truth tables of preset and clear (flip-flop) and clocked *D*-flip-flop
- Explanation of edge triggering, edge triggered *RS* flip-flop and *JK* master-slave flip-flop

24.1 INTRODUCTION

A flip-flop is an electronic circuit, which has memory. If its output is 1/0, it remains same unless input changes. On change in input, its output changes (flips) to 0/1 and then remains constant. A flip-flop is a basic element of all sequential systems. A flip-flop is also called a *latch*.

24.2 IEEE LOGIC SYMBOLS

The logic gate symbols you have memorised are the traditional ones recognised by all workers in the electronics industry. These symbols are very useful in that they have distinctive shapes. Manufacturers' data manuals include traditional logic symbols and are recently including the newer *IEEE functional logic symbols*. These newer symbols are in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. These newer IEEE symbols are commonly referred to as "*dependency notation*." For simple gating circuits, the traditional logic symbols are probably preferred, but the IEEE standard symbols have advantages as ICs become more complicated. Most military contracts call for the use of *IEEE standard symbols*.

Figure 24.1 shows the traditional logic symbols and their IEEE counterparts. All IEEE logic symbols are rectangular. There is an identifying character or symbol inside.

24.3 NAND GATE LATCH/NOR GATE LATCH

Two NAND gates are cross connected as shown in Fig. 24.2. Its truth table is given in Fig. 24.2(c). It is verified below.

$\bar{R} = \bar{S} = 1$

Let the prior output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 1 are 1, 0, so its output is $\bar{Q} = 1$ (no change). The inputs to the gate 2 are (1, 1), so its output in $\bar{Q} = 0$. So no change. Some happens if $Q = 0$, $\bar{Q} = 1$. The inputs to gate 1 are (1, 1), so output is $Q = 0$. The inputs to gate 2 are (1, 1), output is $Q = 0$. So no change.

❑ **Note** Replace NAND gate by NOR gate for achieving NOR latch.

$\bar{R} = 1, \bar{S} = 0$

Previous output $Q = 1$, $\bar{Q} = 0$. The gate 1 input is (1, 0) and output is $Q = 1$, $\bar{Q} = 0$, no changes.

Previous output $Q = 0$, $\bar{Q} = 1$, the gate 1 inputs are (0, 1) which cause its output to change to $Q = 1$ and correspondingly output of gate 1 changes to $\bar{Q} = 0$.

Thus, the stable state is $Q(\bar{Q} = 0)$.

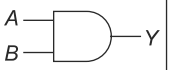
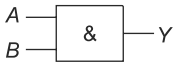
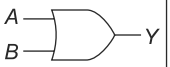
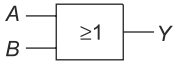
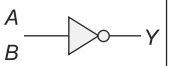
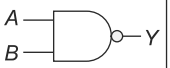
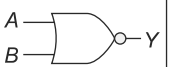
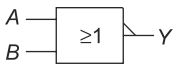
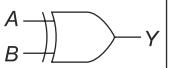
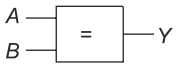
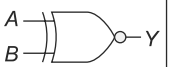
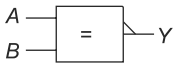
$\bar{R} = 0, \bar{S} = 1$

Stable state is $Q = 0$ ($\bar{Q} = 1$), which is easily verified. If the output is $Q = 1$, it will change to $Q = 0$.

$\bar{R} = 0, \bar{S} = 0$

0 would try to make $Q = 1$, $\bar{Q} = 1$, which is not possible. So there is a conflict.

The symbols of $\bar{S}\bar{R}$ latch are given in Fig. 24.2(b).

Logic Function	Traditional Logic Symbol	IEEE Logic Symbol*
AND		
OR		
NOT		
NAND		
NOR		
XOR		
XNOR		

*ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

Fig. 24.1 *Comparing traditional and IEEE logic gate symbols*

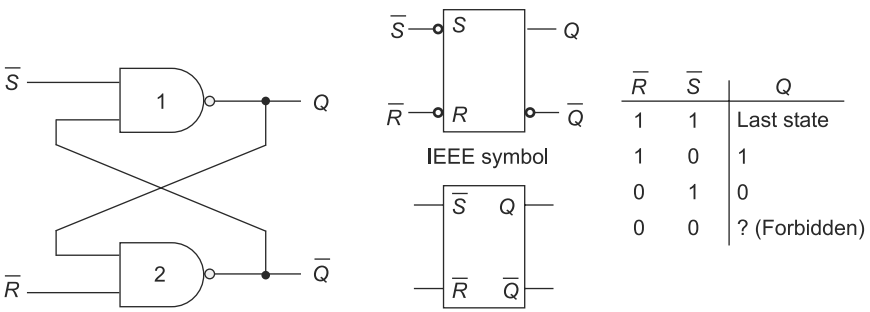


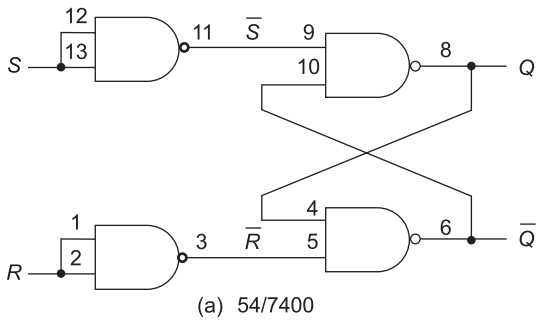
Fig. 24.2 *NAND gate latch*

24.4 *RS* FLIP-FLOP

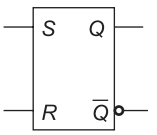
In *RS* flip-flop, we want to

- Set $S = 1 \Rightarrow Q = 1$
- Reset $R = 1 \Rightarrow Q = 0$

It means that we want to reverse the entries of the truth table of Fig. 24.2(c) and $\overline{R} \rightarrow R$, $\overline{S} = S$. This is shown in the truth table of Fig. 24.3(c). This is achieved simply by obtaining $\overline{S}$ from S and R from $\overline{R}$ by means of an inverter; we shall use NAND gate inverter. The complete circuit is drawn in Fig. 24.3(a) and its symbol in Fig. 24.3(b).



(a) 54/7400



(b) Logic symbol

R	S	Q
0	0	Last state
0	1	1
1	0	0
1	1	? (Forbidden)

(c)

Fig. 24.3 *RS flip-flop latch*

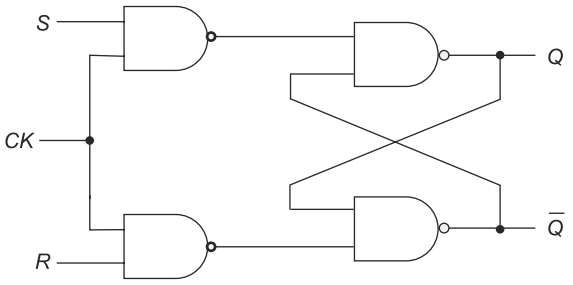
24.5 GATED FLIP-FLOPS

RS flip-flops (or latch) are said to be *transparent* as any change in R or S is immediately transmitted to the outputs Q and $\overline{Q}$. Whether R, S change will be reflected in Q, is achieved by two NAND gates.

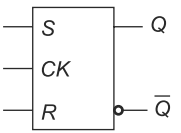
Clocked RS Flip-flop

A clock signal is fed to both input NAND gates as shown in Fig. 24.4(a).

- When the clock is HIGH, the output of the two-input NAND gate is $\overline{S}$, $\overline{R}$. So the latch operates normally.



(a)



CK	R	S	Q_{n+1}
1	0	0	Q_n (no change)
1	0	1	0
1	1	0	1
1	1	1	? (Illegal)
0	X	X	Q_n (no change)

X means 'do not care'; 1 or 0

(b) IEEE symbol and truth table

Fig. 24.4 *Clocked RS flip-flop*

- When the clock is LOW, the output of the two input NAND gates is (1, 1) and the latch is disabled and output does not change.

The truth table and symbol of a clocked *RS* flip-flop are shown in Fig. 24.4(b).

24.6 PRESET AND CLEAR

When power is turned on, the flip-flop assumes a random state depending upon the time delay of the gates. It is often desirable to predefine the starting state (set or reset) of the flip-flop. This is achieved by two inputs, called *preset* and *clear*, as shown in Fig. 24.5. These inputs are applied in the interval between two clock pulses.

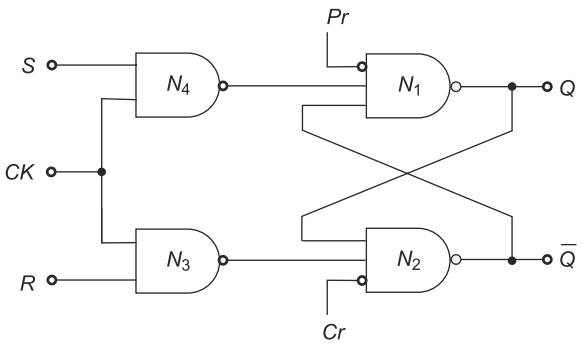


Fig. 24.5 *Present and clear*

Assume $CK = 0$. When $Pr = 0$ and $Cr = 1$, Q is 1, so $\bar{Q} = \overline{1.1.1} = 0$; the flip-flop is set. When $Pr = 1$ and $Cr = 0$, $\bar{Q}$ is 1 and $Q = \overline{1.1.1} = 0$; the flip-flop is in reset state or cleared. When Pr and Cr are both 1, the circuit functions like a normal clocked *SR* flip-flop. If $Pr = Cr = 0$, both Q and $\bar{Q}$ will become 1, which is not desired. So $Pr = Cr = 0$ is not allowed.

Pr and *Cr* inputs are applied direct, not in synchronism with the clock pulse. Thus, they are asynchronous inputs and are also called direct set and direct reset respectively. Since the desired function is performed when the corresponding input is LOW ($Pr = 0$, $Cr = 1$ sets and $Cr = 0$, $Pr = 1$ clear the flip-flop); they are active low inputs (indicated by placing a bubble at these inputs). The truth table with active low preset and clear is shown below.

Table 24.1 *Truth table of preset and clear*

CK	*Pr*	*Cr*	*S*	*R*	Q_{n+1}
1	1	1	0	0	Q_n
			0	1	0
			1	0	1
			1	1	Not allowed
0	0	1	×	×	1 (Set
0	1	0	×	×	0 (Reset)

24.7 CLOCKED *D* FLIP-FLOP

In an *RS* flip-flop, 1 is transferred to *Q* if $S = 1$, $R = 0$ and a 0 is transferred to *Q* if $S = 0$, $R = 1$. It means that while transferring 1/0 to *Q*, *R* and *S* should be complements of each other. This is achieved by an inverter and two AND gates as shown in Fig. 24.6(a). When *CK* is high, $D = 1000$ are entered into *S* and its complement to *R*. It means *D* value (1/0) appears at *Q*. Thus, data *D* is transferred to *Q*. When *CK* is low, system is disabled and *Q* remains unchanged.

The truth table and logic symbol are given in Fig. 24.6(b).

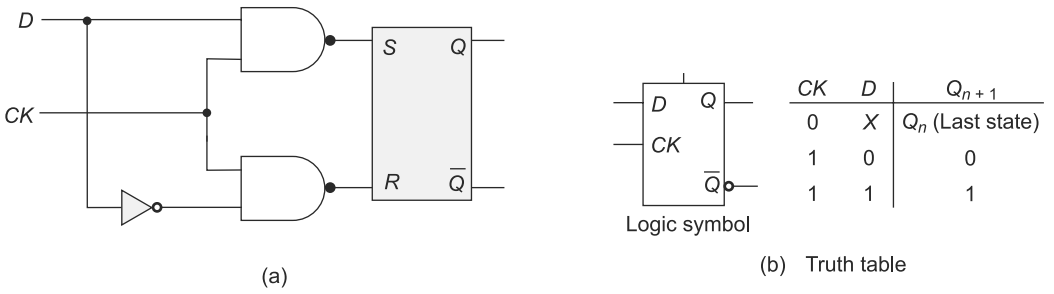


Fig. 24.6 *A clocked D flip-flop*

24.8 EDGE TRIGGERING

In edge triggering, short-duration pulses are generated from the clock signal of the same frequency, by passing the clock signal through certain gate arrangement. The clock signal of corresponding pulses are shown in Fig. 24.7. Positive pulses are produced when the clock signal goes from LOW to HIGH and negative pulses are produced when the clock goes from HIGH to LOW. So we have two types of edge triggering, positive edge (PT) and negative edge (NT) as shown in Fig. 24.7.

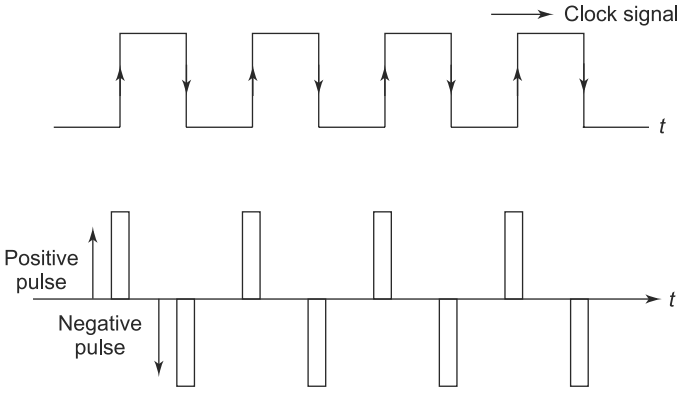


Fig. 24.7 *Edge triggering*

Pulse Production

PT (Positive Transition)

The clock signal is applied to NAND and AND. The output of NAND which acts as inverter is the second signal fed to AND as shown in Fig. 24.8(a). It is to be noted here that the output of an AND gate is HIGH only when both inputs are HIGH.

Because of signal inversion and direct input to AND is HIGH and the other is LOW; so AND gate output is LOW. However, the signal delay of t_p in the inverter causes both signals fed to AND gate to be HIGH for time t_p. This is low-to-high transition; a positive pulse. The pulse appears as the AND gate after a delay of t_p as shown in Fig. 24.8(b).

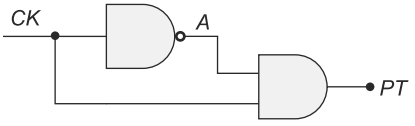


Fig. 24.8(a) *Positive transition*

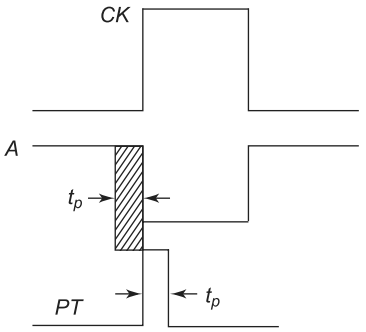


Fig. 24.8(b) *Pulse after delay*

NT (Negative Transition)

The output AND gate is replaced by an OR gate as shown in Fig. 24.9(a). It is reminded here that the output OR gate is LOW when both inputs are low.

The clock and its inverted signal *A* waveform are drawn in Fig. 24.9(b). Because of inverter delay t_p, when this clock, must become LOW, the signal *A* remains LOW for time t_p. Thus, for time t_p, the output of the OR, which is high, and then becomes low. This is the equivalent for HIGH to LOW, a negative pulse (NT).

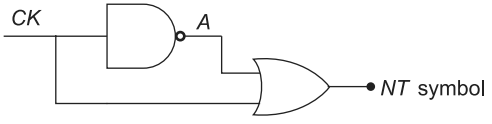


Fig. 24.9(a) *Negative transition*

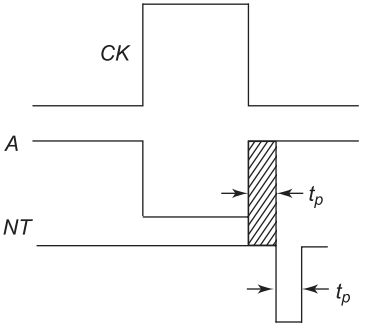


Fig. 24.9(b) *Inverted signal waveform*

Note:

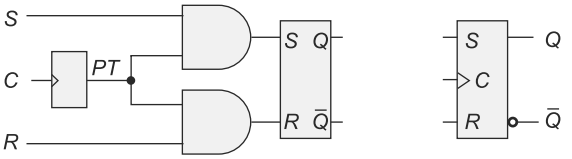
In case of edge triggering, $CK = 1$ will be replaced by arrows.

$\uparrow$ for RT and $\downarrow$ for NT

24.9 EDGE-TRIGGERED *RS* FLIP-FLOP

Positive-edge-triggered

The logic diagram, symbol and truth table are given in Fig. 24.10(a).



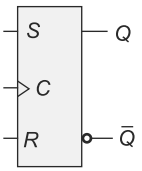
C	S	R	Q_{n+1}	Action
↑	0	0	Q_n	No change
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	?	Illegal

(a) Logic diagram (b) IEEE symbol (c) Truth table

Fig. 24.10(a) *Positive-edge-triggered RS flip-flop*

Negative-edge-triggered

The symbol and truth table are shown in Fig. 24.10(b).



C	S	R	Q_{n+1}	Action
↓	0	0	Q_n	No change
↓	0	1	0	Reset
↓	1	0	1	Set
↓	1	1	?	Illegal

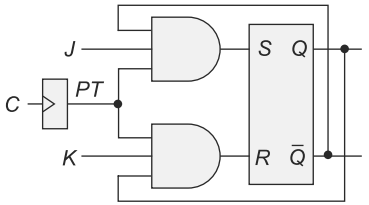
(a) IEEE symbol (b) Truth table

Fig. 24.10(b) *Negative-edge-triggered RS flip-flop*

24.10 POSITIVE-EDGE-TRIGGERED *JK* FLIP-FLOPS

In Fig. 24.11, the pulse-forming box changes the clock into a series of positive pulses, and thus this circuit will be sensitive to PTs of the clock. The basic circuit is identical to the previous positive-edge-triggered *RS* flip-flop, with two important additions:

1. The Q output is connected back to the input of the lower AND gate.
2. The $\overline{Q}$ output is connected back to the input of the upper AND gate.



C	J	K	Q_{n+1}	Action
↑	0	0	Q_n (Last state)	No change
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	$\overline{Q}_n$ (toggle)	Toggle

(a) One way to implement a *JK* flip-flop (b) Truth table

Fig. 24.11 *Positive-edge-triggered JK flip-flop*

Table 24.2 *Development truth table*

		Previous state				
J	*K*	Q_n	$\bar{Q}_n$	*S*	*R*	Q_{n+1}
0	0	1	0	0	*Q*	Q_n
		0	1	0	0	Q_n
0	1	1	0	0	1	0 Resets
		0	1	1	0	0 no change
1	0	1	0	0	0	1 no change
		0	1	0	1	1 set
1	1	1	0	0	1	0 resets (Toggle)
		0	1	1	0	1 sets

The above table conforms the truth table of the *JK* flip-flop.

Race-Around Condition

If the triggering pulse is longer in time (t_p) than the delay in toggle time (f_g), i.e. $t_g < t_p$, triggering occurs again, so the five outcomes are certain. This problem is remedial by master-slave condition of true *JK* flip-flop if such situation is lost likely in edge triggering.

24.11 *JK* MASTER-SLAVE FLIP-FLOP

Two *JK* flip-flops are connected as shown in Fig. 24.12.

The master feeds the slave such that

$$J_s = Q_m,\ K_s = \bar{Q}_m$$

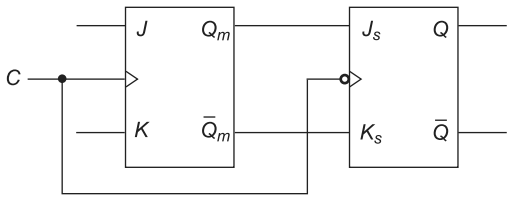


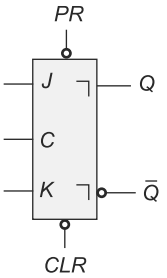
Fig. 24.12 *Master-slave flip-flop*

The master is triggered by the positive end of clock pulse and the slave follows with delay, triggered by the negative end of the pulse. Q_m and $\bar{Q}_m$ of the master as triggers are in accordance with the *JK* truth table. If $Q_m = 0$ and $\bar{Q}_m = 1 \Rightarrow J_s = 0$. $K_s = 1$. Upon triggering up the slave, the output is $Q = 0$ and $Q = 1$, same as the master. Similarly, $Q_m = 1$ and $\bar{Q}_m = 0 \Rightarrow J_s = 0$, $K_s = 1$. Upon triggering of the slave, the output is $Q = 1$, $\bar{Q} = 0$; same as the master. It means the slave simply copies the master with a delay.

7476 JK Master Slave

The symbol and truth table are given in Fig. 24.13. It is a pulse-triggered-flip-flop. Presetting *PR* low, Q = H, and when CLR is low Q = L.

❑ **Operation** When the clock C is high, master Q_m, $\bar{Q}_m$ changes according to JK, which therein changes during high period of pulse. The contents of the master are shifted to the slave at NT of clock pulse. This is indicated by the symbol ⎍⎍. The symbol ⎍ at output indicates postponed output changes in JK should be in low part of the pulse.



(a) Symbol

C	J	K	Q_{n+1}	Action
⎍	L	L	Q_n	No change
⎍	L	H	L	Reset
⎍	H	L	H	Set
⎍	H	H	$\bar{Q}_n$	Toggle

(b) Truth table

Fig. 24.13 *Operations of JK master-slave flip-flop*

24.12 *JK* CLOCKED CONVERSIONS

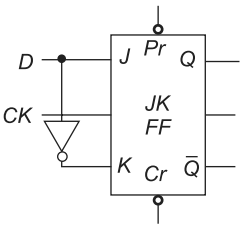
D Flip-Flop [Fig. 24.14]

J and K are made complementary by connecting these through an inverter.

$D = 0 = J, K = 1 \rightarrow Q = 0$

$D = 1 = J, K = 0 \rightarrow Q = 1$

Hence, the truth table on clock point D appears at Q; data is transferred as shown in Fig. 24.13(b).



(a)

Truth table

D	Q_{n+1}
0	0
1	1

(b)

Fig. 24.14 *JK conversions of D flip-flop*

T Flip-Flop [Fig 24.15]

J and K are connected

$T = 0, J = K = 0 \rightarrow Q_n$ (no change)

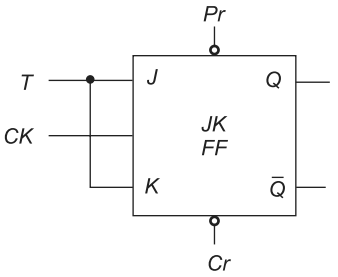
$T = 1, J = K = 1 \rightarrow \bar{Q}_n$ (flips)

On positive clock pulse,

$T = 0, Q_{n+1} = Q$

$T = 1, Q_{n+1} = \bar{Q}_n$ } Toggle

as shown in Truth table of Fig. 24.15.



Truth Table

T	J	K	Q_{n+1}
0	0	0	Q_n
1	1	1	$\bar{Q}_n$

Fig. 24.15 *JK conversions of T flip-flop*

Summary of Excitation Tables of Flip-flops

In problems involving flip-flops, a table listing the required inputs for a certain change of state, called excitation table, is very helpful. The excitation table for various kinds of flip-flops are given in Table 24.3.

Table 24.3 *Excitation table for various kinds of flip-flops*

(a) *SR*

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(c) *JK*

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) *D*

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

(d) *T*

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Summary

➢ In this chapter flip-flops are introduced and their conversions are described. IEEE logic symbols are explained NAND gate and RS flip flop are discussed. Functional truth tables of preset and clear and clocked D flip-flop explained. Edge triggering, edge trigged RS flip-flop JK master-slave flip-flop are also explained.

Exercises

Review Questions

1. What is a latch?
2. Why are universal gates preferred for making flip-flops?
3. Clear the comparative changes in various flip-flops.
4. How does a sequential circuit differ from a combinational circuit?
5. Explain the term *edge triggering*.
6. Draw and explain with excitation table the *RS*, *JK*, *D* and *T* flip-flop.

Problems

1. (a) Identify the flip-flop of Fig. 24.16.
   (b) If $Q = 1$, what are R and S?
   (c) if $\overline{S} = 1$ and $\overline{Q} = 0$, what is R?
   (d) $S = 0$, $R = 1$, what is Q?
   Note: NOR gate output is 1 only if both inputs are 1.
2. For pin diagram of Fig. 24.16, is it a flip-flop? If so what kind?
   Hint: Two inputs of the two NORs make three inputs; NORs as two input NORs.
3. For the NAND-based flip-flop of Fig. 24.17,
   (a) $R = 0$, $\overline{S} = 1$; what would be Q?
   (b) For $\overline{Q} = 1$; what would be $\overline{R}$, $\overline{S}$?
   Hint: $\overline{Q} = \overline{S + Q}$
   $Q = \overline{R + \overline{Q}}$

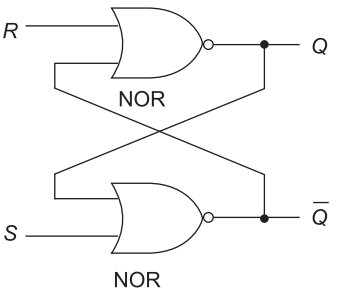


Fig. 24.16

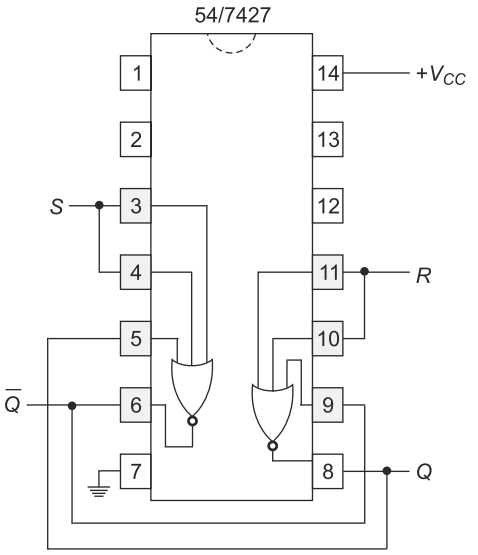


Fig. 24.17

4. Draw the symbols of *RS* flip-flop for various types of triggering.
5. For the NOR gate flip-flop of Fig. 24.14, label the logic levels (1/0) on LED pin for
(a) $R = S = 0$ (b) $R = S = 1$ (c) $R = 0, S = 1$ (d) $R = 1, S = 0$

Pin No.1	*(a)*	*(b)*	*(c)*	*(d)*
1	0	1	0	1
2	0	1	0	1
3	1	0	1	0
5	1	0	1	0
12	0	1	1	0
13	0	1	1	0
11	1	0	1	0
9	0	0	1	0
4	1/0	(last state) conflict	1	0
8	1/0		1	0
6	0/1		0	1
10	0/1		0	1

6. Why is an edge triggered flip-flop is preferred over one with a clocked angle gates?
7. Establish the equivalence of the flip-flop of Fig. 24.18. What happens when the clock is low?

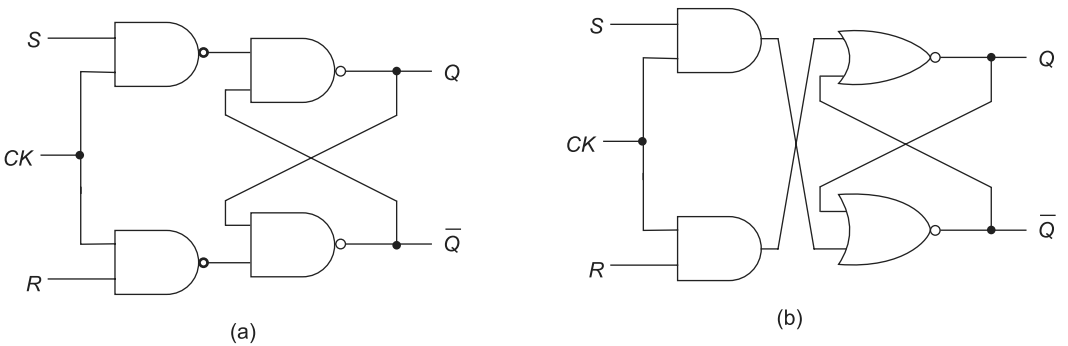


Fig. 24.18

8. Check the given excitation table of various flip-flops.

$Q_n \rightarrow Q_{n-1}$		S	R	J	K	D	T
0	0	0	×	0	×	0	0
0	1	1	0	1	×	1	1
1	0	0	1	×	1	0	1
1	1	×	0	×	0	1	0

Hint: Look at the truth table of the flip-flops in the reverse way.

9. Show that the *D* flip-flop excitation table connected as in Fig. 24.19 acts as an *RS* flip-flop.
Hint: A bubble at the input of the AND gate is the symbol of the inverter.

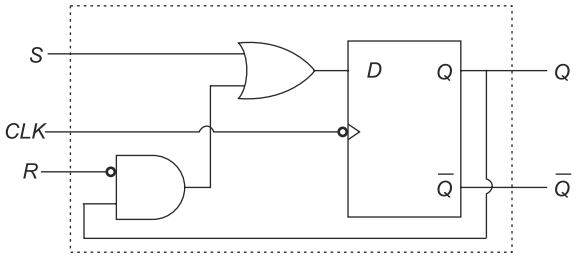


Fig. 24.19

10. Figure 24.20 shows the input waveform *R*, *S*, and *EN* applied to a clocked *RS* flip-flop. Below these waveforms, draw the timed output *Q* waveform.

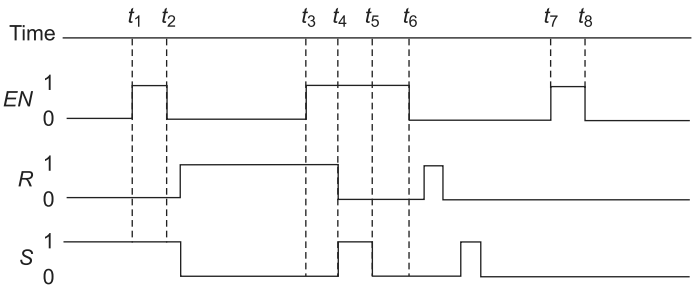


Fig. 24.20

11. Draw the output waveform for the following waveform input to the *SR* flip-flop (Fig. 24.21).

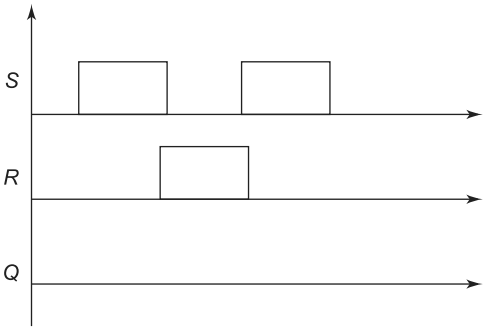


Fig. 24.22

12. Implement the 4:1 multiplexer using basic gates.
13. In the sequential circuit of Fig. 24.15, the NOR gates are replaced by NAND gates. Check that its operation agrees with the *SR* flip-flop truth table (Table 24.2).
Hint: NAND gate the output is 0 only if both inputs are 1.

14. In an *SR* flip-flop (Fig. 24.19), *S* is connected to *R* through a NOT gate input (1/0) given to *S*. Using the truth table 24.2, show that it acts as D flip-flop. Identify the output terminal.

Multiple-Choice Questions

1. A flip-flop is
   (a) a combinational circuit (b) a sequential circuit
   (c) an analog to digital converter (d) a digital to analog converter
2. The race-around condition occurs in
   (a) *SR* flip-flop (b) *D* flip-flop (c) *T* flip-flop (d) *JK* flip-flop
3. Race-around condition is avoided by using
   (a) master-slave flip-flop (b) set reset flip-flop
   (c) level-triggered flip-flop (d) *D* flip-flop
4. The *D* flip-flop is mainly used in
   (a) counters (b) serial abler (c) shift registers (d) all of these
5. Which property of the flip-flop is used in counter designing?
   (a) Shifting (b) Toggling (c) Set-Reset property (d) None of these
6. Which of the following table is used for determining input if given present state and next state?
   (a) Characteristics table (b) Truth table (c) Excitation table (d) None of these
7. The race-around condition in *JK* flip-flop occurs when
   (a) $J = 0, K = 1$ (b) $J = 1, K = 0$ (c) $J = 1, K = 1$ (d) $J = 0, K = 0$
8. In a master-slave *JK* flip-flop,
   (a) the slave follows the output of the master (b) the master follows the output of the slave
   (c) both work independently (d) none of these
9. The reason for race-around condition to occur is
   (a) the clock period is less than the propagation delay of the gates
   (b) the clock period is greater than the propagation delay of the gates
   (c) because of the improper feedback connection
   (d) because of the circuit delay involved
10. The *SR* flip-flop processes illegal output only when
    (a) $S = 0, R = 0$ (b) $S = 0, R = 1$ (c) $S = 1, R = 0$ (d) $S = 1, R = 1$

Answers

Problems

1. (a) *RS* (b) $R = 0$, $S = 1$ (c) 0 (d) 0.
2. *RS* flip-flop
3. (a) 0 (b) 0
14. Not given

Multiple-Choice Questions

1. (b) 2. (d) 3. (a) 4. (c) 5. (b) 6. (c) 7. (c) 8. (a) 9. (b) 10. (d)

Registers and Counters

chapter 25

Goals & Objectives

- Introduction of shift registers—series in serial out (SISO) serial in parallel out (SIPO), parallel in serial out (PISO), parallel in parallel out (PIPO)
- Explanation of counters—asynchronous counter and synchronous counters

25.1 INTRODUCTION

A register can store data, which is entered into it. The data can be taken out when needed.

Counters count the input pulses, which have known frequencies. So these can measure time.

25.2 SHIFT REGISTERS

Data are entered and stored in a shift register. It can then be taken out when needed. A 4-bit shift register is shown in Fig. 25.1. It comprises 4 *JK* flip-flops in which data are entered.

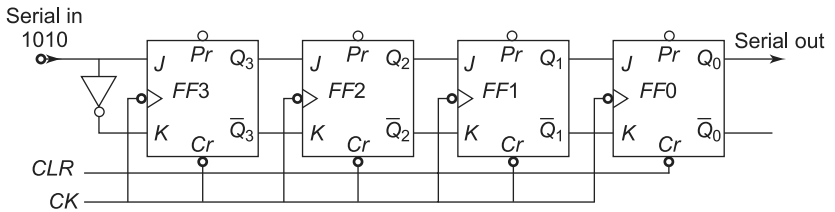


Fig. 25.1 *4-bit shift register*

FF3 J, *K* terminals are connected through an inverter so that it acts as D flip-flop through which the data are entered; the flip-flops are cleared by placing 0 at CLR. During a normal operation, the CLR is held at 1. Also, *Pr* is held at 0 so that these do not interfere with normal operation of the registers.

Operation

All the flip-flops are triggered by common clock pulses (CK), data (010) is now fed in LSD first and MSD last as shown in Table 25.1.

Table 25.1 *Operation of shift registers*

Clock pulse	*Serial in*	Q_3	Q_2	Q_1	Q_0 *(serial out)*	
0	0	0	0	0	0	
1	1	1	0	0	0	
2	0	0	1	0	0	
3	1	1	0	1	0	Data entered
4	0	0	1	0	1	
5	0	0	0	1	0	
6	0	0	0	0	1	
7	0	0	0	0	0	1 Register cleared

25.3 REGISTER TYPE

- Serial In Serial Out (SISO)
- Serial In Parallel Out (SIPO)
- Parallel In Serial Out (PISO)
- Parallel In Parallel Out (PIPO)

A 4-bit shift register which can operate as all-fuse type is shown in Fig. 25.2. The SISO operation is same as illustrated in Fig. 25.1. All we need to explain is the parallel operation.

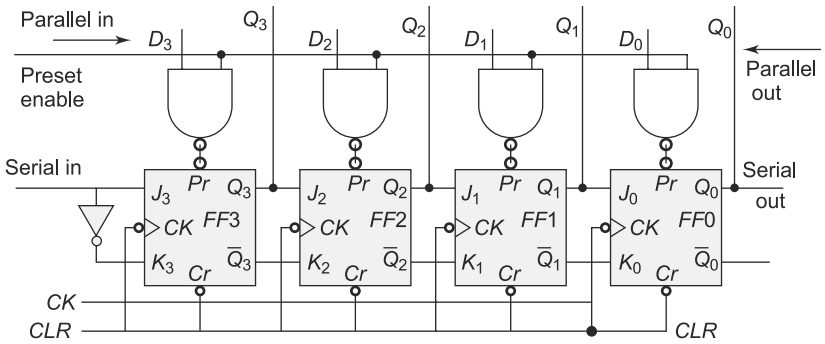


Fig. 25.2 *4-bit shift register*

Parallel Out

Connections are directly taken from Q_3 to Q_0 outputs of flip-flops.

Parallel In

After clearing the register, 'parallel enable' input is made. The results in NAND gates to act as inverters.

Any D_i input causes

$D_i = 0$, $P_r = 1$ and $Q_i = 0$

$D_i = 1$, $P_r = 0$ and $Q_i = 1$

Data is thus entered in parallel (simultaneously) at Q_is. It can then be read at $Q_3 - Q_0$ or it can be serially output by applying four pulses.

Shifting of Data to Left

In the register of Figs 25.1 and 25.2, the data is shifted from left to one bit at clock pulse by feeding output of FF0 to input of FF1, and FF1 to FF2, FF3. On the occurrence of a pulse, the data word will shift one bit to left; this logic is shown in Fig. 25.3.

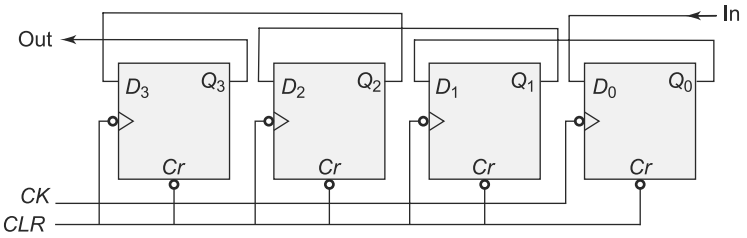


Fig. 25.3 *Register shift left*

Bidirectional Register

By combining Figs 25.1 and 25.3 through AND-OR-logic, we can build a bidirectional shift register. This logic is shown in Fig. 25.4 in which AND gets 1 input, while the other AND gets 0, and the connection in one is Q, while the other will be $\bar{Q}$.

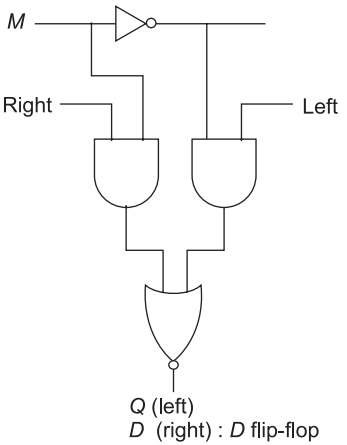
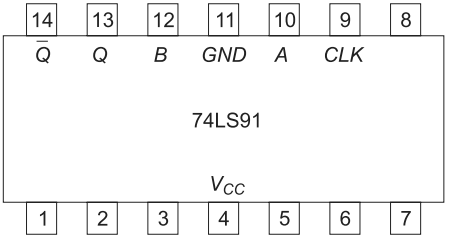


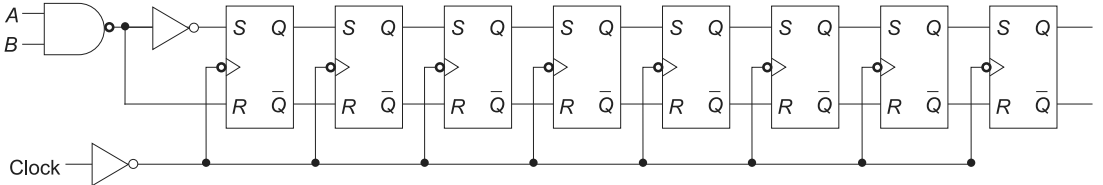
Fig. 25.4 *Bidirectional register*

25.4 COMMERCIALLY AVAILABLE TTL MSI/LSI REGISTERS

Serial In Serial Out—54/74 LS91 8 bits
Serial In Parallel Out—54/74164 8 bits
Parallel In Serial Out— 54/74165 8 bits
Parallel In Parallel Out—54/74198 8 bits
An example of 74LS91 shift register is shown below in Fig. 25.5.



(a) DIP pinout



(b) Logic diagram

Fig. 25.5 *74LS91 8-bit shift register*

The NAND gate with inputs A and B simply provides a gating function for the input data stream if desired. If B is set at 1, the NAND acts as inverter for input at A.

The two inverters feed the input at S of first flipflop. A_1 as data sets $S = 1$ and $R = 0$. A_0 as data resets $S = 0$ and $R = 1$.

If gating is not desired, simply connect the pins 10 and 12 together and apply the input data stream to this connection. If $A = B$, NAND gate acts as inverter.

25.5 COUNTERS

Binary counters are one of the most important and widely used of all digital circuits. A counter is a circuit that counts the number of occurrences of an input (in terms of positive or negative edge transitions in the case of a binary input). Each count, a binary number, is called a state of the counter. Hence, a counter counting in terms of n bits has 2^n different states. The number of different states of a counter is also known as the *modulus* of the counter. Thus, an n-bit counter is a modulo 2^n counter.

Counter circuits are primarily constituted of flip-flops, which along with combinational elements are used for the generation of control signals. Depending on the manner in which the flip-flops are triggered, counters can be divided into two major categories:

1. Asynchronous counter (ripple counter)
2. Synchronous counter

In case of an *asynchronous counter*, not all the flip-flops are clocked simultaneously, whereas in a *synchronous counter*, all the flip-flops are clocked simultaneously.

If the counter counts in such a way that the decimal equivalent of the output increases with successive clock pulses, it is called an UP counter. If it decreases, it is called a DOWN counter. An UP/DOWN counter can also be designed which can count in any direction depending upon the control input.

A decoding circuit can be connected to the output of a counter in such a way that the output of the circuit goes high (or low) only when the counter contents are equal to a given state.

25.6 ASYNCHRONOUS COUNTERS

Figure 25.6 shows a 3-bit (modulo 8) asynchronous counter. As J and K are tied together to 1 input, the JK, flip-flop act as T-flip-flop. The Q-output of one flip-flop feeds the CK trigger of the next flip-flop.

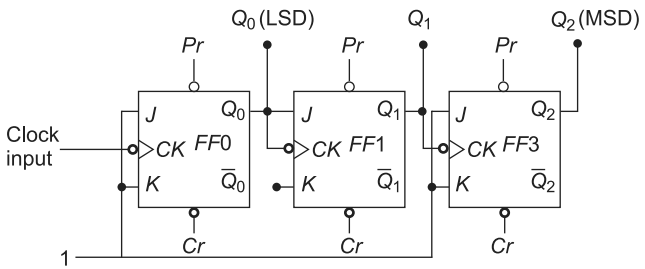


Fig. 25.6 *3-bit asynchronous counter (UP)*

Operation

All the flip-flops are initially cleared. The clock pulses are then applied with each clock pulse NT (1 to 0)\Q_0 toggles. For each NT (1 to 0) of Q_0, Q_1 toggles; similarly 1 to 0 transition of Q_2 toggles. The transition and

count are shown in Table 25.2. Thus, the counter counts from 0 to 7(111), these all the three transit from 1 to 0 and the counter returns to 0. As the pulses get applied to flip-flops in sequence, it is also called a *ripple counter*.

Table 25.2 *Operations of asynchronous counter*

Input (Clock)	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Observation

The clock transits (NT) 8 times, Q_0 4 times, Q_1 2 times, and Q_3 1 time. The wave frequency reduces by a factor of 2 at each stage (frequency division).

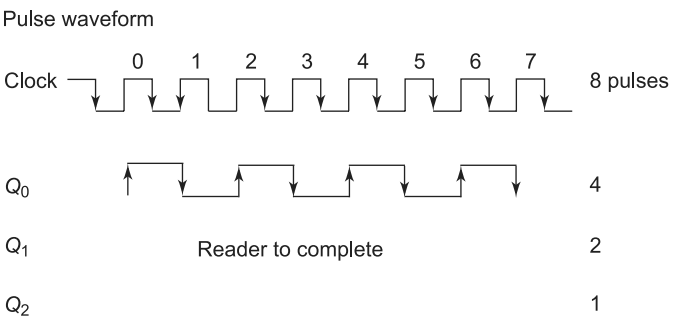


Fig. 25.7 *Pulse waveform*

❑ **Down Counter** $\overline{Q}$s are connected to of the next flip-flop. As $\overline{Q}$ toggles from 1 to 0, the corresponding Q toggles 1 to 0, which is count down.

❑ **Up-Down Counter** *CK* are connected to Q for up down and $\overline{Q}$ through AND-OR logic.

❑ **Preset** The counter through *Pr* input is set to desired value before the clock pulses are applied. The logic circuit is beyond the scope of this book.

25.7 SYNCHRONOUS COUNTER

The clock pulses are applied synchronously (at the same time) to all the flip-flops. This avoids the ripple delay of asynchronous counter and logic complexity increases.

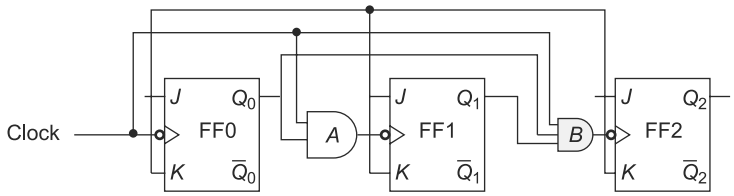


Fig. 25.8 *Synchronous counter (up)*

Connected Diagram and Operation

Clock is applied to all the three flip-flops simultaneously. However clock NT for FF_1 and FF_2 must pass through AND gates *A* and *B* respectively. AND gate Δ passes NT at NT of clock, and NT (1 to 0) of Q_0, then FF_1 toggles.

- AND gate *B* passes NT at NT of clock, and NT (1 to 0) of Q_0 and Q_1, FF_2 then toggles.
- FF0 toggles at every NT of clock, at clock frequency.

Values of Q_2, Q_1, Q_0 against count are shown in Table 25.3. 1 to 0 transitions are also indicated there.

Table 25.3 *Operation of synchronous counter*

Count	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1 →
2	0	1	0 ↓
3	0	1 →	1
4	1	0 ↓	0 ↓
5	1	0	1 →
6	1	1	0 ↓
7	1 →	1 →	1
8	0 ↓	0 ↓	0 ↓

Count Down

The A gate is for Q_0 and $\overline{Q}_0$ and the B gate is fed $\overline{Q}_0$, $\overline{Q}_1$ and $\overline{Q}_2$. The counter is preset to $Q_2 = Q_1$. $Q_0 = 1$. The transition table of $\overline{Q}_2$, $\overline{Q}_1$, $\overline{Q}_0$ and the countdown is given in Table 25.4.

Table 25.4 *Countdown*

Count	Q_3	Q_2	Q_1
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

Example 25.1

How many flip-flops are needed in a shift register to store

(a) 6-bit binary numbers?

(b) Decimal numbers up to 24?

(c) Hexadecimal numbers up to E?

Solution

(a) 6

(b) $24 \rightarrow 11000$, five

(c) $E \rightarrow 14 \rightarrow 1110 \rightarrow$ four

Example 25.2

A shift register has eight flip-flops. What is the largest binary, decimal and hexadecimal numbers that can be stored in it?

Solution

(a) 11111111

(b) 255

(c) FF

Example 25.3

Name the four types of shift registers. Draw their block diagrams.

Solution

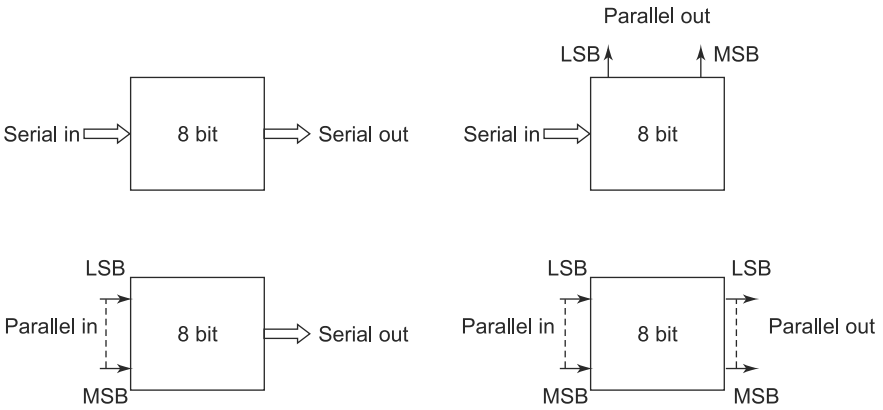


Fig. 25.9

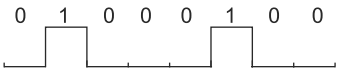
Example 25.4

How is the decimal number 68 is shifted into the register 74LS91 of Fig. 25.4? Prepare a table giving the state of each flip-flop on the clock pulses applied. Draw the waveform when the number has been shifted in the register. How many pulses are needed to clear the register?

Solution 68 in binary is 1000100.

Number to be entered	*Pulse no.*	*State register 8 bits*	
		MSD	*LSD*
	0		
01000100	1	00000000	
0100010	2	00000000	
010001	3	00000000	
01000	4	10000000	
0100	5	01000000	
010	6	00100000	
01	7	00010000	
0	8	10001000	
		01000100	

Waveform after 8th pulse



No. of pulses to clear the registers = 7

Example 25.5

How long will it take to shift 8-bit binary data into 54/74164 of Fig. 25.10 if the clock is (a) 1 MHz (b) 5MHz?

Solution

(a) 1 MHz = 10^6 cycles/second, Time for 8 cycles = $8 \times 10^{-6} = 8$ μs

(b) 5 MHz, Time for 8 cycles = $8 \times (10^{-6}/5) = 1.6$ μs

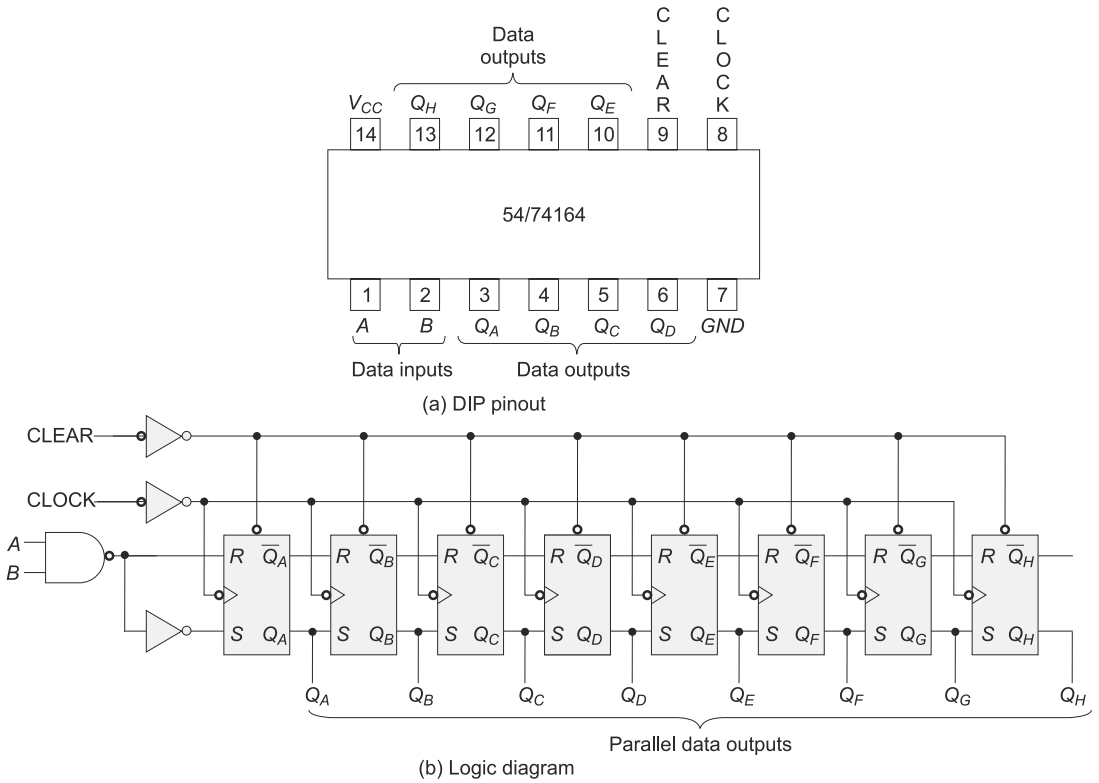


Fig. 25.10 *54/74164 8-bit shift register*

The register is enabled when $B = 1$, data at A will go to S of the first flip-flop. If $B = 0$, the register is disabled as $S = 0$ for data 1 or 0.

Example 25.6

How many flip-flops are needed for (a) Mod-128 counter, (b) Mod-64 counter, and (c) Mod-32 counter? What is the largest decimal number and largest hexadecimal number that can be stored in the Mod-64 counter?

Solution

(a) $128 = 2^7$, 7 flip-flops

(b) $64 = 2^6$, 6 flip-flops

(c) $32 = 2^5$, 5 flip-flops

Mod-64 is 6 flip-flops
Largest binary number that can be stored is 111111 → decimal 63 → Hexadecimal 63
Hexadecimal number AE

Example 25.7

What is the Mod of the counter to stove Hexadecimal number *AE*.

Solution

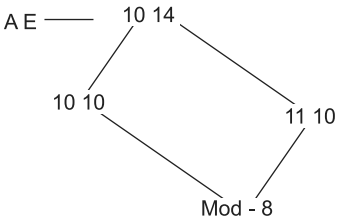


Fig. 25.11

Example 25.8

A 6-bit ripple down counter has the following states:

(a) 101010 (b) 001100 (c) 110000

Determine the number of flip-flops that would be complemented after the application of one clock pulse.

Solution Subtract 1 in each case.

(a) 101010
−1
101001 First and second from right are complemented two.

(b) 001100
−1
001010 Three

(c) 110000
−1
101110 Four

Example 25.9

It is desired to reduce the frequency of a pulse signal to one half. Suggest a suitable circuit for the signal.

Solution

All it needs is a single *T* flip-flop with negative edge triggering. See Fig. 25.12.

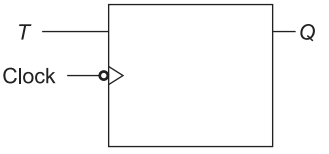


Fig. 25.12

Example 25.10

Design a mod-3 counter (non-linear).

Solution

$2^1 < 3 < 2^2$

We need 2 flip-flops. $\bar{B}$ is connected to *J* of FF1 with synchronous triggering.

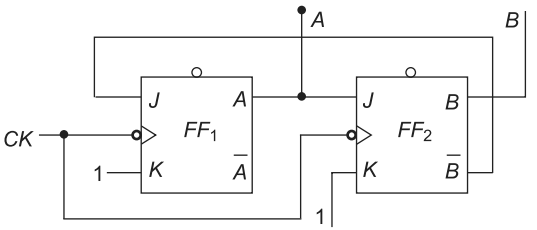


Fig. 25.13

- $A = 0, B = 0, \quad J_1 = \overline{B} = 1, J_2 = A = 0$, count 0
- On negative edge triggering (NT), count 1
  FF_1 toggles $\rightarrow A = 1, B = 0, \overline{B} = 1 = J_1, J_2 = A = 1$
- On next NT Count 2
  $A = 0, B = 1, \quad J_1 = \overline{B} = 0, \; J_2 = A = 0$
- On next NT, count 3
  $A = 0, B = 0$
- Next cycle starts

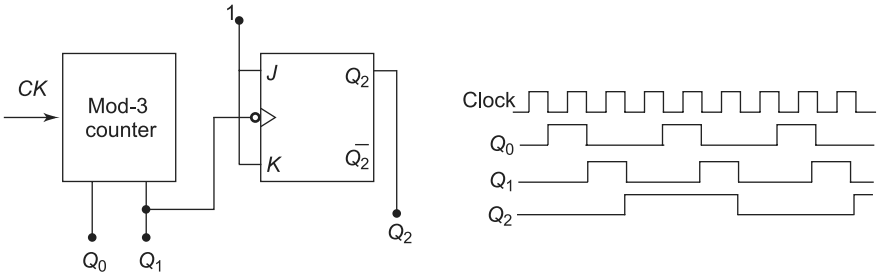
Truth table

Count	*B*	*A*
0	0	0
1	0	1
2	1	0
2	0	0 Next cycle

Example 25.11

Convert Mod-3 counter to a Mod-6 counter.

Solution At the output of the Mod-3 counter, connect a *JK* flip-flop in toggle mode as shown in Fig. 25.14. The result is a 2×3 = Mod 6 counter.



(a) Mod-6 counter (b) Waveforms

Fig. 25.14

Counter state

Count	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	1	0	0
4	1	0	1
5	1	1	0
6	0	0	0 repeats

Summary

➢ Shift registers have been introduced and synchronous and asynchronous counters have been explained.

Exercises

Review Questions

1. Explain shift registers with examples.
2. Distinguish between synchronous and asynchronous counters.

Problems

1. How many flip-flops would be required for a shift register to store
   (a) 0.7-bit number? (b) decimal number up to 64? (c) hexadecimal numbers up to I?
2. A shift register has 12 flip-flops. What is the largest (a) decimal number, and (b) hexadecimal number that can be stored in it?
3. The hexadecimal number *AB* is stored in 54/74LS91 in Fig. 25.4. Show the waveform at the output, assuming that the clock is allowed to run for eight cycles and that $A = B = 0$. What hexadecimal number will remain stored if the clock is run for 4 more cycles.
4. Four *D* flip-flops are connected to form a shift register. The register is initially empty. The number 1001 is shifted into the register.
   (a) Complete the following table.

Data	Pulse No.	Q_3	Q_2	Q_1	Q_0
1001					

   (b) Also draw the waveform at third clock transition.
5. For S4/74164 of the Fig. 25.12, $B = 1$, clear = 1, and a 1 MHz clock is used to shift the decimal number 200 into the register at *A*. How much time will it take? Propose the table as below.

Data	Pulse count	Register state
8-bit		

6. Assume that binary number 1100 (left 1 MSB and right CS0) is present in the shift register of Fig. 25.2. It is desired to reverse the order of the stored bits. How can this be done? If the clock frequency is 1 MHz, what would be the time required to do so? Assume that parallel entry of data is not allowed.
7. Using four *D* flip-flops design a shift-left register and explain its operation.
8. Getting the idea from Fig. 25.7, draw the schemetion of four *JK* flip-flops. Design an asynchronous down counter and write its truth table.
9. Getting the idea from Fig. 25.9, draw the schemation of a model synchronous down counter using *T* flip-flops and prepare its truth table.
10. The synchronous up/down, mod-16 by additional logic circuitry is preset at 1010. Write its truth table as clock pulses are applied for up count from this state.
11. An up counter, 6-bit binary, has the following states:
    (a) 1101010 (b) 001100 (c) 110000
    Determine the number of flip-flops which would be complemented after application of one clock pulse.

Multiple-Choice Questions

1. Which of the following is a type of registers?
   (a) Serial in serial out (b) Serial in parallel out (c) Parallel in serial out (d) All of these
2. Asynchronous counters are also called
   (a) ring counters (b) ripple counter (c) BCD counter (d) Mod-6 counter
3. A Mod-10 counter has a total of—states
   (a) 10 (b) 15 (c) 9 (d) ∞
4. A counter can count in the direction
   (a) up (b) down (c) up-down (d) all of these
5. A counter is
   (a) a group of registers (b) a memory storage device
   (c) a group of transistors (d) none of these
6. A 4-bit shift register will have
   (a) 4 flip-flops (b) 8 flip-flops (c) 2 flip-flops (d) none of these
7. A shift register is used for
   (a) storing and shifting binary information (b) to give specific sequence of binary number
   (c) performing some special Boolean functions (d) none of these
8. Which of the following shift register will require minimum number of clock pulses to give the output?
   (a) Serial In Serial Out (SISO) (b) Parallel In Serial Out (PISO)
   (c) Serial In Parallel Out (SIPO) (d) Parallel In Parallel Out (PIPO)
9. Which of the following are the special **fy*** of counter?
   (a) Johnson counter (b) BCD counter (c) Ring counter (d) Both (a) and (c)
10. The total number of states a counter can count before reaching the first state is called
    (a) modulus of the counter (b) mod number of the counter
    (c) count of the counter (d) both (a) and (b)

Answers

Problems

3. A

4. (b)
6. Feedback serial output to serial input. Apply two clock pulses, 0011, 2 μs.
11. Answer (a) 1 (b) 1 (c) 1

Multiple-Choice Questions

1. (d) 2. (b) 3. (a) 4. (d) 5. (a) 6. (a) 7. (a) 8. (d) 9. (d) 10. (a)

Digital to Analog (D/A) and Analog to Digital (A/D) Converters

chapter 26

Goals & Objectives

- Introduction of Analog to Digital (A/D) and Digital to Analog (D/A) converters
- Functional diagrams of converters (A/D and D/A)
- Calculating the accuracy and resolution of D/A and A/D converters with examples

26.1 INTRODUCTION

Digital-to-Analog (D/A) and Analog-to-Digital (A/D) conversion form two very important aspects of digital-data processing. Digital-to-analog conversion involves translation of digital information into equivalent analog information. As an example, the output of a digital system might be changed to analog form for the purpose of driving a pen recorder and servomotors which drive the cursor arms of a plotter. In this respect, a D/A converter is sometimes considered a *decoding device*.

The process of changing an analog signal to an equivalent digital signal is accomplished by the use of an A/D converter. For example, an A/D converter is used to change the analog output signals from transducers (measuring temperature, pressure, vibration, etc.) into equivalent digital signals which can be fed to a digital system for digital processing. An A/D converter is often referred to an encoding device since it is used to encode signals for entry into a digital system.

Digital-to-analog conversion is a straightforward process and is considerably easier than A/D conversion. In fact, a D/A converter is usually an integral part of any A/D converter. For this reason, we consider the D/A conversion process first.

26.2 DIGITAL-TO-ANALOG CONVERTER (DAC)

The analog output voltage V_A of an N-bit straight binary DAC converter is related to the digital equation

$$V_A = K(2^{N-1} b_{N-1} + 2^{N-2} b_{N-2} + \ldots + 2b_1 + b_0) \tag{26.1}$$

where K = proportionality factor

$$\left.\begin{aligned} b_j &= +1 \text{ if } j\text{th bit of input is } 1 \\ &= 0 \quad \text{if } j\text{th bit of input is } 0 \end{aligned}\right\}; j = 0 \text{ to } (N-1)$$

Weight Resistor DAC

As the D/A conversion involves a weighted sum corresponding to the input to the converter, the summing circuit of Fig. 26.1 can be used as a DAC. In this circuit,

$$I_i = I_{N-1} + I_{N-2} + \ldots + I_1 + I_0 \tag{26.2}$$

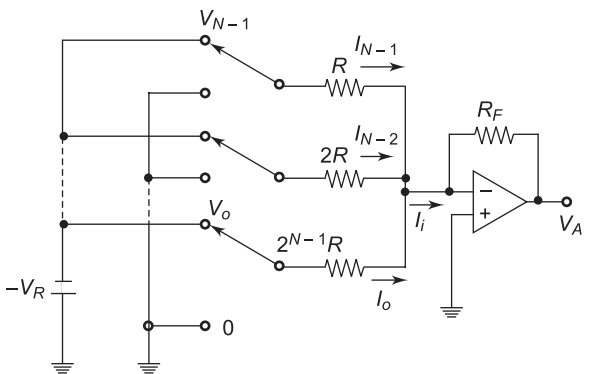


Fig. 26.1 *Weighted resistor DAC*

These currents can be expressed in terms of voltages as

$$I_{N-1} = V_{N-1}/R$$

$$I_{N-2} = V_{N-2}/2R$$

or $$I_0 = V_0/2^{N-1}\,R$$

Let $$V(0) = -b_0\,V_R$$

$$V(1) = -b_1\,V_R$$

Then $$V_{N-1} = -b_{N-1}\,V_R$$

The switches in the circuit are *digitally controlled* causing b_n to acquire values 0 or 1.
We can now express Eq. (26.2) as

$$I_i = -V_R\left[\frac{1}{R}b_{N-1} + \frac{1}{2R}b_{N-2} + \cdots + \frac{1}{2^{N-1}R}b_0\right] \tag{26.3}$$

The analog output of the circuit is given by

$$V_A = -R_F I_i$$

or $$V_A = V_R\left[\frac{R_F}{R}b_{N-1} + \frac{R_F}{2R}b_{N-2} + \cdots + \frac{R_F}{2^{N-1}R}b_0\right]$$

$$= K[2^{N-1}\,b_{N-1} + 2^{N-1}\,b_{N-1} + \ldots + 2^1 b_1 + 2^0 b_0] \tag{26.4}$$

where $$K = \frac{V_R R_F}{2^{N-1}R} \tag{26.5}$$

Hence, the circuit is a DAC.

For accurate conversion, the input voltages would have to be precisely known values, a condition that is not required in a digital system. The various weighing resistors would also have to be precisely formed, a very difficult requirement in an IC. In practice, the *R*-2*R* ladder discussed below is used.

R-2R Ladder Network

An *R*-2*R* ladder network is shown in Fig. 26.2(a). It uses resistors of only two values, *R* and 2*R*. The inputs to the resistor network are applied through digitally controlled switches.

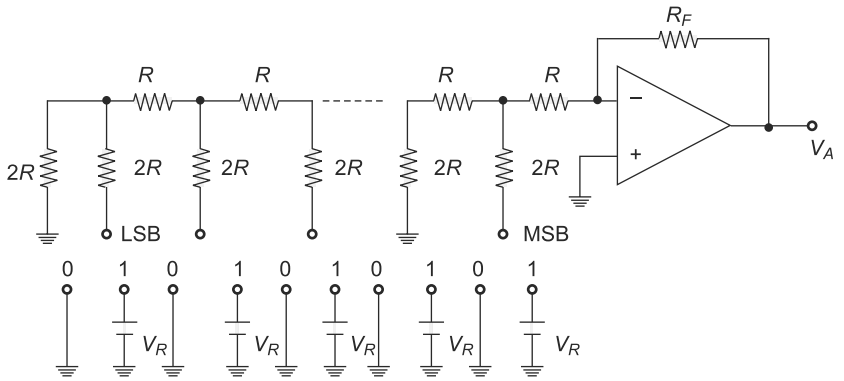
To analyse this circuit, consider a 3-bit *R*-2*R* ladder DAC as shown in Fig. 26.2(b), wherein the input is assumed as 001. Applying Thevenin's theorem at *XX*′, *YY*′ and *ZZ*′ we obtain circuits of Fig. 26.3 (a), (b) and (c) respectively. It is immediately seen that for input† 001, voltage $V_R/2^3$ is applied through 3*R* to the inverting terminal of the OP-AMP.

Similarly, for the digital inputs of 010 and 100, the equivalent voltages are $V_R/2^2$ and $V_R/2^1$ respectively with resistance 3*R* in each case. Therefore, we obtain equivalent circuit of Fig. 26.3(d) wherein the voltage V_A is given by

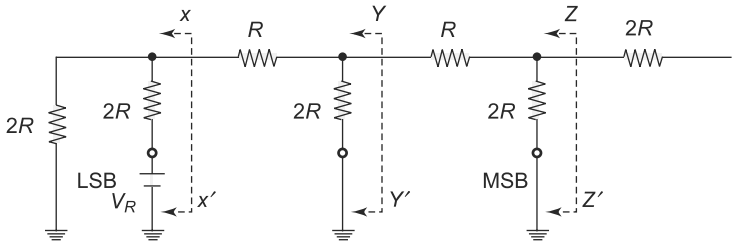
$$V_A = -\left[\frac{R_F}{3R}\frac{V_R}{2^3}b_0 + \frac{R_F}{3R}\frac{V_R}{2^2}b_1 + \frac{R_F}{3R}\cdot\frac{V_R}{2^1}b_2\right]$$

$$= -\left(\frac{R_F}{3R}\right)\left(\frac{V_R}{2^3}\right)\left[2^2 b_2 + 2^1 b_1 + 2^0 b_0\right]$$

† Note that binary digit are in reverse order, i.e. LSB to MSB.



(a) *R*-2*R* ladder DAC



(b) 3 bit R-2R ladder DAC network

Fig. 26.2

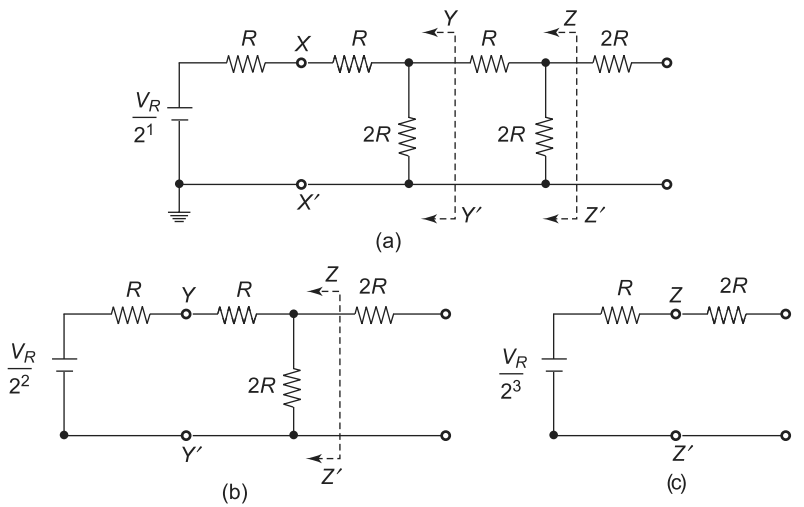


Fig. 26.3 *(Contd.)*

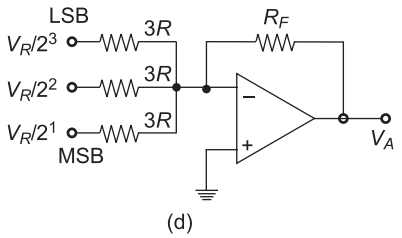


Fig. 26.3

The equation shows that the analog output voltage is proportional to the digital input. In general, for *N*-bit DAC,

$$V_A = V[2^N b_{N-1} + 2^{N-2} b_{N-2} + \ldots + 2^1 b_1 + 2^0 b_0] \tag{26.6}$$

where $R_F = 3R$ and $V_R = -2^N V$

The number of resistors required for an *N*-bit DAC is 2*N* in the case of an *R*-2*R* ladder, whereas it is only *N* in case of a weighted-resistor network. But because of wide spread in the resistance values for large *N,* a weighted resistor DAC is not widely used.

Implementation

The *R*-2*R* ladder D/A converter is implemented by the circuit of Fig. 26.4. When this strobe pulse is high, the input bits are fed to the register (4 *SR* flip-flops). The register output is fed to the level amplifier connected to the position voltage above (+10 V). For the register output of $b = 1$, the level amplifier output of + 0 V is fed to the ladder. Hence, V_A = equivalent of form bits b_3, b_2, b_1, b_0.

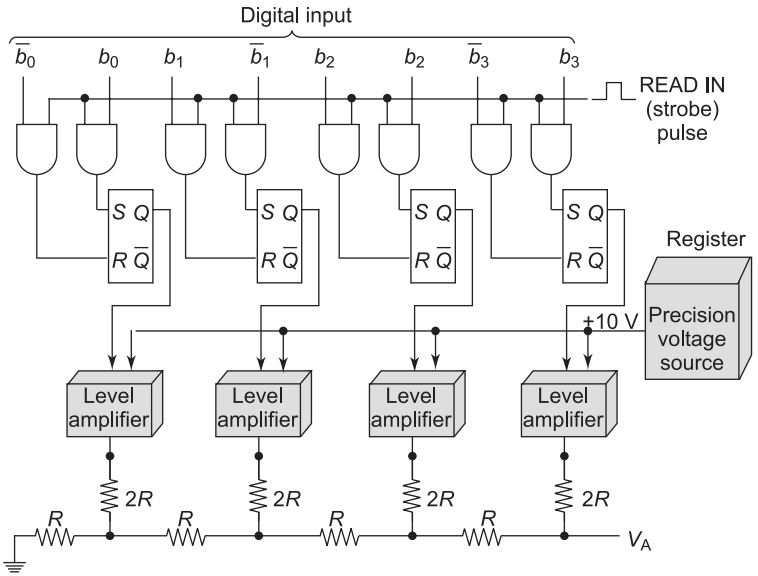


Fig. 26.4 *4-bit D/A converter*

$$V_A = 10\left\{\frac{b_3}{2^1} + \frac{b_2}{2^2} + \frac{b_1}{2^3} + \frac{b_0}{2^4}\right\};\ b_3 \text{ is MSD and } b_0 \text{ is LSD}$$

or
$$V_A = \frac{10}{2^4}(2^3 b_3 + 2^2 b_2 + 2^1 b_1 + 2^0 b_0) \tag{26.7}$$

In general, for N bits,

$$V_A = \frac{10}{2^N}\ (2^{N-1} b_{N-1} + 2^1 b_1 + 2^0 b_0);\ b_{N-1} \text{ is MSB} \tag{26.8}$$

Figure 26.5 shows
Case I: V_A is connected to non-inverting unit gain op-amp.
Case II: V_A is connected to inverting op-amp

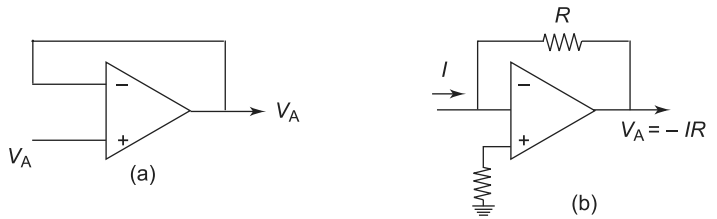


Fig. 26.5 *V_A connected to non-inverting and inverting op-amps*

26.3 ANALOG-TO-DIGITAL CONVERTER (ADC)

It is often required that data taken in a physical system be converted into digital form. Such data would normally be in electrical analog form voltage or current picked up at the output of a transducer (like temperature, pressure, displacement, etc.) or electric voltage or current source. There are various ways in which electrical analog data can be converted to digital form. We shall consider following two methods:

1. The counting ADC
2. The parallel comparator ADC
3. Successive approximation

Counting ADC

This system is shown in Fig. 26.6(a).

The clear pulse resets the counter to the zero count. The counter then records the number of pulses from the clock line in binary form. The clock is the source of pulses equally spaced in time. Since the number of pulses counted increases with time, the binary word representing this count is used as an input to the DAC, whose output is the staircase waveform shown in Fig. 26.6(b). The comparator has an output which is 'HIGH' and the AND gate is open for transmission of clock pulses. When V_d exceeds V_a, the comparator output goes 'LOW' and AND gate is disabled. This stops the counting at the time when $V_a = V_d$ and the counter can be read as the digital output representing analog input voltage.

An improved version of the counting ADC called tracking or servo converter is shown in Fig. 26.7. To understand the operation of the system, assume initially that the output of the DAC is less than the analog

input V_a. Then the positive comparator output causes the counter to read UP. The DAC output increases until it exceeds V_d. The UP-DOWN control line changes state, so that it now counts down and the count decreases by one count. This causes the control to change to UP and the count increases by 1 LSB. This process keeps repeating so that digital output bounces back and forth by ±1 LSB around the correct value. This is also known as *a continuous converter*.

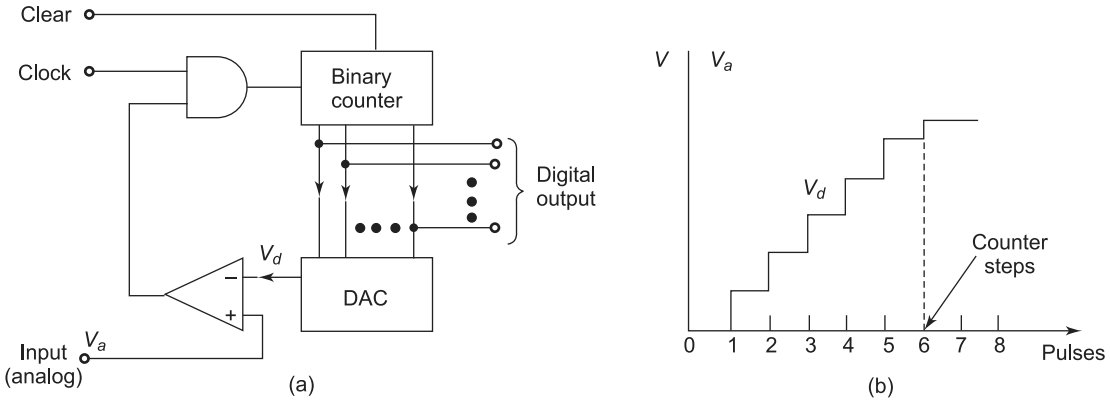


Fig. 26.6 *Counting ADC*

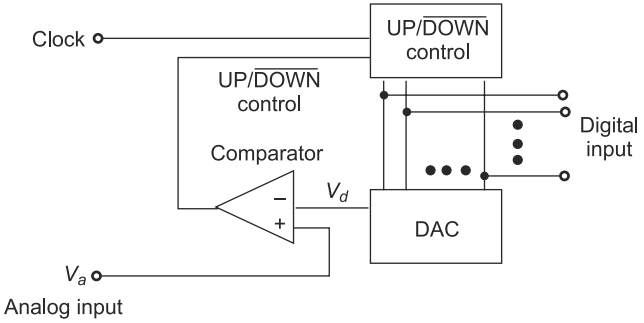


Fig. 26.7 *A tracking ADC*

26.4 SUCCESSIVE APPROXIMATION CONVERTER

The successive-approximation converter is most useful. The block diagram for this type of converter is shown in Fig. 26.8. The converter operates by successively dividing the voltage ranges in half. The counter is first reset to all 0's, and the MSB is then set. The MSB is then left in or taken out (by resetting the MSB flip-flop) depending on the output of the comparator. Then the second MSB is set in, and a comparison is made to determine whether to reset the second MSB flip-flop. The process is repeated down to the LSB, and at this time, the desired number is in the counter. Since the conversion involves operating on one flip-flop at a time, beginning with the MSB, a ring counter may be used for flip-flop selection.

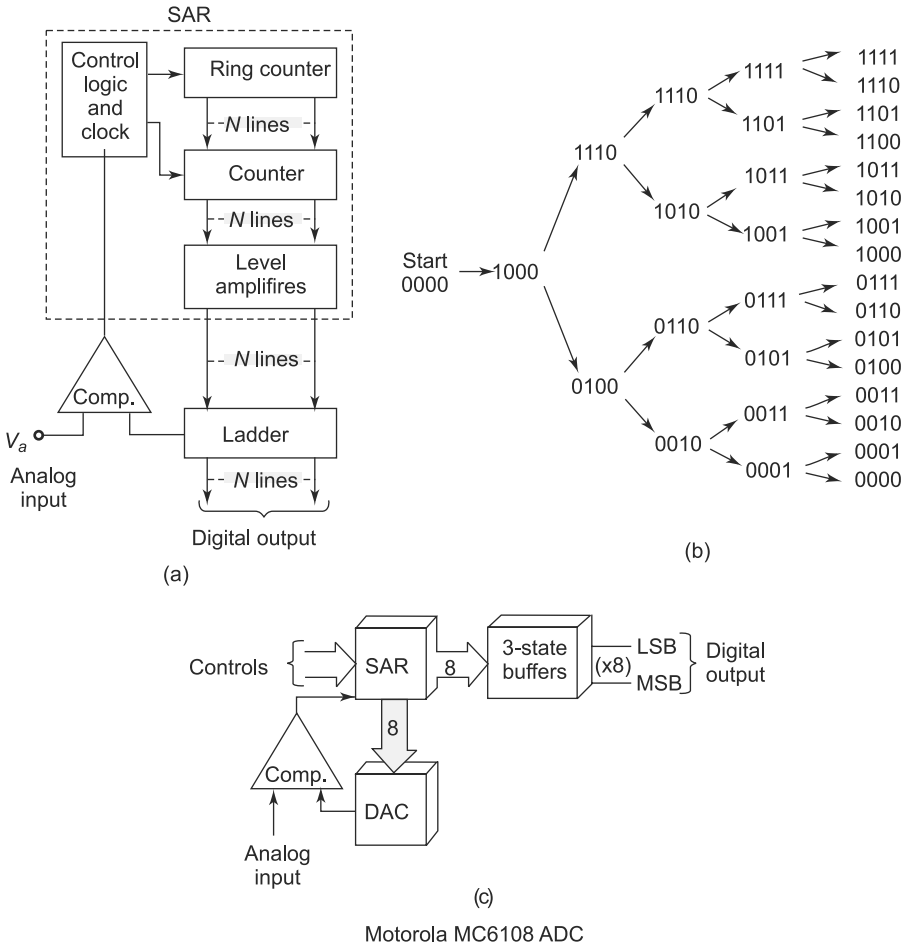


Fig. 26.8 *A/D converter-successive approximation method*

The successive-approximation method thus is the process of approximating the analog voltage by trying 1 bit at a time beginning with the MSB. The operation is shown in diagram form in 26.8. It can be seen from this diagram that each conversion takes the same time and requires one conversion cycle for each bit. Thus, the total conversion time is equal to the number of bits N times the time required for one conversion cycle. One conversion cycle normally requires one cycle of the clock. As an example, a 10-bit converter operating with a 1 MHz clock has a conversion time of $10 \times 10^{-6} = 10^{-5} = 10\ \mu s$.

26.5 COMMERCIALLY AVAILABLE CONVERTERS

D/A Converter

The block diagram with pin numbers is shown in Fig. 26.9.

$$I_{ref} = V_{ref}/R_{ref}$$

The current into the pin 4 is

$$I_0 = I_{\text{ref}} \left[\frac{A_1}{2^1} + \frac{A_2}{2^2} + \cdots + \frac{A_8}{2^8} \right]$$

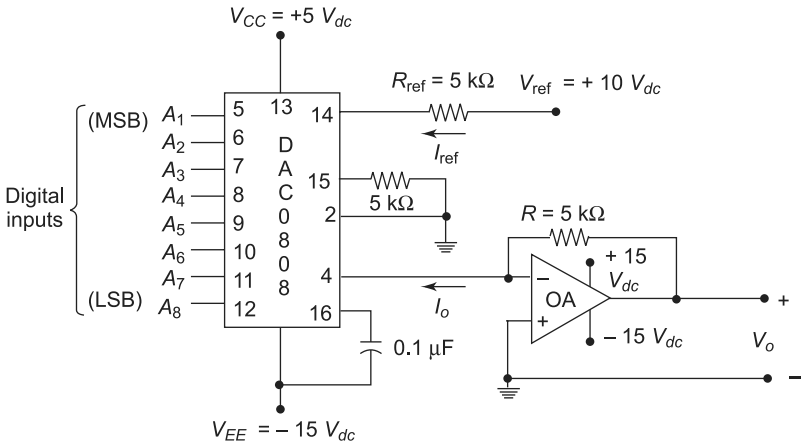


Fig. 26.9 *DAC0808 D/A converter*

The output voltage is

$$V_0 = I_0 R = V_{\text{ref}} \left(\frac{R}{R_{\text{ref}}} \right) \left[\frac{A_1}{2^1} + \frac{A_2}{2^2} + \cdots + \frac{A_8}{1^8} \right]$$

Choosing $R = R_{\text{ref}}$

$$V_0 = V_{\text{ref}} \left[\frac{A_1}{2^1} + \frac{A_2}{2^2} + \cdots + \frac{A_8}{2^8} \right] \tag{26.9}$$

If all $A = 0$, $V_0 = 0$

If all $A = 1$ $V_0 = 0.996\ V_{\text{ref}}$; it does reach V_{ref}

A/D Converter

The ADC0804 is an inexpensive and very popular A/D converter. It is an 8-bit CMOS successive approximation converter, which can digitise 0 V to +5 V dc. Its diagram is shown in Fig. 26.10. The controls can be circuited for continuous conversion-free running mode.

The 10 kΩ resistor and 150 pF establish the operating frequency $f = 1/1.1\ (RC)$. In this case,

$$f = \frac{1}{1.1 \times (10\ \text{k}\Omega)} \frac{1}{(150\ \text{pF})} = 607\ \text{kHz}$$

To begin the operation, the start switch is momentarily activated.

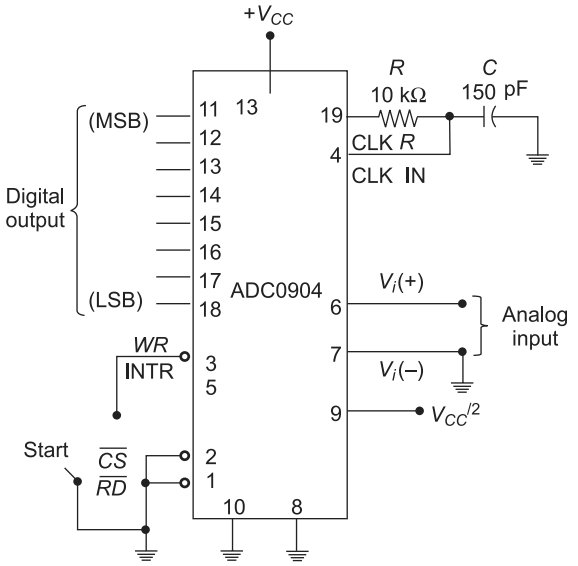


Fig. 26.10 *ADC0804 A/D converter*

26.6 ACCURACY AND RESOLUTION

The accuracy and resolution of D/A and A/D converter are explained here.

Digital-to-Analog Accuracy and Resolution

❑ **Accuracy** It is primarily a function of the accuracy of the precision resistors of the ladder and the precision of the reference voltage supply. Accuracy is a measure of how close the actual voltage is to the theoretical output value.

$$\text{Accuracy} = \frac{\text{Theoretical voltage} - \text{Actual voltage}}{\text{Theoretical voltage}}$$

$$\text{Accuracy (say)} = \frac{10 - (9.9 \text{ or } 10.1)}{10} = 0.01 \text{ or } 1\,\%$$

❑ **Resolution** It is the smallest change in voltage that can be discerned. It is a function of the number of bits and corresponds to voltage change caused by LSD.

For 4-bit input, this is $\frac{1}{16}$ of the input voltage corresponding to LSD. For input voltage of 16 V, it is 1 V. For better resolution, more input bits are needed. For 10-bit input, the resolution is

$$\frac{1}{2^{10}} = \frac{1}{1024}$$

For full-scale output of 10 V, the minimum voltage change is

$$= \frac{10}{1024} \approx 1 \text{ mV}$$

Analog-to-Digital Accuracy and Resolution

An A/D converter is a feedback system. Assuming that the components are precise and function properly; there are two sources of error. These are

- **DAC resolution**, which is determined by LSD weight called *quantising error*.
- **Comparator error**, the output ladder voltage, which causes a variation in switching point. The comparator senses the voltage difference by a small (very) amount before it switches state. Switching is also affected by ripple and noise.

Differential linearity is a measure of variation in step change that causes the DAC to switch state.

The quantising error, ladder error and comparator error may be assumed to be additive. For an 88-bit converter, quantisation error = $\frac{1}{256}$ = 0.4 percent. To achieve an overall accuracy of 1 percent, converter accuracy 0.5 percent, ladder accuracy is 0.1 percent and comparator accuracy of 0.2 percent is acceptable.

Example 26.1

Find the output voltage for a 5-bit ladder that has digital input 10011. Assume 0 to 0 V and input to be +10 V.

Solution Proceeding from MSB to LSB,

$$V_A = 10 \text{ V} \left(\frac{1}{2^1} + \frac{0}{2^2} + \frac{0}{2^3} + \frac{1}{2^4} + \frac{1}{2^5} \right)$$

$$V_A = \frac{10}{2^5}(2^4 + 0 + 0 + 2^1 + 2^0) = \frac{10}{32}(16 + 2 + 1)$$

$$V_A = \frac{10}{32} \times 19 = 5.9375 \text{ V}$$

Example 26.2

An 8-bit A/D converter-type inverter has 500 kHz clock. Find (a) maximum conversion time, (b) average conversion, and (c) maximum conversion rate.

Solution

Counter cycle time = $\frac{10^6}{500 \times 10^3} = 2 \, \mu\text{s}$

Counter advance by 1 count is 2 μs

Maximum counter = $2^8 = 256$

(a) Maximum conversion time = $256 \times 1 = 512 \, \mu\text{s}$

(b) Average conversion time = $\frac{1}{2} \times 512 = 256 \, \mu\text{s}$

(c) Maximum conversion rate = $\frac{10^6}{512} = 1953$ conversions/s

Example 26.3

What is the resolution of a 9-bit D/A which uses ladder network? Express it as percent. What is the resolution in volts if the full-scale converter output is 10 V?

Solution The LSB in a 9-bit system has a weight of $\frac{1}{2^9} = \frac{1}{512}$. Thus, the resolution is 1 part in 512; as a percent $\frac{100}{512} = 0.2$. Resolution in voltage

$$= \frac{10}{512} \times 10^3 = 20 \text{ mV}$$

Example 26.4

What is the quantising error of a 10-bit A/D converter? What overall accuracy do you expect if the analog part error is 0.1 percent?

Solution Quantising error corresponds to LSD = $\frac{1}{2^{10}} = \frac{1}{1024} \approx 0.1$ percent

Analog part accuracy = 0.1 percent
Expected overall accuracy = 0.1 + 0.1 = 0.2 percent

Example 26.5

Consider the residue divider of Fig. 26.11; determine V_A, the node voltage.

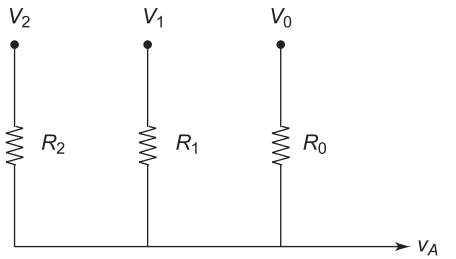


Fig. 26.11

Solution Sum of nodal current is

$$(V_0 - V_A)/R_0 + (V_1 - V_A)/R_1 + (V_2 - V_A)/R_2 = 0$$

or $$\frac{V_0}{R_0} + \frac{V_1}{R_1} + \frac{V_2}{R_2} = V_A \left(\frac{1}{R_0} + \frac{1}{R_1} + \frac{1}{R_2} \right)$$

or $$V_A = \frac{V_0/R_0 + V_1/R_1 + V_2/R_2}{1/R_0 + 1/R_1 - 1/R_2}$$

This result follows directly by application of *Millman's theorem* which states that the node voltage is obtained by the sum of currents entering the node, assuming node voltage to be zero decided by the sum of conductances connected to the node.

Example 26.6

How can the output voltage V_A be made to represent the binary number $b_2b_1b_0$?

Solution

Let $R_1 = R_0/2$. $R_2 = R_0/4$
$V_0 = b_0V$, $V_1 = b_1V$, $V_2 = b_2V_1$; b's can be 0 or 1.
We can then write

$$V_A = \frac{V(2^0 b_0 + 2^1 b_1 + 2^2 b_2)/R_0}{\frac{1}{R_0}(2^0 + 2^1 + 2^2)}$$

$$V_A = V\left[\frac{2^0 b_0 + 2^1 b_1 + 2^2 b_2}{(2^3 - 1)}\right]$$

Or, in general,

$$V_A = V\left[\frac{(2^{N-1}b_{N-1} + \cdots + 2^1 b_1 + 2^0 b_0)}{(2^N - 1)}\right] \tag{26.10}$$

Example 26.7

In a resistor divider of 6 bits, what is the weight of each bit?

Solution

$$N = 6(2^{N-1}) = 2^6 - 1 = 63$$

The weights of 6 bits are

$$\underset{0}{\frac{1}{63}}, \underset{1}{\frac{2}{63}}, \underset{1}{\frac{4}{63}}, \underset{1}{\frac{8}{63}}, \underset{0}{\frac{16}{63}}, \underset{1}{\frac{32}{63}}$$

Summary

- A/D and D/A converters are introduced with their functional diagrams.
- Their accuracy and resolution with examples are discussed.

Exercises

Review Questions

1. Distinguish between weighted resistor DAC and *R*-2*R* ladder DAC. What is preferred and why?
2. What is the purpose of a level amplifier in DAC?
3. Draw the block diagram of the DAC of Fig. 26.4. Briefly explain its operation.
4. What are the various types of A/D converters? Which is the fastest? What limits its use?
5. What is a parallel ADC? How many comparators does this need? How is the comparator output converted to digital form?
6. Compare successive-approximation A/D converter, with counter-type converter. Which requires less conversion time and why?
7. What determines the resolution of a D/A counter?
8. What is meant by quantising error in a A/D converter?

Problems

1. Draw the schematic of a 6-bit resistor divider. If the divider has a full-scale output of +10 V, find the following:
   (a) Change in output due to change in LSB
   (b) The output voltage for an input of 1001110
2. What is the full-scale output of 6-bit binary ladder if 0 = 0 V and 1 = +10 V? What is the output for input of 110001?
3. A 12-bit D/A converter has full-scale output of 10 V. What are its percent resolution and voltage resolution?

4. Find the following for a 12-bit converter-type ADC using a 1 MHz clock:
   (a) Maximum conversion time
   (b) Average conversion time
   (c) Maximum conversion rate
5. What is the full-scale output of an *R*-2*R* ladder for
   (a) 2-bit number (b) 5-bit number
   Hint: Take 0 = V and 1 = +10 V
6. What is the output of an *R*-2*R* ladder for the following 4-bit input patterns?
   (a) 1010 (b) 0101
   Hint: Take $R_F = 3R$, 0 = +0 V, 1 = +10 V
7. What clock frequency must be used with an 8-bit counter-type A/D converter which can make 5000 conversions per second?
8. What is the conversion time of a 12-bit successive-approximation-type ADC using a 1 MHz clock?

Multiple-Choice Questions

1. An 8-bit converter is used for a dc range of 0 to 10 V. Find the weight of LSB.
   (a) 39 mV (b) 78 mV (c) 39.2 mV (d) None of these
2. A successive-approximation A/D converter has a resolution of 20 mV. What will be its digital output for an analog input of 2.17 V?
   (a) 01101100 (b) 01101101 (c) 01101011 (d) None of these
3. An analog transducer has a range of 0–10 V. Calculate bits of an ADC if the resolution is 5 mV.
   (a) 10 (b) 9 (c) 11 (d) None of these
4. A 0–10 V ADC has to have a resolution of 0.025%. Find the rms value of quantisation error.
   (a) 176 μV (b) 352 μV (c) 705 μV (d) 1410 μV
5. A 5-bit DAC has a current output. The digital input is 10100 and the output current corresponding to this is 10 mA. What will be the output current for digital input 11101?
   (a) 10.5 mA (b) 29 mA (c) 14.5 mA (d) None of these

Fill in the Blanks

1. The resolution of a 12-bit D/A converter is _____ of the full-scale output.
2. The maximum quantising error for an A/D converter is _____ of maximum analog input voltage.
3. The number of comparators required for an 8-bit parallel comparator A/D converter is _____.
4. The linearity of a D/A converter is specified as _____LSB.
5. The maximum sampling time T_s of a 10 kHz sinusoidal voltage for conversion to digital form is _____.

Answers

Problems

1. (a) $\frac{10}{63}$ V, (b) $\frac{10}{63}(2 + 4 + 8 + 32)$ 2. 9.844 V, 7.656 V
3. $\frac{1}{4096}$ or 0.0244%. 2.44 mV 4. (a) 4.096 ms, (b) 2.078 ms, (c) 2.44 s
5. (a) –7.5 V, (b) –9.6875 V 6. (a) = 5.25 V (b) -3.125 V
7. 1.28 MHz 8. 12 μs

Multiple-Choice Questions

1. (a) 2. (a) 3. (c) 4. (c) 5. (c)

Fill in the Blanks

1. 1/4095 2. 1/510 3. 255 4. Less than $\pm\frac{1}{2}$ 5. 0.05 ms

Transducers

chapter 27

Goals & Objectives

- Mechanical transducers
- Passive electrical transducers
- Active electrical transducers

27.1 INTRODUCTION

A transducer is a device or combination of elements, which responds to the physical condition or chemical state of a substance and converts it into an output signal. The output signal may be an electrical or mechanical parameter, which can be easily measurable. If a transducer produces mechanical-nature signal as its output then it is called a *mechanical transducer*. The transducers that produce electrical signals as output are called *electrical transducers*. Sometimes two transducers connected in cascade may produce an electrical quantity in the output terminals as shown in Fig. 27.1.

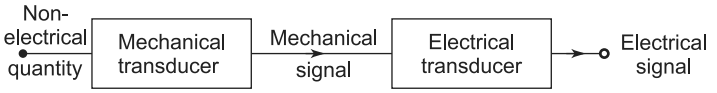


Fig 27.1 *Transducers connected in cascade*

A *sensor*, or primary sensing element, is the first element, which is not directly coupled to the system under examination. A transducer may be considered to have accomplished the function of measurement by drawing an insignificant amount of power and energy from the system under study whereas a sensor does it by standing away without getting into physical contact with the medium or system under examination. Intensity and luminance of a source may be measured by sensors, whereas temperature is measured by transducers.

Based on the role of transducers, it can be classified into input and output transducers. An input transducer can be used as a measurement device and is known as an *instrument transducer*. An output transducer is known as a *power transducer*; it delivers output signals like force, torque, pressure or displacement when the electrical signal is applied as an input.

Based on the operation, transducers are classified into active and passive transducers. *Active transducers* develop the voltage and current as the output signal from the physical quantities being measured. But external energy is required for *passive transducers* to create the electrical output signals.

Thermo-couple, piezoelectric transducers, photoelectric cell and photovoltaic cell are the examples of the active transducer. Resistance strain gauge, thermistor, Linear Variable Differential Transformer (LVDT), Hall Effect sensor and photomultiplier tube are the examples of passive transducers.

Transducers should have satisfactory static and dynamic characteristics. The accuracy, precision, repeatability, reproducibility, stability, sensitivity and linearity are the steady-state characteristics. Dynamic error, fidelity, bandwidth and speed of response are the dynamic performance characteristics.

27.2 MECHANICAL TRANSDUCERS

Mechanical quantities like temperature, pressure, flow, density, speed, velocity, acceleration, *altitude* and distance are the most important quantities to be controlled in any industry. Accuracy of the control of the above quantities is not possible without the accuracy of measurement. Table 27.1 lists transducer with the mechanical quantities to be measured.

Table 27.1 *Mechanical transducers*

Mechanical quantity to be measured	*Transducer*
Temperature	• Bimetallic element
Pressure	• Metallic diaphragms
	• Bourdon tubes
Force	• Spring balance
	• Cantilever
	• Diaphragms
	• Hydraulic load cells
Torque	• Torsion bar
	• Flat spiral springs
	• Gyroscope
Density	• Hydrometer
	• U-tube weighting system
Liquid level	• Float elements
	• Manometer
Viscosity	• Capillary tube
Flow rate	• Pilot rube
	• Rotating wave system
Displacement	• Flapper nozzle system
Vehicle attitude	• Gyroscope

A **transducer** is a device that converts a signal in one form of energy to another form of energy. The term *sensor* should be distinguished from *transducer*. The latter is a converter of one type of energy into another, whereas the former converts any type of energy into *electrical*. Transducers are widely used in measuring instruments.

The mechanical transducers are the mechanical elements that are used for converting one form of energy into other form that can be measured easily.

Strain Gauge

If a resistor of fine wire is distorted then its resistance changes as a result of dimensional change. The result is a resistor for which the resistance is related to strain. Such a device is called a strain gauge. Strain gauges find extensive use in mechanical and biological measurements. Often the fine wire is attached to some flexible insulating substrate such that, when the substrate is flexed the actual wire itself is also flexed. Some strain gauges are made by depositing thin metal film directly onto the substrate. Since the resistance change is usually a very small fraction of the total resistance, it is very important to use a very sensitive resistance measurement technique. A second difficulty is that, small changes in temperature of the gauge can

masquerade as a change in strain. One most often uses a Wheatstone bridge configuration with a temperature controlled strain gauge in order to maximize the sensitivity of the measurement.

There are two main types of Displacement Sensors. Linear Variable Differential Transformer (LVDTs) are beautiful devices that can detect motion and position with incredible sensitivity and linearity. The second type is a capacitive position sensor – this device has a smaller dynamic range than the LVDT but has even higher sensitivity. LVDT's internal structure consists of a primary winding centered between a pair of identically wound secondary windings, symmetrically spaced about the primary. The coils are wound on a one-piece hollow form of thermally stable glass reinforced polymer, encapsulated against moisture, wrapped in a high permeability magnetic shield, and then secured in cylindrical stainless steel housing. This coil assembly is usually the stationary element of the position sensor. The moving element of an LVDT is a separate tubular armature of magnetically permeable material called the core, which is free to move axially within the coil's hollow bore, and mechanically coupled to the object whose position is being measured. This bore is typically large enough to provide substantial radial clearance between the core and bore, with no physical contact between it and the coil. In operation, the LVDT's primary winding is energized by alternating current of appropriate amplitude and frequency, known as the primary excitation. The LVDT's electrical output signal is the differential AC voltage between the two secondary windings, which varies with the axial position of the core within the LVDT coil. Usually this AC output voltage is converted by suitable electronic circuitry to high level DC voltage or current that is more convenient to use. As an alternative, to avoid the use of magnetic materials one can place the primary coil on the moving object with the two secondary fields picking up its driving field.

There are number of mechanical transducers, some of the commonly used ones are described below.

❑ **Bellows** These are the elastic elements, that convert the air pressure into displacement and it is commonly used for the measurement of pressure.

❑ **Bourdon Tube** This elastic tube converts air pressure to the rotary motion of the pointer used to indicate the pressure.

❑ **Spring** The spring tends to expand when force is applied to them; thus they are used for the measurement of force.

❑ **Proving Rings** Like the springs, the proving rings also convert applied force to the displacement.

❑ **Diaphragm** It converts applied pressure to the displacement.

❑ **Manometer** The manometer converts the applied pressure into variable displacement of the liquid within it, enabling to measure the pressure.

❑ **Thermocouple** Thermocouple is the devise that produces electric current when one of its end is heated. The current produce by the device can be measured, which can be calibrated against the temperature enabling us to measure the temperature of the body.

❑ **Bimetals** These are the bimetallic strips comprising of two different metals having different coefficient of thermal expansion, joint together. When the strip is heated, one metal expands lesser while the other metal expands more leading to the deflection of the bimetallic strip, which is converted into the rotary motion of the pointer that indicates the temperature.

❑ **Hydropneumatic Transducers** These include devices like orifice, venturi, pitot tube, vanes and turbines that are used for measurement of pressure, velocity, flow rate and force of water.

Apart from the mechanical transducers mentioned above there are many others like seismic mass, pendulum scale, float etc. Most of the mechanical transducers are used as the primary transducers, meaning the initial input is applied to them, while the output obtained from them can be used directly to measure the quantity or it can be given as input to the secondary transducer, which are mostly of electrical type.

27.3 PASSIVE ELECTRICAL TRANSDUCERS

The three passive elements in an electric circuits are resistor, inductor and capacitor. The transducers that are based on the variation of the parameters due to application of any external stimulus are known as passive transducers.

Resistive Transducers

The dc resistance R can be given by

$$R = \frac{\rho l}{a} \tag{27.1}$$

where l = conductor length in m
a = area of cross section in m^2
ρ = specific resistivity in Ω-m

Change in the value of the resistive element can be brought about by subjecting the element to external stimulus that affects either dimensions of the element or its resistivity. The dimensional changes can be brought about by subjecting the resistive elements, to pressure, force or torque, directly or by means of some primary transducers. Resistive strain gauges enable measurement of strain of mechanical members on to which they are bonded. The resistivity of the material medium constituting the path of the current in the resistor varies with the temperature and composition of the medium. Resistance thermometers are known to be exceptionally good for temperature measurements.

27.3.1 Resistance Thermometers

In this, the temperature changes are measured in terms of resistance changes. The resistive element is usually made of a solid material, a metal, metallic alloy or a semiconductor compound. The resistivity of the metal increases with temperature, but in semiconductors and insulators generally decreases.

Wire-wound elements employ considerable length of wire, and it is free to expand. The length also increases with increase in temperature. Hence, as temperature changes, the change in resistance will be due to changes, in both length and resistivity. The temperature coefficient of resistance, is given by

$$\alpha = \frac{1}{\Delta T} \cdot \frac{\Delta R}{R_0} \tag{27.2}$$

ΔT = change in temperature, °C
$\Delta R/R_0$ = fractional change in resistance
R_0 = resistance at 0°C

The resistance R_T at any other temperature T°C is given by $R_T = R_0(1 + \alpha T)$ (27.3)

The wire resistance thermometers as shown in Fig. 27.2 usually consist of a coil wound on a mica or ceramic former, which also serves as a support mount for the coil. This element is normally enclosed in a protective tube of pyrex glass, porcelain, quartz or nickel. The element is brought to contact with the fluid whose temperature is to be measured. The two terminals of the Platinum wire is connected with Wheatstone bridge for measuring the change in resistance and so the temperature is measured [Eq. (27.3)].

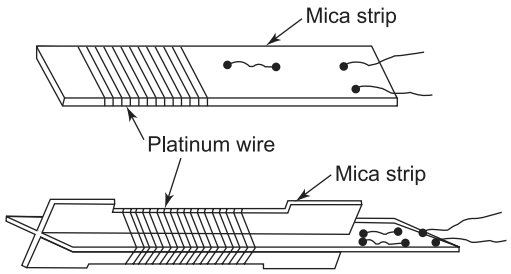


Fig. 27.2 *Resistance thermometer*

Thermistor

It is a two-terminal semiconductor slab whose resistance decreases with increase in temperature, unlike a metal. Materials employed are oxides of cobalt, nickel, copper, iron, uranium and manganese.

A thermistor has very high negative coefficient of temperature 3–5% per °C, ideal for temperature measurement. Its resistance can be empirically expressed as

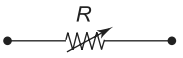
$$R = R_0 \exp\beta\left(\frac{1}{T} - \frac{1}{T_0}\right) \tag{27.4}$$

where R_0 = resistance at T_0 (k)
R = resistance at T(k)
β = constant to be determined experimentally

For large values of T, we can approximate as

$$R = R_0 \exp\left(\frac{\beta}{T}\right)$$

❑ Symbol



Parameters of Interest

- **Time constant**—Time, for resistance to fall to 63% of the final value; Range: 1–50 s
- **Dissipation factor**—Power dissipated in watts/°C temperature; Range: 1–10 mW/°C
- **Resistance ratio**—R(20°C)/R(125°C): Range: 3–60

Application

Measurement of

1. Temperature
2. Flow and pressure
3. Liquid level
4. Voltage and power
5. Vacuum
6. Thermal conductivity

Resistive Displacement Transducers

The simplest form of converting linear or angular displacement into a change of resistance is the resistive element provided with a movable contactor. The change in resistance is brought out by only a change in length or portion of the resistor from one end to the point of contact. The transducer of resistance *Rp* is usually energised by dc or ac supply, and electrical output signals are obtained by using simple electrical circuits shown in Fig.27.3. For angle measurement, the resistor elements is in circular form and the contactor is rotable as shown Fig. 27.3(a). Various other way of measuring x or θ are shown in Fig. 27.3(b), (c) and (d).

Resistive Strain Transducer

Strain-gauge pressure transducers and strain-gauge accelerometers are employing strain gauges as the secondary element along with a suitable primary mechanical transducer for converting the basic quantity under measurement into stress. The resistances wire strain gauges are available in two forms: unbonded-type and bonded-type systems. They employ four sapphire posts and hold four equal lengths of tungsten-platinum

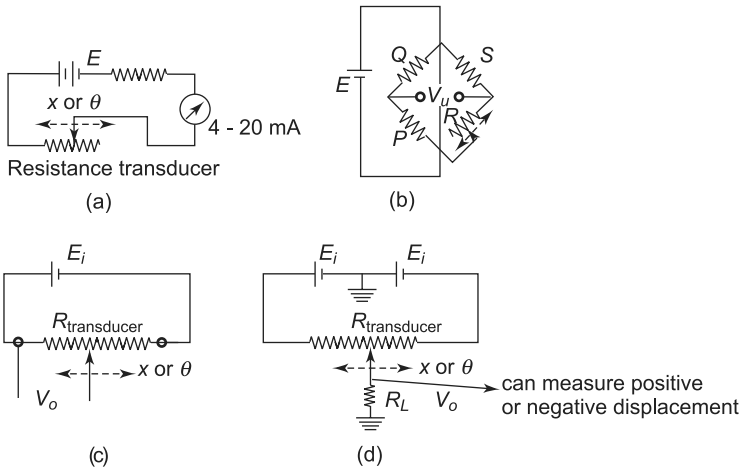


Fig. 27.3 *Resistance transducer and its different circuits*

wire of 5 μm diameter, which are common as the four wires can form a Wheatstone bridge circuit providing temperature compensation. The four posts as shown in Fig. 27.4 are mounted on a star spring structure. When the centre of the star spring is subjected to the force under measurement, the star spring flexes, with each pair of the strain-gauge elements on opposite sides going into strain of opposite polarity. The resulting unbalance voltage of the bridge circuit is proportional to the force and hence, the pressure on the diaphragm. The whole assembly is encased in housing with provisions for admission of pressure and for electrical connections.

The bounded-strain transducer is used for stress analysis. The pressure transducer uses a variety of sensing devices to provide an electrical output proportional to applied pressure. The sensing device employed in the transducer under discussion is bonded, metal-foil strain gauges.

While designing a strain-gauge pressure transducer, two fundamental considerations are kept in mind—one is the mechanical pressure-sensing element and the other is the electrical strain gauge bridge. The sensing element is typically a diaphragm or tube whose internal volume contains applied pressure. The fluid pressure causes the element to deflect in a predictable manner causing surface strains as well as applied force. The strain gauge is bonded to the non-pressurised face of the sensing element and responds to the surface strains or the strain gauge can be bonded to a separate structure usually a cantilever beam, driven by the force input of the diaphragm.

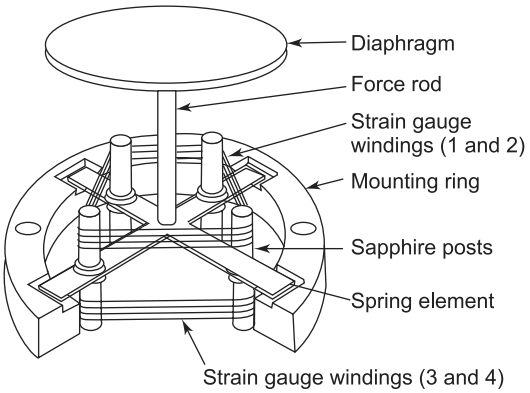


Fig. 27.4 *Unbonded-type pressure-measurement transducers*

27.3.2 Inductive Transducers

In this, the self-inductance of a coil or mutual inductance of a pair of coils is altered in value due to a variation in the value of the quantity under measurement. This type of transducers posses considerable sensitivity and scope of application, especially for displacement and thickness measurements.

Linear Variable Differential Transformer (LVDT)

The LVDT is based on mutual inductance type with variable coupling between the primary and the two secondary coils. It consists of a primary coil, uniformly wound over a certain length of the transducer, and two identical secondary coils symmetrically wound on either side of the primary coil and away from the centre as shown in Fig. 27.5(a). The iron core is free to move inside the coil in either direction from the central (null) position. When the primary is excited by ac supply, the secondary emfs are equal to each other with the core lying in the central position. The secondaries are connected in series but in phase opposition so that the net voltage is zero. Displacement of the core in either direction from the centre position results in output voltages proportional to displacement but of opposite polarity. See Figs 27.5(a) and (b).

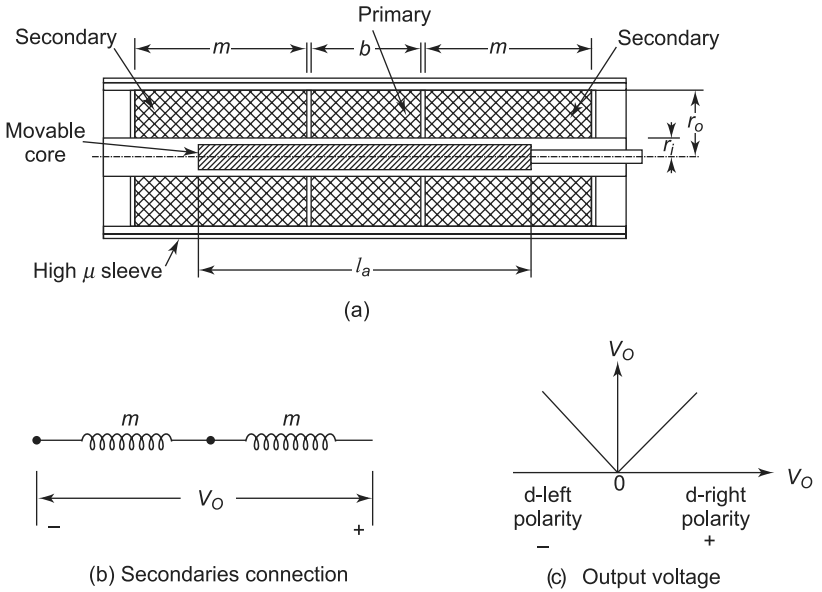


Fig. 27.5 *Linear Variable Differential Transformer (LVDT)*

27.3.3 Capacitive Transducers

It is a non-loading, non-contact and non-invasive type of transducer for displacement measurements. Capacitive transducers are also known as *proximity transducers*. They measure the nearness of an object without any mechanical coupling between them. The only coupling is through the electrostatic forces of attraction between the object and one plate of the capacitor.

The capacitance is given by

$$C_0 = \varepsilon_0 \varepsilon_r A/d \tag{27.5}$$

ε_0, ε_r = absolute and relative permittivity, respectively
A = area of the plate in m^2
d = separation between the plates in m

Proximity Transducers

In some applications, the proximity of an object with respect to the fixed plate of the transducers is desired. Electrical circuits that develop output voltages proportional to the separation between the plates are available. This transducer giving an output signal ρ_0 proportional to x_0 is shown in Fig. 27.6. The output signal ρ_0 is given by

$$\rho_0 = \frac{C_f x_0}{\varepsilon_0 A} E_m \sin \omega t \tag{27.6}$$

C_f = capacitance of the standard capacitor
$E_m \sin \omega t$ = sinusoidal applied voltage

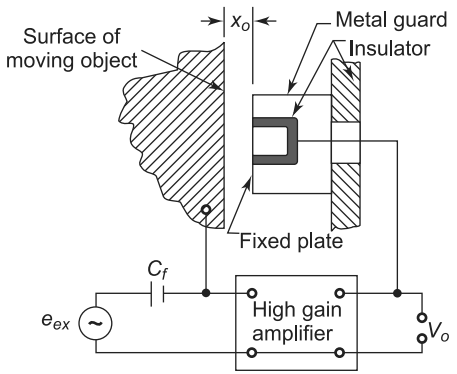


Fig. 27.6 *A proximity transducer with signal processing circuit*

If the object is vibrating, the amplitude of vibrations can be measured and in such a case, ρ_0 is an amplitude-modulated wave. Capacitor transducers can also be used for displacement, strain, pressure, microphone, level, moisture measurement, etc.

27.4 ACTIVE ELECTRICAL TRANSDUCERS

Thermocouples and piezoelectric crystals are the popular examples of active transducers.

27.4.1 Thermoelectric Transducers

It converts thermal energy into electric energy. Three phenomena which govern the behaviour of a thermocouple are the Seebeck effect, the Peltier effect and the Thompson effect.

Seebeck Effect

If two wires of different metals joined together form two junctions and if the two junctions are different temperatures, an electric current will flow round the circuit. The current flows across the hot junction from the former to the latter metal of the following series:

Bi – Ni – CO – Pd – Pt –
U – Cu – Mn – Ti – Hg – Pb–
Sn – Cr – MO – Ph – Ir – Au – Ag –
Zn – W – Cd – Fe – As – Sb – Te

If metal *A* is of copper and metal *B* is of iron then the current flows from copper to iron at the hot junction and from iron to copper at the cold (reference) junction as shown in Fig. 27.7(a). The Seebeck emf depends on the difference in the temperature of the two junctions.

Peltier Effect

It is the reverse phenomenon of Seebeck effect. An external emf is connected as shown in Fig.27.7(b) and a current is forced through the junctions. It is observed that heat is absorbed when the current flows across iron-copper if the flow of current is reversed. The amount of heat liberated or absorbed is proportional to the quantity of electricity that crosses the junction and the amount of heat liberated or absorbed when one ampere passes for a second is called the Peltier coefficient.

Thompson Effect

It is also the reversible heat flow effect and involves the contribution of Seebeck emf in the wire of the same metal, if a temperature difference existed within that particular conductor. When a current flows through a copper conductor having a thermal gradient along its length, heat is liberated at any point where the current is in the same direction as the heat flow, while heat is absorbed at any point where these metals are replaced. In iron, heat is absorbed at any point when the current flows in the direction of heat flow, while heat is liberated, when the current flows in the direction opposite to the flow of heat.

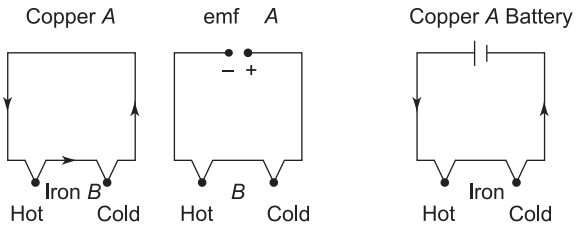


Fig. 27.7 *(a) Seebeck effect (b) Peltier effect*

27.4.2 Piezoelectric Transducers

It converts mechanical energy into electrical energy and are based on the direct piezoelectric effect observed in certain nonmetallic and insulating dielectric compounds. Electrical charge is developed on the surface of the crystals, when they are under mechanical strain due to application of stress. Piezoelectric transducers are having high mechanical rigidity so it is used to measure force, pressure, acceleration, torque, strain and amplitudes of vibration. And it is smaller in size, high natural frequency, linearity, high sensitivity, wide measuring range and polarity sensitivity. The basic piezoelectric phenomenon is the effect of force applied in longitudinal and transverse directions. The charge sensitivity or piezoelectric *d*-coefficient is the charge developed per unit force. The three modes of operations are thickness expander mode, length expander mode and volume expander mode. These modes are based on the direction of force applied which is to be measured. The materials exhibiting the piezoelectric phenomenon are quartz, Rochelle salt, tourmaline, Ammonium Dihydrogen Phosphate (ADP), Lithium Sulphate (LS) and Di Potassium Tartrate (DKT). Figure 27.8 shows the piezoelectric crystal wafer used as transducer.

The net piezoelectric effect is represented by the vector of electric polarisation $\overline{P}$ as

$$\overline{P} = \overline{P}_{xx} + \overline{P}_{yy} + \overline{P}_{zz} \tag{27.7}$$

where $\overline{P}_{xx}$, $\overline{P}_{yy}$, $\overline{P}_{zz}$ refer to the effect on the face perpendicular to each axis due to the application of stresses.

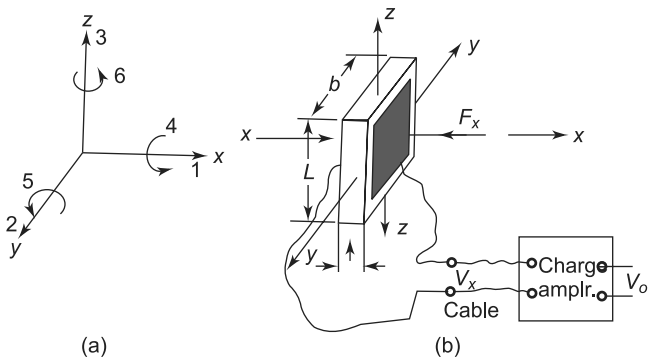


Fig. 27.8 *Piezoelectric transducer*

27.4.3 Photoelectric Transducers

A photoelectric transducer is based on the effects of physical radiation on matter. If light energy interacts with an electron bound in a metal surface, the entire quantum energy is converted into kinetic energy of the electron. This kinetic energy helps the electrons to move and contributes current in the metal. This is called photoelectric effect, i.e. the effect of visible radiation on the metal (In semiconductor also it is possible). The photo-emissive, photovoltaic, and photoconductive (resistive) are the different forms of photoelectric effects.

Metallic cathode and an anode in an evacuated tube is the main part of photo-emissive transducers. The emitted electrons from cathode are attracted towards the anode, which causes the current flow proportional to the amount of light fallen. The photocurrent depends on the wavelength of the radiation and the material of the surface. The effect of the optical radiation on the semiconductor may be observed as a change in either current, developed voltage or resistance. Photovoltaic cells are self-generating and are favoured for use in exposure meters. Photoresistive cells are passive and the change in the resistance value according to the illumination of light should be measured by suitable circuitry. It is known as Light Dependent Resistor (LDR). Photodiodes and photo transistors are considered to function in both the photo-emissive and photovoltaic modes.

27.4.4 Hall-Effect Transducers

This is one of the galvanomagnetic phenomena in which the interaction between the magnetic field and moving electrical charges results in the development of forces that alter the motion of the charge. This is very much prominent in semiconductor materials. A thin strip of bismuth or *N*-type germanium is subjected to magnetic field *B* normal to its surface as shown in Fig.27.9 while it carries a current *I* along the length of the strip, but normal to *B*. Because of the force from magnetic field the electrons move towards the edges of the strip with a velocity *V*. So the edge surfaces act like charged electrodes and potential difference between two edges known as Hall potential. E_h is proportional to B and *I*. It is suitable for measurement of magnetic field. The important application is, this transducer has made it possible to measure dc and ac currents in a conductor without interruption of the circuit and without making any electrical contact with the conductor.

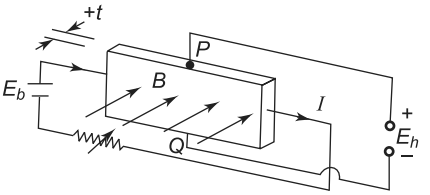


Fig 27.9 *Hall-effect transducer*

Summary

- Various types of transducers have been explained in this chapter.
- Their importance, different types with applications have been discussed.

Exercises

Review Questions

1. What is a transducer?
2. Distinguish between active and passive transducers.
3. What is a resistance thermometer?
4. Explain the resistance displacement transducer. Draw the circuit for measuring positive and negative displacement?
5. Explain the working of LVDT.
6. Explain what is Hall effect and its application?
7. Explain the principle of peizoelectric transducer. What are its applications?
8. What is proximity transducer? Can it be used for a vibrating object?
9. Explain Seebeck effect and Peltier effect with diagrams.
10. What is a electric transducer. What are its different forms?
11. Name the transducers for temperature measurement?
12. What are the quality characteristics of a transducer?
13. Distinguish between static and dynamic characteristics of an transducer.
14. Why are the transducers increasingly getting popular?
15. List the problems encountered while measuring small displacement by a capacitive transducer.
16. Explain the transformer type transducers with its working.
17. Discuss the application of piezoelectric effect and materials.
18. Differentiate the photovoltaic, photo-emissive and photoconductive transducers.

Multiple-Choice Questions

1. Which one of the following is an active transducer?
   (a) Strain gauge (b) Thermistor
   (c) Photovoltaic cell (d) Photo-emissive cell
2. A transducer has an output impedance of 1 kΩ and a load resistance of 1 MΩ, the transducer behaves as
   (a) a constant current source (b) a constant voltage source
   (c) a constant power source (d) none of the above
3. In a transducer, the observed output deviates from the correct value by a constant factor the resulting error is called
   (a) zero error (b) non confirmatory error
   (c) sensitivity error (d) hysteresis error
4. Unbounded strain gauges are
   (a) exclusively used for transducer application
   (b) exclusively used for stress analysis
   (c) commonly used for both transducer application as well as for stress analysis
   (d) none of the above

5. In wire-wound strain gauges, the change resistance on application of strain is mainly due to
   (a) change in length of wire
   (b) change in diameter of wire
   (c) change in both length and diameter
   (d) change in resistivity.
6. In an LVDT, the core is made up of a
   (a) non-magnetic material
   (b) a solid ferro-electric material
   (c) high permeability, nickel-iron hydrogen annealed material in order to produce low harmonics, low null voltage and high sensitivity. The core is slotted to reduce eddy current losses.
   (d) all of the above
7. An LVDT
   (a) exhibits linear characteristics upto a displacement of ±5 mm
   (b) has a linearity of 0.05%
   (c) has an infinite resolution and a high sensitivity which is of the order of 40 V/mm
   (d) all of the above
8. What is the minimum displacement that can be measured with capacitive transducer?
   (a) 1 cm (b) 1 mm (c) 1 μm (d) 1×10^{-12} m
9. A Hall-effect transducer can be used for measurement of
   (a) power
   (b) displacement
   (c) current
   (d) all of the above
10. A photoconductive cell is used for
   (a) high-frequency application
   (b) low-frequency application
   (c) medium-frequency application
   (d) all of the above

Answers

Multiple-Choice Questions

1. (c) 2. (b) 3. (c) 4. (a) 5. (c)
6. (c) 7. (d) 8. (c) 9. (d) 10. (b)

Basics of Computers

chapter 28

Goals & Objectives

- Introduction to basic computers and generation of computers
- Classification of various types computers and their hardware and software specifications
- Discussion of communication packages and development tools
- Explanation of data communication, computer network and emerging technologies in computing
- Introduction of next-generation computing paradigm

28.1 INTRODUCTION

Today computers are influencing every sector and the impact has been nowhere been more revolutionary than in electrical engineering. The use of computers has improved our life at work and at home in contrast to our ancestors in the primitive stages of civilisation, who were using their fingers and pebbles for computing purposes. The need for performing lengthy and complex calculations led to the invention of first a variety of calculators, and then finally to computers. In the simplest words, a computer is an electronic machine with capabilities of performing calculations and controlling operations. These operations are performed with the help of instructions (collectively known as a program) to process the given set of data in order to achieve desired results (known as information). Today, computers are an inseparable part of our day-to-day lives—in our workplaces, homes, automobiles, appliances, etc. In fact, the application domain is limited only by human creativity and imagination. The landscape of applications include education, industry, government, medicine, scientific and engineering research, defence, business, commerce, law and even music, arts and sports. The major characteristics that makes computers an essential part of our lives include speed, accuracy, reliability, storage capability, versatility and diligence. Perhaps and except, the lone major limitation to overcome that remains is a computer can only perform what it is programmed to do. The Electronic Numeric Integrator and Calculator (ENIAC), developed in 1946 by John Eckert and John Mauchly at the University of Pennsylvania, embodied almost all the components and concepts of today's high-speed, electronic digital computers. In the related development, the Electronic Discrete Variable Automatic Computer (EDVAC) was first developed to use the stored-program concept introduced by John von Neumann. However, the world's first stored-program, electronic digital computer, successfully executed its first program on 21st June 1948. Initially, it was called the "Small Scale Experimental Machine", but was soon nicknamed the "*Baby Computer*". It is also sometimes known as the "Mark 1 prototype". The Baby machine had a 32-bit word length, a memory of 32 words extendable up to 8192 words and a speed of around 1.2 milliseconds per instruction.

The above developments led to the recognition of the computer as an independent discipline. Subsequently, Software Engineering was recognised as an independent discipline in 1968. Both these disciplines remain much younger and are still evolving unlike core engineering. UNIVAC (Universal Automatic Computer) became the first general-purpose and commercially available computer, which was capable of handling numeric and textual information. Since early days Indians have immense contributions to computing disciplines. India commissioned its first digital computer named 'TIFRAC (Tata Institute of Fundamental Research Automatic Calculator) in 1956 just after 4 years commissioning of UNIVAC in the US. Today, India occupies a unique position in computing and information technology with the potential to lead the world in the era of knowledge economy.

28.2 GENERATION OF COMPUTERS

According to the kind of processor installed in a computer, there are five generations (or stages) of technological development or innovation. The first-generation computers (1940–1956) were built using vacuum tube/ thermionic valves. These computers used binary-coded language (also called machine language consisting of 0s and 1s) to perform operations. The notable examples include ENIAC, EDVAC and UNIVAC.

The second generation of computers (1959–1964) was the era of transistor-based computers. The *transistor was invented during 1947* which functions like a vacuum tube in that, it can be used to relay and switch electronic signals. There were obvious differences between the transistor and the vacuum tube. The transistor was faster, more reliable, smaller, and much cheaper to build unlike a vacuum tube. One transistor replaced the equivalent of 40 vacuum tubes. These transistors were made of solid material, some of which is *silicon*, an abundant element. Transistors were found to *conduct electricity faster* and *better* than vacuum tubes. They were also much smaller and gave off virtually *no heat* compared to vacuum tubes. Their use

marked a new beginning for the computer. Without this invention, the technological progress in the 1960's would not have been possible.

The third generation of computers (1965–1970) were made up of integrated circuits, which replaced transistors. The *integrated circuit*, or as it is sometimes referred to as *semiconductor chip*, packs a huge number of transistors onto a single *wafer of silicon*. Placing such large numbers of transistors on a single chip vastly increased the power of a single computer and lowered its size and cost considerably. Most electronic devices today use some form of integrated circuits placed on printed *circuit boards* (thin pieces of *Bakelite* or *fibre glass* that have electrical connections etched onto them) sometimes called a *motherboard*. These third-generation computers could carry out instructions in billionths of a second. The size of these machines dropped to the size of small file cabinets.

The fourth generation can be characterised by both the jump to monolithic integrated circuits and the invention of the microprocessor. The monolithic integrated circuits involved putting millions of transistors onto one single chip by which more calculation and faster speeds could be reached by computers. The microprocessor is a single chip that could do all the processing of a full-scale computer. As the size of components and the distances between them became smaller, the speed of computers improved greatly. Initially, the microprocessor was made to be used in calculators, not computers. Subsequently, it led to the invention of *personal computers* (PCs), or *microcomputers*. It wasn't until the 1970's that people began buying computers for personal use. One of the earliest personal computers was the *Altair 8800 computer kit*. In 1975, people could purchase this kit and put it together to make their own personal computer. In 1977, the Apple II was sold to the public and in 1981, IBM entered the PC market. Microsoft entered the PC revolution as the co-developer of desktop operating system along with IBM.

The fifth-generation computers are still in the development stage. The computers of the next generation will have millions upon millions of transistors on one chip and will perform over a billion calculations in a single second. The goal of fifth-generation computing is to develop devices that respond to natural language input, and will have the capabilities of learning and self-organising.

28.3 CLASSIFICATION OF COMPUTERS

Due to rapid technological developments and changing information needs, computers are now available in many sizes and types serving diverse purposes. As such, we can classify computers according to the purpose, nature of data handling and functionality (typically characterised by physical size, performance and application scenarios). This classification is summarised in Fig. 28.1.

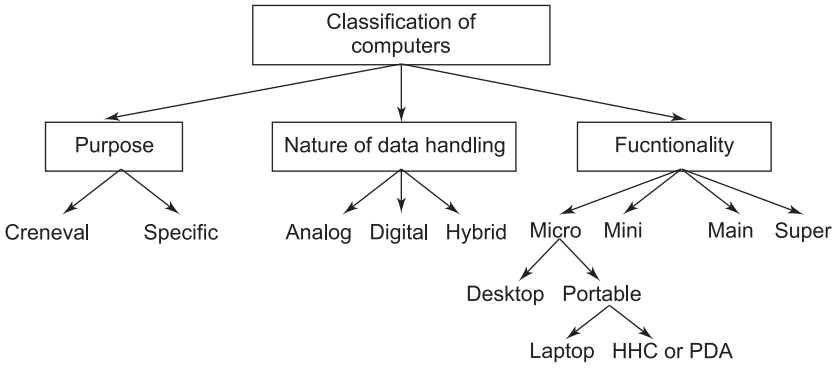


Fig. 28.1 *Computer classification*

28.4 THE COMPUTER SYSTEM

Typically, a computer (of any generation and/or classification) can be viewed as a system that comprises several units or parts such as computer hardware, peripherals, communication equipment and software. These interrelated units or parts work together for converting data into information. The simplified computer-system architecture is depicted in Fig. 28.2.

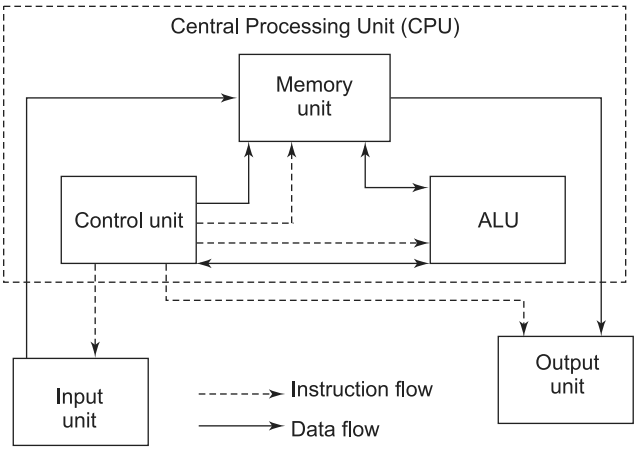


Fig. 28.2 *Computer architecture*

The CPU or the microprocessor or simply processors is referred as the brain of a computer system. The processors differ from one another by their instruction set (hard wired in the processors) or the instruction set determines the machine language for the process. In general, the CPU contains the ALU (Arithmetic and Logic Unit) that performs computations, the control unit that can issue control signals, and registers (words of memory inside the CPU).' The main job of the CPU is to execute (i.e. interpret) machine-language programs, one instruction at a time. A program is a sequence of machine-language instructions, stored in consecutive memory locations. To execute programs, the CPU uses two special registers: *PC (Program Counter)* containing the memory address of the current or next instruction to be executed and *IR (Instruction Register)* that contains the current instruction being executed. Instructions are executed in a sequence of operations called the *instruction cycle*. One instruction cycle may have multiple machine cycles. One machine cycle consisting of the following operations:

- **Fetch**—Feeding the instructions from memory to ALU
- **Decode**—Converting instruction to control signals that initiate the required operation
- **Execute**—completing the task and generating output

The instruction cycle is repeated indefinitely, as long as the machine is on. Figure 28.3 gives details of the *data path* within the CPU of a typical von Neumann machine.

In general, one machine cycle corresponds to one cycle of the data path. The control unit (not shown in the data-path diagram), generates signals to direct the operations of the data path such as choosing registers from the register file to be loaded into registers *A* and *B* (or generally working registers), choosing the ALU operation for this cycle (add, subtract, and, or, etc.), choosing the destination register for storing the result, and handling the instruction sequence.

Further, a specially designed buffer storage called *cache* is used to improve computer performance by reducing access time. It holds instructions and data that are likely to be needed for the next operation by the processor. The cache copies frequently accessed data and instructions from primary storage (main memory) or secondary storage (disks).

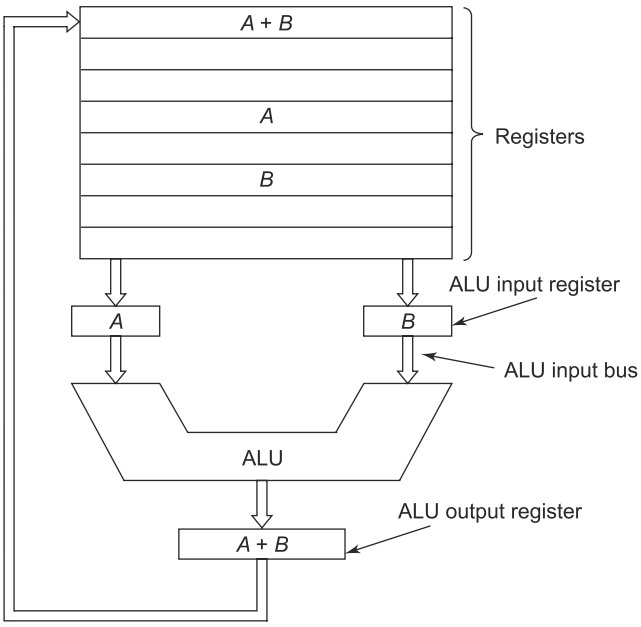


Fig. 28.3 *The data path of a typical von Neumann machine*

❑ **Disk Cache** A disk cache is in a reserved segment of primary memory or in an extra memory on the disk-controller card. It contains a large block of frequently accessed data copied from a disk. The data in a disk cache can be used to fulfill the data requests from a processor at high speed. The disk cache lets the processor avoid a slow disk access.

❑ **Memory Cache** A memory cache is a high-speed memory storage between the memory and the CPU. It is smaller and much faster than the main memory (primary storage). The memory cache copies blocks of instructions and data from the main memory so that execution and data updating are performed in the higher-speed memory bank.

28.5 COMPUTER HARDWARE

The major constituents of computer hardware are the processor, memory and input/output devices. As mentioned previously, the size and cost of hardware has been falling due to rapid technological advancements. Further, many hardware components may be integrated on a single board, known as the motherboard. Today's motherboards may have a built-in hard-disk controller, graphics, multi-media and network interface cards. The following sections provide brief descriptions of major hardware constituents.

28.5.1 Processors

A processor is a microprocessor whose elements are miniaturised into one or a few integrated circuits contained in a single silicon microchip, which can execute instructions. Intel and Motorola are the major companies that produce important microprocessors. In a microcomputer, the Central Processing Unit (CPU) is held on a single microprocessor and requires a system clock, primary storage, and power supply to perform its processing functions. The capacity of a microprocessor chip is represented in word sizes. A word size is

the number of bits (e.g. 8, 16 or 32 bits) that a computer (CPU) can process at a time. If a word has more bits, the processing is faster and more powerful. For example, a 16-bit-word CPU can access and manipulate 2 bytes (1 byte = 8 bits) at a time, while a 32-bit-word CPU can access and manipulate 4 bytes at a time. Therefore, the 32-bit CPU is faster than the 16-bit CPU. Based upon the instruction sets, there are two types of computing architectures, CISC and RISC.

❑ **CISC Chips** CISC stands for *Complex Instruction Set Computer*. It is pronounced as "sisk." CISC is a computer architecture that has large sets of instructions in the order of several hundred instructions. Intel's Pentium chip uses CISC design.

❑ **RISC Chip** RISC stands for *Reduced Instruction Set Computer*. In RISC, most programs generally use only a few instructions. This architecture has a small number of instructions built into the circuits and if those basic instructions are made to execute faster then RISC computers increase performance. Although RISC machines are only around 30% faster than CISC machines, RISC chips are less expensive to produce.

28.5.2 Primary Memory (Internal Storage)

Primary memory (*internal storage*, *main memory* or *memory*) is the computer's working storage space that holds data, instructions for processing, and processed data (information) waiting to be sent to secondary storage. Physically, primary storage is a collection of RAM chips. The contents are held in the primary storage only *temporarily*. Its *capacity* varies with different computers. Data or instructions are stored in primary-storage locations called *addresses*.

28.5.3 Secondary Storage (Hard Disk Drives—HDD)

As the primary memory is small and volatile in nature, there is need to use secondary storage. The secondary storage is typically of large and permanent capacity. The most commonly used and available secondary storage is the hard disk drive or HDD. A *hard disk* is a magnetic disk made of metal and covered with a magnetic recording surface. It is a nonvolatile storage device which stores digitally encoded data on rapidly rotating platters with magnetic surfaces. Hard disks come in removable and fixed varieties that hold from several hundreds of megabytes to several gigabytes. Older HDDs quoted their smaller capacities in megabytes, some of the first drives for PCs being just 5 or 10*MB, but recent HDDs are of few gigabytes to few hundred gigabytes. The capacity of an HDD can be calculated by multiplying the number of cylinders by the number of heads by the number of sectors by the number of bytes/sector (most commonly 512 bytes/sector).

28.5.4 Tertiary or Auxiliary Storage

Tertiary, or auxiliary storage, is typically an external storage meant for data transfer and back-up purposes. This storage includes floppy diskettes, magnetic tape, optical disk, CD ROMs and USB drives. Floppy diskettes are mostly used for boot-up programs and rarely as auxiliary storage. Currently, CD-ROMs and USB Drives are predominantly used as auxiliary storage.

CD-ROM (an abbreviation of "Compact Disc read-only memory") is a pre-pressed Compact Disc that contains data accessible but not writable by a computer. The Compact Disc format was originally designed for music storage and playback. CD-ROMs are popularly used to distribute computer software, including games and multimedia applications, though any data can be stored (up to the capacity limit of a disc). Some CDs hold both computer data and audio with the latter capable of being played on a CD player, whilst data (such as software or digital video) is only usable on a computer (such as PC CD-ROMs). Discs are made from a 1.2 mm thick disc of polycarbonate plastic, with a thin layer of aluminum to make a reflective surface. The most common size of a CD-ROM disc is 120 mm in diameter, though the smaller Mini CD standard with an 80 mm diameter, as well as numerous nonstandard sizes and shapes (e.g. business-card-sized media) are also available. Data are stored on the disc as a series of microscopic indentations. A laser is shown onto the

reflective surface of the disc to read the pattern of pits and lands ("pits", with the gaps between them referred to as "lands"). Because the depth of the pits is approximately one-quarter to one-sixth of the wavelength of the laser light used to read the disc, the reflected beam's phase is shifted in relation to the incoming beam, causing destructive interference and reducing the reflected beam's intensity. This pattern of changing intensity of the reflected beam is converted into binary data.

A **USB flash drive** is a NAND-type, flash memory, data-storage device integrated with a USB (Universal Serial Bus) interface. USB flash drives are typically removable and rewritable, much shorter than a floppy disk and lightweight. Storage capacities typically range from 64 MB to 64 GB with steady improvements in size and price per gigabyte. Some allow 1 million write or erase cycles and have 10-year data retention, connected by USB 1.1 or USB 2.0. USB Memory card readers are also available, whereby rather than being built-in, the memory is a removable flash memory card housed in what is otherwise a regular USB flash drive, as described below.

USB flash drives offer potential advantages over other portable storage devices, particularly the floppy disk. They are more compact, faster, hold much more data, have a more durable design, and are more reliable for lack of moving parts. Additionally, it has become increasingly common for computers to ship without floppy disk drives. USB ports, on the other hand, appear on almost every current mainstream PC and laptop. These types of drives use the USB mass storage standard, supported natively by modern operating systems such as Windows, Mac OS X, Linux, and other Unix-like systems. USB drives with USB 2.0 support can also be faster than an optical disc drive, while storing a larger amount of data in a much smaller space.

28.5.5 Input Devices

The keyboard is a main input device used to feed data and instructions to the processor. There are many specialised input devices, viz. mouse, touch screen, light pen, graphics tablet, scanner, bar-code readers and smart cards. Storage devices such as disk drives and even floppy diskettes can also serve as input devices. Voice-based input devices are the latest developments providing next-generation input technology for human-computer interaction. The human-computer interaction will become more sophisticated and complex in the era fast approaching disappearing computing scenarios or smart environments. Computer-to-computer interaction will also assume great importance in the networked world.

28.5.6 Output Devices

The Visual Display Unit (VDU), also commonly called monitor, is the mainly used output device. The other output devices include printers and plotters. Storage devices such as disk drives and even floppy diskettes can also serve as output devices.

A monitor or display, is a piece of electrical equipment, which displays images generated from the video output of devices, such as computers, without producing a permanent record. The monitor comprises the display device, simple circuitry to generate and format a picture from video, sent by the signals source, and usually an enclosure. Within the signal source, either as an integral section or a modular component, there is a display adapter to generate video in a format compatible with the monitor. There are two types of monitors: Cathode-Ray Tube (CRT) monitor and Liquid Crystal Display (LCD) monitor. The CRT monitors are big and heavy looking like a television, but have a better display resolution and often a higher frequency. The liquid crystal display (LCD) monitors, are thin, flat, and lightweight. It is a newer technology than CRTs. The quality can be the same or even better than a CRT, but these types of monitors usually cost more than CRT monitors. A newer LCD monitor typically consists of a Thin Film Transistor (TFT).

A printer is a peripheral device, which produces a hard copy (permanent human-readable text and/or graphics) of documents stored in electronic form, usually on physical print media such as paper or transparencies. Printers are mainly classified into line, daisy-wheel, dot matrix, laser and inkjet printers. The data received by a printer may be a string of characters, a bitmapped image, or a vector image. Some printers can process all three types of data, while some cannot. The speed of early printers was typically measured in units of characters per second. More modern printers are measured in pages per minute.

28.6 COMPUTER SOFTWARE

A computer system is a useless box unless otherwise it is provided with appropriate data and programming instructions. Programming has been a fascinating world since the advent of the computer. Sometimes, programming may be equated with computing itself. However, we need to take a holistic view as there have been several developments since 1948, the year the *Baby Computer* was introduced. Today, we have an independent software engineering discipline which deals with development and management of large and complex programmes working as a unified system. Similarly, we have to deal with the information beyond data, which dominated the early computing domain. Another branch of study, *informatics*, deals with the science of information, the practice of information processing and the engineering of information systems. India has been a pioneer in these fields since the last two decades. Due to dominance of software and services, IBM in association with academia and industry have proposed a new discipline—SSME. The Service Science, Management and Engineering (SSME) is a growing multi-disciplinary effort that integrates aspects of computing, operations research, engineering, management science, business strategy, social and cognitive science and legal science disciplines. However, we limit our discussion here in the following sections dealing with basic software and its applications.

28.6.1 System Software

System software is a program that manages computer resources and operations of a computer system while it executes various tasks such as processing data and information, controlling hardware components and allowing users to use application software. That is, systems software functions as a *bridge* between computer-system hardware and the application software. System software is made up of many language translators, control programs, including the operating system, communications software and database management system.

28.6.2 Operating Systems

An operating system is a collection of integrated computer programs that provide recurring services to other programs or to the user of a computer. These services consist of disk and file management, memory management and device management. In other words, it manages CPU operations, input/output activities, storage resources, diverse support services, and controls various devices. An operating system executes many functions to operate a computer system efficiently. Among them, four essential functions are the following.

❑ **Resource Management** An operating system manages a collection of computer hardware resources by using a variety of programs. It manages computer-system resources, including its CPU, primary memory, virtual memory, secondary storage devices, input/output peripherals, and other devices.

❑ **Task Management** The function of the operating system controls the running of many tasks. It manages one program or many programs within a computer system simultaneously. That is, this function of operating system manages the completion of users' tasks. A task-management program in an operating system provides each task and interrupts the CPU operations to manage tasks efficiently. Task management may involve a multitasking capability.

❑ **File Management** This is a function that manages data files. An operating system contains file management programs that provide the ability to create, delete, enter, change, ask and access files of data. They also produce reports on a file.

❑ **User Interface** It is a function of an operating system that allows users to interact with a computer. A user-interface program may include a combination of menus, screen design, keyboard commands, etc. A well-designed user interface is essential for an operating system to be popular. Because of the function, users can load programs, access files and accomplish other tasks.

❑ **Virtual Memory** This is a technique for an operating system to manage memory. An operating system simulates significantly larger memory capability than the real memory capacity of its actual primary storage unit. It allows computers to process larger programs than the physical memory circuit would allow.

❑ **Multitasking** This refers to the capability of operating systems that run several computing tasks in one computer at the same time. This is controlled by the task-management program in an operating system. It is also called *multiprogramming* and *multithreading*.

The operating system along with language translators typically constitutes a basic platform for computer programming and software development. The language translators can be categorised as assembler, compiler, and interpreter. An assembler translates the assembly-language programme into machine-level-language program. A compiler is used for translating an entire piece of source code written in a high-level language to machine-level language whereas an interpreter translates statement by statement. A modern assembler creates an object code by translating assembly instruction mnemonics into opcodes, and by resolving symbolic names for memory locations and other entities. A cross compiler is a compiler capable of creating executable code for a platform other than the one on which the compiler is run.

28.6.3 Programming Languages

A programming language is used to write programs involving a computer to perform computations. The complex computations typically involve algorithms. A computer program may possibly control external devices such as printers, robots, and so on. It may contain constructs for defining and manipulating data structures or controlling the flow of execution, typically following a prescribed syntax. Most programming languages are purely textual; they use sequences of text including words, numbers and punctuation, much like written natural languages. On the other hand, there are some programming languages, which are more graphical in nature, using spatial relationships between symbols to specify a program. The syntax of a language describes the possible combinations of symbols that form a syntactically correct program. Programming language syntax is usually defined using a combination of regular expressions. There are five generations (levels) of programming languages. The first three generations are procedural and the next two are nonprocedural languages. A *procedure* is effectively a list of computations to be carried out for completing the desired task. So the procedural languages are simply integration of procedures (also known as functions, subroutines, or methods), small sections of code that perform a particular function to be carried out to reach the final state. In nonprocedural languages (fourth-and fifth-generation languages), the user only has to tell what to do, the system will take care of steps to be followed and the logics.

The first-generation language is machine language (involves only 0's and 1's) which directly controls the hardware resources. The second-generation language is assembly programming language in the form of mnemonics, which is an advancement over the machine language. The third-generation languages include high-level languages like BASIC, COBOL, FORTRAN, Pascal and C. The example of fourth-generation language is Structured Query Languages (SQL), which has become a native language for database management systems. SQL is basically a command-based language without low-level interaction with computer hardware. Many computer scientists have advocated in favour of PROLOG (Programming in Logics) as the fifth-generation language though the fifth generation hardware is still being debated. The fifth-generation languages will enable development of intelligent systems capable of making decisions with or without users' involvement.

The other classification of programming languages is structural and object oriented, programming languages. *Structured programming* is a special type of procedural programming. It requires that programmers break the program structure into small pieces of code that are easily understood. It is often associated with a "top-down" approach to design. The most popular structured programming languages include C, Ada and Pascal. In Object-Oriented Programming (OOP), the designer specifies both the data structures and the types of operations that can be applied to those data structures. This pairing of a piece of data with the operations that can be performed on it is known as an *object*. A program thus becomes a collection of cooperating objects, rather than a list of instructions. Objects can store state information and interact with other objects,

but generally each object has a distinct, limited role. Some of the key characteristics of OOP are inheritance, encapsulation and polymorphism. The most popular object-oriented programming languages include C++, Java, C# and Python.

28.6.4 Application Software

Application software consists of programs that direct computers to perform specific information-processing activities for end users. These programs are called *application packages* because they direct the processing required for a particular use, or *application*, which users want to accomplish. Thousands of application packages are available because there are thousands of different jobs end users want computers to do. Application software includes a variety of programs that can be subdivided into general-purpose and application-specific categories.

General-Purpose Application Programs

General-purpose application packages are programs that perform common information processing jobs for end users. For example, word-processing programs, electronic spreadsheet programs, database management programs, graphics programs, communications programs and integrated packages are popular with microcomputer users for home, education, business, scientific and many other general purposes. They are also known as *productivity* packages, because they significantly increase the productivity of end users. This packaged software is also called *commercially-off-the-shelf software* (*COTS*) *package*, because these products are packaged and available for sale. Many features are common to most packaged programs. Some examples are word-processing packages, spreadsheets, etc. which are used to create, manipulate, print the documents and they can even use some formulas and calculate different outcomes. Microsoft office tools and Linux open sources are the most common application programs.

Application-Specific Software

Many application programs are available to support specific applications of end users. These can be classified as *Scientific and Business Application Programs*.

❑ **Scientific Application Programs** Programs that perform information processing tasks for the natural, physical, social and behavioral sciences, engineering and all other areas involved in scientific research, experimentation and development. There are so many other application areas such as education, music, art, medicine, etc. The trend in computer application software is towards multipurpose, expert-assisted packages with natural language and graphical user interfaces.

❑ **Business Application Programs** These are programs that accomplish the information processing tasks of important business functions or industry requirements.

Graphics Packages

A graphics program can typically display numeric data in a visual format for analytical or presentation purposes. Any other types of presentation graphics displays are also possible. Most of the graphics packages support freehand drawing, while desktop publishing programs provide predrawn clip art graphics for insertion into documents. Popular business graphics packages are Harvard Graphics, Freelance, Corel Draw, etc. There are two types of graphics programs. *Analytical graphics programs*, which are used to analyse data and *presentation graphics programs*, which are used to create attractive finished graphs for presentations or reports.

Database Management Packages

A *database* is a large collection of data entered into a computer system and stored for future use. The computerised information in the database is organised so that the parts that have something in common

can be retrieved easily. A database management package or *Database Management System* (*DBMS*) is a software package used to set up, or structure, a database. The four types of DBMS are hierarchical, network, relational DBMS, and object-oriented DBMS. The most popular one is Relational DBMS. The structured query language (SQL) serves as a native language for most DBMS. It is also used to retrieve and manage information from a database. Most DBMS packages can perform four primary tasks:

❑ **Database Development** Define and organise the content, relationships, and structure of the data needed to build a database

❑ **Database Interrogation** Access the data in a database for information retrieval and report generation. A user can selectively retrieve and display information and produce printed reports and documents

❑ **Database Maintenance** Add, delete, update, correct, and protect the data in a database

❑ **Application Development** Develop prototypes of data entry screens, queries, forms, reports, and labels for a proposed application

Communications Packages

Communications software packages for microcomputers are also viewed as general-purpose application packages. These packages can connect a microcomputer equipped with a modem to a public and private network. Communications software enables a microcomputer to send and receive data over a telephone or other communications line. Communications programs are used by all kinds of people inside and outside business. Examples are students doing research papers, travellers making plane reservations, consumers buying products, investors getting stock quotations and economists getting government statistical data. Communications programs give microcomputers a powerful feature, which is connectivity. Connections with microcomputers open a world of services. Before the advent of the Internet, the popular communications software used were ProComm, SmartCom and Crosstalk. Some common usage of computer communications programs are as follows:

❑ **Data Banks** With this communications program, users can access enormous computerised databases—data banks of information. Some of these, such as Dialog, resemble huge electronic encyclopedias.

❑ **Message Exchanges** Communications programs enable users to leave and receive messages on electronic bulletin boards or to use electronic-mail services. Electronic bulletin boards exist for people interested in swapping all kinds of software or information. Many organisations now have electronic mailboxes.

❑ **Financial Services** With communications programs, users can look up airline reservations and stock quotations. Users can order discount merchandise and even do home banking and bill paying.

Development Tools and Special Purpose Software

Software is omnipresent in most of the scientific, engineering, industry and other fields. As such, several domain-specific or special-purpose software tools have been developed to increase productivity, quality and functionality. Further, we have the Computer-Aided Software Engineering (CASE) Tool—an interesting set of tools, which even automates the development of software itself. A typical CASE tool helps in requirements engineering, modelling, architecture, design, verification and validation of software systems. The following sections discuss tools used in other branches of science and engineering.

❑ **MATLAB** is a high-performance language for technical computing. It integrates computation, visualisation, and programming in an easy-to-use environment, where problems and solutions are expressed in familiar mathematical notation. Typical uses are computation, algorithm development, modelling,

simulation, prototyping, data analysis, exploration, visualisation, scientific and engineering graphics, application development, including Graphical User Interface building, etc.

❑ **Mathematica** is a versatile, powerful application package for doing mathematics and publishing mathematical results. It runs on most popular workstation operating systems, including Microsoft Windows, Apple Macintosh OS, Linux and other Unix-based systems. Mathematica is used by scientists and engineers in disciplines ranging from astronomy to zoology; typical applications include computational number theory, ecosystem modelling, financial derivatives pricing, quantum computation, statistical analysis and hundreds more.

❑ **Electronic Design Automation (EDA)** is the category of tools for designing and producing electronic systems ranging from Printed Circuit Boards (PCBs) to integrated circuits. EDA for electronics has rapidly increased in importance with the continuous scaling of semiconductor technology. Some users are foundry operators, who operate the semiconductor fabrication facilities, or "fabs", and design-service companies who use EDA software to evaluate an incoming design for manufacturing readiness. EDA tools are also used for programming design functionality into FPGAs. Cadence provides a wide range of EDA tools.

❑ **AutoCAD** is a Computer Aided Design (CAD) program used by just about every engineering and design office in the world. Although there are alternative CAD packages, AutoCAD is by far the most widely used system. Autodesk's AutoCAD is the industry leader in CAD packages used by civil engineers, architects, mechanical and electrical engineers, aeronautical engineers plus many other disciplines. The drawings with accurate scale can be created and published using AutoCAD's powerful features. 3D models can also be created giving the designer absolute control over the design from start to finish. The computerised model can be viewed through a 360° angle, and even 'rendered' with a texture on screen to give an idea of the finished product.

28.7 DATA COMMUNICATION AND COMPUTER NETWORK

The term *communication* in simple words means exchanging (i.e. receiving or sending) information. In ancient times, the usage of beating drums, smoke signals, mirrors reflecting sunlight, and so on were the common means of communication. With the advancement in science and technology, various communication devices were developed. Voice communication became common after the invention of the telephone by Alexander Graham Bell in 1870. The major breakthroughs in 1980 led to setting up of data communication and networked computers, which revolutionised the field of information and communication technology. The advent of the Internet in 1960s and subsequent technological developments have transformed the world into a global village. The following discussion summarises some of the basic concepts of data communication.

A data-communication system consists of different components that are used to work together to transfer data from one place to another. These are central computer, control programs, terminals, modem, data-communication media, data transmission modes and networking. The computers that manage transmission of data between different computers is called a *central computer*. Control programs control the flow of data from one computer to the other. These are operating systems that control the working of the computers. A terminal is the basic communication unit. Many persons can work on a single computer by connecting many terminals to the large computer. Through telephone-line data transfer from one place to other in the form of analog signals. Thus, for transferring data from one computer to another computer through telephone line, digital signals must be converted to analog signals. For receiving digital signals by another computer, these analog signal must be converted into digital signals. Different data-transmission modes are used such as twisted cable, fibre optical cable, microwave, etc.

There are two basic categories of transmission media: guided and unguided. *Guided transmission media* uses a "cabling" system that guides the data signals along a specific path. The data signals are bound by the "cabling" system. Guided media is also known as *bound media*. Cabling is meant in a generic sense in the previous sentences and is not meant to be interpreted as copper wire cabling only. *Unguided transmission media* consists of a means for the data signals to travel but nothing to guide them along a specific path. The data signals are not bound to a cabling media and as such are often called *unbound media*. There are 4 basic types of guided media: open wire, twisted pair, coaxial cable, and optical fibre. Unguided Transmission Media is data signals in the form of Radio Frequencies (RF) that flow through the air. They are not guided or bound to a channel to follow. The RF wave propagations are classified by ground wave, ionospheric, and Line of Sight (LOS) Propagation.

Based on the permissible direction of the data flow, the communications systems can be categorised as simplex, half-duplex and full-duplex. In *simplex* systems, the data flows in only one direction on the data communication line (medium). Examples are radio and television broadcasts. In *half-duplex* systems, the data flows in both directions but only one direction at a time on the data communication line, for example, conversation* on walkie-talkies. In *full-duplex* systems, the data flows in both directions simultaneously. A common example is Modulator/Demodulator (Modem) based communication, which can be configured for data flow in both directions.

Further, the data transmission may be synchronous or asynchronous. *Asynchronous transmission* sends only 1 character at a time; a character being a letter of the alphabet or number or control character. Preceding each character is a start bit and ending each character is 1 or more stop bits. *Synchronous transmission* sends packets of characters at a time. Each packet is preceded by a *start frame*, which is used to tell the receiving station that a new packet of characters is arriving and to synchronise the receiving station's internal clock. The packets also have end frames to indicate the end of the packet.

28.7.1 Computer Communication Protocols

The International Standards Organization (ISO) developed a set of standard protocols called the Open Systems Interconnection (OSI). The OSI model separates each network's functions into seven layers of protocols or communication rules. This model identifies functions that should be offered by any network system. The OSI Model clearly defines the interfaces between each layer. This allows different network operating systems and protocols to work together by having each manufacturer adhere to the standard interfaces.

❑ **Physical Layer** The physical layer sends data from the user computer to a host computer (and vice versa). This layer is concerned essentially with computer hardware, whereas the upper layers are interested in communications software. This layer, for example, manages voltage of electricity, timing factors or connector standards.

❑ **Data-Link Layer** The data-link layer formats the received data into a record called a frame. This layer also is in charge of error detection.

❑ **Network Layer** The network layer provides the physical layer with the ability to transfer records from one computer to another. This layer provides for the functions of internal network operations such as addressing and routing.

❑ **Transport Layer** The transport layer allows communication to take place between the user and host computers. That is, this layer takes care of end to end validity and integrity of the transmission. OSI transport services takes place through layer 1 to layer 4, which are collectively responsible for acquiring data and information from the sender to the receiver.

❑ **Session Layer** The session layer is in charge of starting, maintaining, and ending each logical session between the interacting end-user computers.

❑ **Presentation Layer** The presentation layer formats incoming data so that it can be presented on the receiving terminal for end users. In other words, it is in charge of displaying, formatting and editing user inputs and outputs.

❑ **Application Layer** The application layer controls the input from the user computer and allows the application program to be run on the host computer. This layer is the end user's access to the network.

US Department of Defence project ARPAnet officially adopted the Transmission Control Protocol/ Internet Protocol (*TCP/IP*) *developed in the 1970s by pioneering network engineers Vinton Cerfand Bob Kahn*. TCP/IP has two parts. TCP protocol controls data transfer that is the function of the transport layer in the OSI model. IP protocol provides the routing and addressing mechanism that are the roles of the network layer in the OSI model. This protocol is supported by many hardware vendors from microcomputers to mainframes. It is used by most universities, federal governments, and many corporations. TCP/IP is also the network protocol used on the Internet thus making it the *de facto* standard while the OSI remained as the reference model.

28.7.2 Types of Networks

Communications networks vary in geographical size. Networks may be constructed within a building or across several buildings. Networks may also be citywide and even international, using both cable and air connections. There are three major network types: Local Area Network (LAN), Metropolitan Area Networks (MAN) and Wide Area Network (WAN).

A computer communications network contained in a small area such as a commercial building is known as a local area network (LAN). A LAN usually is accomplished with either telephone, coaxial, or fibre optic cables. The major benefit of a LAN is that it can help reduce costs by allowing people and microcomputers to share expensive resources. Also, a LAN enables users to participate in office automation systems. Network designers can choose the method in which messages are controlled in a LAN. Two basic methodologies are the token-passing approach and the contention-based approach. The *token-passing approach* allows the designers of a network to achieve a degree of centralised control. A group of data bits, or "token", is passed from one network node to another. A node can only send a message when it is in possession of the token. In the *contention-based approach*, a node that wishes to send a message first listens to determine if another node is currently sending a message. If not, the node attempts to send its message. However, the lack of centralised control can result in a collision—two nodes attempting to send messages simultaneously. Consequently, contention-based approach is usually not suitable for networks with a large amount of communications activity. The Ethernet is the most popular example using the contention-based approach.

The next larger network than LAN may be a Metropolitan Area Network (MAN) usually spanning a city or county area. It interconnects various buildings or other facilities within this citywide area. For example, linkages can be established between two commercial buildings. A more recent use of MAN technology has been the rapid development of cellular phone systems.

A wide area network (WAN) is one that operates over vast distances spanning cities, states or national boundaries. This network interconnects computers, LANs, MANs and other data-transmission facilities. Typically, WAN will employ communications circuits such as long-distance telephone wires, microwaves and satellites.

28.7.3 Network Topology

Networks can be classified by their topology. The topology is the basic geometric arrangement of the network. Communications channels can be connected in different arrangements using several different topologies.

Four basic types of network configurations are star, bus, ring and mesh. The LANs typically use bus or star and sometime ring topologies. Star and mesh topologies are commonly used in MANs and WANs. The networks are usually built using a combination of several different topologies.

A *star topology* is one in which a central unit provides a link through which a group of smaller computers and devices are connected. The central computer is commonly called a *host computer*. In the star network,

all interactions between different computers in the network travel through the host computer. The central unit will poll each to decide whether a unit has a message to send. If so, the central computer will carry the message to the receiving computer.

In a *bus configuration*, each computer in the network is responsible for carrying out its own communications without the aid of a central unit. A common communications cable (the bus) connects all of the computers in the network. As data travels along the path of the cable, each unit performs a query to determine if it is the intended recipient of the message. As the information passes along the bus, it is examined by each terminal to see if the data is for it.

A *ring configuration* features a network in which each computer is connected to the next two other computers in a closed loop. Like the bus network, no single central computer exists in the ring configuration. Messages are simply transferred from one computer to the next until they arrive at their intended destinations. Each computer on the ring topology has a particular address. As the messages pass around the ring, the computers validate the address. If the message is not addressed to it, the node transmits the message to the next computer on the ring.

The *mesh* is a netlike configuration in which there are at least two pathways to each node. In a *mesh topology*, computers are connected to each other by point-to-point circuits. In the topology, one or more computers usually become switching centres, interlinking computers with others. Although a computer or cable is lost, if there are other possible routes through the network, the damage of one or several cables or computers may not have vital impact except the involved computers. However, if there are only few cables in the network, the loss of even one cable or device may damage the network seriously.

28.7.4 Types of Internetworks

An internetwork is composed of two or more networks or network segments connected. Any interconnection among or between public, private, commercial, industrial or governmental networks may also be defined as an internetwork or simply an internet. In modern practice, the interconnected networks use the Internet Protocol (IP). There are at least three variants of internetwork, depending on who administers and who participates in them: Intranet, Extranet and the Internet. An *intranet* is an IP network within an organisation or a corporate. An intranet may or may not have connections to the Internet. An intranet provides IP-based tools such as Web browsers and file-transfer applications that are under the control of a single administrative entity. That administrative entity closes the intranet to all but specific, authorised users. A large intranet will typically have at least one Web server to provide users with organisational information. An intranet is called an extranet when it provides access to itself from an authorised external organisation or an employee on the move (e.g. marketing or field engineer).

An *extranet* is a network or internetwork that is limited in scope to a single organisation or entity. It may also have limited connections to the networks of one or more usually, but not necessarily, other trusted organisations or entities (e.g. a company's customers may be given access to some part of its intranet creating in this way an extranet, while at the same time the customers may not be considered 'trusted' from a security standpoint). Technically, an "extranet may also be categorised as a CAN, MAN, WAN, or other type of network, although, by definition, an extranet cannot consist of a single LAN; it must have at least one connection with an external network.

The *Internet* is a specific internetwork. It consists of a worldwide interconnection of governmental, academic, public, and private networks using the Internet Protocol Suite. The Internet has become a backbone underlying the World Wide Web (WWW). Participants in the Internet use an addressing system (IP Addresses) administered by the Internet Assigned Numbers Authority (IANA). The Internet Engineering Task Force (IETF) coordinates protocols development. Service providers and large enterprise exchange information about the reachability of their address spaces through the Border Gateway Protocol (BGP), forming a redundant worldwide mesh of transmission paths.

28.7.5 Application of the Internet

The major applications of the internet are e-mail, remote login, discussion groups and information resources.

E-mail on the Internet

Electronic mail (e-mail) is one of the most rapidly growing developments in networked communications. Users of e-mail have their own file stored on a computer system. This file can be called a "mailbox." Access to a person's mailbox is protected by means of a password. Once logged on to an e-mail account, an end user may send messages and files to other mailboxes. An individual electronic mail transmission may be sent to one or many recipient accounts. This person may also read messages that have "arrived" in her or his mailbox from other e-mail accounts. Popular uses of e-mail have been to set up meetings within business organisations and to distribute memoranda throughout an organisation. Anyone with access to the Internet can send e-mail to anyone else on the Internet. An Internet e-mail address has two parts, the individual user's account address and the address of the computer. The computer's address in turn has two parts, the computer name and its domain. The general format is therefore, user@computer.domain. Note that the "at" symbol (@) separates the user's account from the computer address, and a period (.) separates the name of the computer from its domain.

Telnet (Remote Login)

The service that allows users to connect to a remote Internet host is called *Telnet*. Users on one computer in the Internet can login into other computers on the Internet by a special program, called Telnet, on your computer. This program uses the Internet to connect to the computer users specify. The users should know the account name and password of the remote computer. In Telnet, a user's computer is called the *local computer*. The other computer that the Telnet program connects is called the *remote computer*. An example of using Telnet is that users can read and send e-mail while travelling.

Discussion Groups

Discussion groups are the Internet users who have joined together to discuss some topic. Two groups are commonly used for business include Usenet and Listserv. *Usenet* is a large collection of discussion groups involving millions of people from all over the world. This is the most formally organised among the discussion groups. To read Usenet articles, users use a program called a newsreader. A *Listserv* is simply a mailing list developed on the large Bitnet network (not on the Internet). The listserv processor processes listserv commands such as requests to subscribe and unsubscribe, while the listserv mailer mails any message it receives to everyone on the mailing list.

Information Resources

The major use of the Internet is to find information. There are six major ways to find and achieve information:

❑ **FTP** File Transfer Protocol (FTP) is the underlying set of specifications that support Internet file transfer. In other words, FTP is a service that allows us to copy a file from any Internet host to any other Internet host.

❑ **Archie** Throughout the Internet, there are a number of computers, called *Archie servers*, which provide a service to help users find the name of anonymous FTP hosts that carry a particular file. Archie is a tool that allows users to search most of the publicly available anonymous FTP sites worldwide for specific files of interest.

❑ **Gopher** The Gopher is a powerful system that allows users to access many resources of the Internet in a simple, consistent manner. To use the Gopher, all users need to do are making selections from a menu.

❑ **Veronica** Veronica is a Gopher-based resource that users can use to search gopher space for all the menu items that contain specified words. Veronica is to Gopher what Archie is to FTP. It enables users to search all publicly available Gopher sites by specifying key words.

❑ **World Wide Web (WWW)** WWW or simply Web is one type of information resource that is growing even faster than Internet itself. It is an attempt to organise all the content on the Internet as a set of hypermedia documents. Besides that, it allows users to access all kinds of online resources using a Web browser and a Web server. A browser is a software package for accessing a Web server that stores files using HTML. There are many Web browsers available, for example, Microsoft Internet Explorer (IE), Mozilla FireFox, etc. A Web server stores information in a series of text files called *pages*. These text files or pages use a structured language called HTML (Hypertext Markup Language) to store their information.

❑ **WAIS** The WAIS stands for Wide Area Information Service. The original idea behind WAIS was to develop a generalised system of information retrieval that could access collections of data all around the world.

28.7.6 Basic Network Components

All networks are made up of basic hardware building blocks to interconnect network nodes, such as Network Interface Cards (NICs), repeaters, bridges, hubs, switches, routers and gateways. The repeaters and bridges are now not in use. A NIC is a piece of computer hardware designed to allow computers to communicate over a computer network. It provides physical access to a networking medium and often provides a low-level addressing system through the use of Media Access Control (MAC) addresses.

A *hub* is a multiple-port device. When a packet arrives at one port, it is copied to all the ports of the hub for transmission. When the packets are copied, the destination address in the frame does not change to a broadcast address. It does this in a rudimentary way, it simply copies the data to all of the nodes connected to the hub. This may lead to collision on the network. A *switch* is a device that performs switching which reduces broadcast domain. Specifically, it forwards and filters chunk of data communication between ports (connected cables) based on the MAC addresses in the packets. This is distinct from a hub in that it only forwards the datagram to the ports involved in the communications rather than all ports connected. Strictly speaking, a switch is not capable of routing traffic based on IP address, which is necessary for communicating between network segments or within a large or complex LAN. Some switches are capable of routing based on IP addresses but are still called switches as a marketing term. A switch normally has numerous ports with the intention that most or all of the network be connected directly to a switch, or another switch that is in turn connected to a switch.

A *router* is a networking device that forwards data packets between networks using headers and forwarding tables to determine the best path to forward the packets. Routers also provide interconnectivity between like and unlike media. This is accomplished by examining the *header* of a data packet, and making a decision on the next hop to which it should be sent. They use preconfigured static routes, status of their hardware interfaces, and routing protocols to select the best route between any two subnets. A router is connected to at least two networks, commonly two LANs or WANs or a LAN and its ISP's network.

A *gateway* is a combination of hardware and software that translates between two different protocols and acts as the connection point to the Internet. Gateways are the indispensable components in order to achieve multimedia communications between terminals connected to heterogeneous networks that use different protocols and have different network characteristics.

As the Internet is also used for commercial and business transactions, the issue of information security is very important. Typically, the network firewalls are used to safeguard any network connected to the Internet. Firewalls are configured and managed to realise an important security policy for the particular needs of a

given company or entity. A network gateway typically act as a firewall in that it filters packets and separates a proprietary corporate network, such as an Intranet, from a public network, such as the Internet.

28.8 CONVERGENCE OF COMPUTING AND COMMUNICATION

28.8.1 Computer Telephony Integration

Computer Telephony Integration (CTI) is a set of technologies for integrating computers and telephone systems. CTI functionality falls into two general categories: enabling computers to control the telephone system and enabling the telephone system to display information on computers. A user with a CTI-enabled computer will be able to dial the telephone, answer the telephone, and hang up the telephone, all from a computer. CTI enables users to dial the phone from address books stored on their computer. Most CTI systems facilitate users to interact with teleconferencing systems. A CTI-enabled computer will also display information from the telephone system, such as Caller-ID. Sophisticated CTI systems also display information from touch-tone and Interactive Voice Response (IVR) systems.

28.8.2 Network Convergence

Network convergence is an efficient coexistence of telephone, video and data communication within a single network. The use of multiple communication modes in a single network offers convenience and flexibility not possible with separate infrastructures. Network convergence is also called *media convergence*. Nowadays, a plethora of innovative applications are available, for example, Web surfing, VoIP (Voice over IP), FoIP (Fax over IP), streaming media, videoconferencing, e-business and e-learning.

28.8.3 Device Convergence

The device convergence means bringing the three worlds of communications, computing and consumer electronics in a single device. This convergence is ushering in a new epoch of multimedia, in which voice, data and images are combined to render services to the users. Typical examples include Web TV, e-mail and World Wide Web access via digital TV decoders and mobile phones, web casting of radio and TV programming on the Internet.

28.8.4 Voice-over-Internet Protocol (VoIP)

VoIP is a protocol optimised for the transmission of voice through the Internet or other packet-switched networks. VoIP is often used abstractly to refer to the actual transmission of voice (rather than the protocol implementing it). This latter concept is also referred to as IP telephony, Internet telephony, voice-over broadband, broadband telephony and broadband phone. VoIP-to-VoIP phone calls are sometimes free, while VoIP calls connecting to public switched telephone networks (VoIP-to-PSTN) may have a cost that is borne by the VoIP user. Voice-over-IP systems carry telephony signals as digital audio, typically reduced in data rate using speech data compression techniques, encapsulated in a data-packet stream over IP.

28.8.5 Videoconferencing

A videoconferencing (or *videoteleconferencing*) is a set of interactive telecommunication technologies, which allow two or more locations to interact via two-way video and audio transmissions simultaneously. The core technology used is digital compression of audio and video streams in real time. The hardware or software that performs compression is called a codec (coder/decoder). The compressed digital stream is transmitted through a digital network of some kind (usually ISDN or IP network).

28.9 EMERGING TECHNOLOGIES IN COMPUTING

28.9.1 Mobile Computing

Mobile computing enables users to work from a nonfixed location using portable computing and communications devices such as laptops, notebooks, palmtops, smart cell phones and Personal Digital Assistants (PDAs). Mobile voice communication has been widely established throughout the world impacting our life at work and home. An extension of the above development forms the basis of mobile computing. A PDA is such a device, which have both color screens and audio capabilities, enabling them to be used as mobile phones, smartphones, Web browsers, or portable media players. Many PDAs can access the Internet, intranets or extranets via Wi-Fi. The wireless-fidelity (Wi-Fi) is used to connect to the Internet when within range of a wireless network. The main aims of Wi-Fi are the following: make access to information easier, ensure compatibility and co-existence of devices, eliminate cabling and wiring, and eliminate switches, adapters, plugs, pins and connectors. The Bluetooth is a wireless protocol utilising short-range communications technology facilitating data transmission over short distances from fixed and/or mobile devices, creating wireless Personal Area Networks (PANs). Bluetooth provides a way to connect and exchange information between devices such as mobile phones, telephones, laptops, personal computers, printers, GPS receivers, digital cameras and video game consoles.

28.9.2 Grid Computing

Grid computing is a form of distributed computing whereby a "super and virtual computer" is composed of a cluster of networked, loosely coupled computers, acting in concert to perform very large tasks. This technology has been applied to computationally intensive scientific, mathematical and academic problems through volunteer computing. It is also used in commercial enterprises for diverse applications such as drug discovery, economic forecasting, seismic analysis, and back-office data processing in support of e-commerce and Web services. Grid computing facilitates more cost-effective use of a given amount of computer resources as well as provides as a way to solve problems that can't be approached without an enormous amount of computing power. In some grid computing systems, the computers may collaborate rather than being directed by one managing computer. One likely area for the use of grid computing will be pervasive computing applications—those in which computers pervade our environment without our necessary awareness.

28.9.3 Cloud Computing

Cloud computing means Internet ('Cloud') based development and use of computing. It is a paradigm in which information is permanently stored in servers on the Internet and cached temporarily on clients that include desktops, entertainment centres, table computers, notebooks, wall computers, handhelds, etc. The majority of cloud-computing infrastructure currently consists of reliable services delivered through next-generation data centres that are built on compute and storage virtualisation technologies. The services are accessible anywhere in the world, with the cloud appearing as a single point of access for all the computing needs of consumers.

28.9.4 Green Computing

Green computing is the study and practice of using computing resources efficiently. The goals are similar to green chemistry, i.e. reduce the use of hazardous materials, maximise energy efficiency during the product's lifetime, and promote recyclability or biodegradability of defunct products and factory waste, etc. Modern IT systems rely upon a complicated mix of people, networks and hardware. Green computing is the environmentally responsible use of computers and related resources. Such practices include the implementation of energy-efficient central processing units (CPUs), servers and peripherals as well as reduced resource consumption and proper disposal of electronic waste (e-waste). The work habits of computer users and businesses can be modified to minimise adverse impact on the global environment.

28.10 NEXT-GENERATION COMPUTING PARADIGMS

Silicon-based technologies have dominated the computing domain since its inception more than six decades ago. Researchers have been pursuing a number of alternatives to silicon-based computing. Now, the technology pundits say that silicon-based technologies are fast reaching towards the saturation point and would have to accommodate a swell of new computing paradigms, which are decidedly silicon-free. These nontraditional computing paradigms include DNA, quantum, molecular, biological, optical and nano-fluidic computing. All these are in their infancy but have the potential to complement the current silicon-based technologies if not to replace them. Most probably, these new paradigms would be applied to special-purpose computing. The following paragraphs provide a few examples of new computing paradigms.

DNA computing is a form of computing which uses DNA, biochemistry and molecular biology, instead of the traditional silicon-based computer technologies. It is fundamentally similar to parallel computing in that it takes advantage of the many different molecules of DNA to try many different possibilities at once. For certain specialised problems, DNA computers are faster and smaller than any other computer built so far. However, DNA computing does not provide any new capabilities from the standpoint of computability theory, the study of which problems are computationally solvable using different models of computation.

Quantum computing is direct use of distinctively quantum mechanical phenomena, such as superposition and entanglement, to perform operations on data. In a classical (or conventional) computer, information is stored as bits; in a quantum computer, it is stored as qubits (quantum binary digits). The basic principle of quantum computation is that the quantum properties can be used to represent and structure data, and that quantum mechanisms can be devised and built to perform operations with these data. If large-scale quantum computers can be built, they will be able to solve certain problems much faster than any of current computers.

Molecular computing are massively parallel computers taking advantage of the computational power of molecules (specifically biological). Molectronics specifically refers to the sub-field of physics, which addresses the computational potential of atomic arrangements. *Molecule cascade computing* is the newest area in the development of alternatives to traditional computing. This technique is based on forming circuits by creating a precise pattern of carbon monoxide molecules on a copper surface. By nudging a single molecule, it has been possible to cause a cascade of molecules, much like toppling dominoes. Different molecules can represent the 1's and 0's of binary information, making possible calculations. While this technique may make possible circuits hundreds of thousands of times smaller than those used today, it shares with the other alternatives the fact that a number of problems must be solved for it to be ever suitable for practical applications.

Biological computing is the use of living organisms or their component parts to perform computing operations or operations associated with computing, e.g. storage. The various forms of biological computing take a different route than those used by quantum or optical computing to overcome the limitations to performance that silicon-based computers face. Rather than focusing on increasing the speed of individual computing operations, biological computing focuses on the use of massive parallelism, or the allocation of tiny portions of a computing task to many different processing elements. Each element in and of itself cannot perform its task quickly, but the fact that there is an incredibly huge number of such elements, each performing a small task, means that the processing operation can be performed far more quickly.

Optical computing uses light instead of electricity (i.e. photons rather than electrons) to manipulate, store and transmit data. Photons have fundamentally different physical properties than electrons, and researchers have attempted to make use of these properties, mostly using the basic principles of optics, to produce computers with performance and/or capabilities greater than those of electronic computers. Most research projects focus on replacing current computer components with optical equivalents, resulting in an optical digital computer system processing binary data. This approach appears to offer the best short-term prospects for commercial optical computing, since optical components could be integrated into traditional computers to produce an optical/electronic hybrid.

Summary

- ➢ Basic computers, classification and different types of computers are introduced with their hardware and software specifications.
- ➢ Future computers and next generation computing paradigm are also discussed.

Exercises

Review Questions

1. What are the main objectives of fifth-generation computers?
2. What are the main functions of the control unit in microprocessors?
3. What are provided for the computers with on chip memory (storage)?
4. Compare the features of CISC and RISC.
5. What are the main functions of an operating system?
6. What are the main functions of gateway in the network components?
7. Discuss the merits of convergence in computing.
8. What is green computing? Also discuss the its importance,
9. In what way is the nontraditional computing is superior to silicon-based computing? What are the main properties of nontraditional computing?

Multiple-Choice Questions

1. How many generation of computers are there?
   (a) Four (b) Five (c) Six (d) Two
2. The computer system is used to
   (a) store data (b) process data (c) retrieve data (d) all of these
3. Cache memory is used
   (a) to speed up data processing (b) to slow down data processing
   (c) to start processing (d) none of these
4. Which one is not an input device?
   (a) Light Pen (b) Graphics Tablet
   (c) Storage devices (d) Printers
5. Virtual memory helps process
   (a) small programs (b) larger programs
   (c) the programs requiring more memory after RAM (d) none of these
6. Multitasking means
   (a) to run the same program on different machines
   (b) to run more than one program on a single machine
   (c) to run a single program on the single machine
   (d) all of the above
7. Which one is not a network component?
   (a) Huts (b) Switch (c) Router (d) Hard disk
8. Which one helps route packets in the network?
   (a) Hub (b) Switch (c) Router (d) Bridges
9. Which is not an operating system?
   (a) Win XP (b) Ms Word (c) Unix (d) Linux

10. Which network topology is the best?
    (a) Bus
    (b) Star
    (c) Ring
    (d) It depends on the geographic conditions

Answers

Multiple-Choice Questions

1. (b) 2. (d) 3. (a) 4. (d) 5. (c)
6. (b) 7. (d) 8. (c) 9. (b) 10. (d)

Clock and Timing Circuits

chapter 29

Goals & Objectives

- Introduction of clock and timing circuits
- Analysis and functional operation of IC 555 timer—astable and monostable operation with block diagrams
- Time constant changes in different operations

29.1 INTRODUCTION

The heart of a computer is the clock which produces clock pulses with the *precise cycle time*. The clock pulses advance the various circuits of the computer one step at a time. The clock pulses are normally rectangular; positive pulses followed by negative pulses as shown in Fig. 29.1. The duty cycle could be other than 50% but the cycle time must be precise. All logic elements must complete their transition in one cycle.

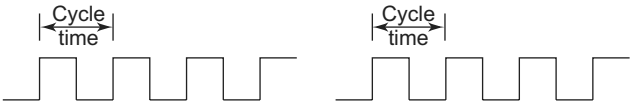


Fig. 29.1 *Ideal clock waveform*

The clock pulses can be generated by an IC-555 timer or by a crystal oscillator. We will study the IC-555 timer.

29.2 THE IC-555 TIMER

A popular and versatile analog-digital integrated circuit is the 555 timer. The entire circuit is housed in an 8-pin package as shown in Fig. 29.2, whose detailed circuitry is drawn in Fig. 29.3. It comprises

- Two op-amp comparators set at (2/3 V_{CC}) and (1/3 V_{CC}) respectively
- A three-resistor circuit, to obtain voltage 2/3 V_{CC} and 1/3 V_{CC}, to set the comparator

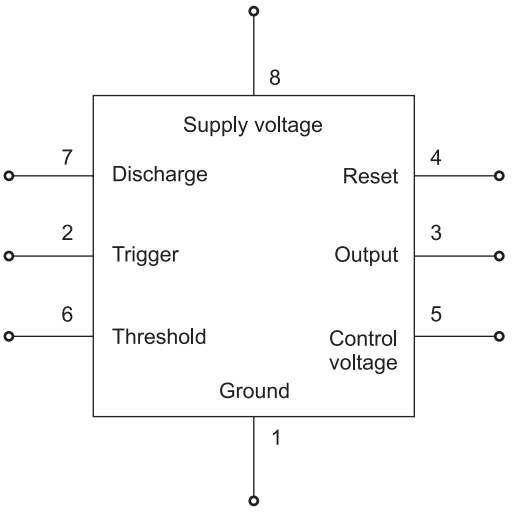


Fig. 29.2 *Pin diagram of 555 timer*

- The comparator's output sets or results the *flip-flop* (*F*/*F*) which feeds the output stage. The F/F operates as

  $R = 1, S = 0$, output = 0

  $R = 0, S = 1$, output = 1

The F/F also operates a transistor which when driven low, discharges a timing capacitor (external).

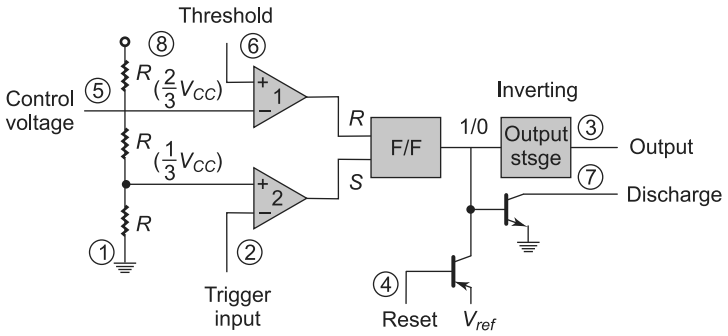


Fig. 29.3 *Internal details of IC-555 timer*

29.3 ASTABLE OPERATION

A common application of the 555 timer is as astable multivibrator or *clock circuit*. Figure 29.4 shows a stable circuit built using two external resistors and a capacitor, which sets the timing in intervals of the output.

The capacitor begins to charge from the dc source V_{CC}. When the voltage of the threshold pin 6 tends to increase beyond 2/3 V_{CC}, the comparator 1 saturates and its output triggers the flip-flop and so the output at pin 3 goes low. At the same time, the transistor becomes 'on' causing the output at pin 7 to discharge the capacitor through R_2 at time constant $\tau_2 = R_2C$.

As the capacitor voltage which is the trigger input at pin 2 falls below (1/3) V_{CC}, the comparator 2 output causes the flip-flop to reset, the output at pin 3 becomes high and the transistor goes 'off'. The capacitor now begins to charge through R_1 and R_2 at the time constant $\tau_1 = (R_1 + R_2)C$. The process then repeats continuously.

The output waveform and capacitor charging and discharging are shown in Fig. 29.5.

By writing the exponential expression for R_2C discharging and $(R_1 + R_2)$ charging from V_{CC}, we can find T_{high} and T_{low} periods. These results are,

$T_{high} \approx 0.7\ (R_1 + R_2)C$; exact 0.7 is 0.639

$T_{low} \approx 0.7\ R_2C$

The oscillation period

$$T = T_{high} + T_{low}$$

The oscillation frequency

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)C} \qquad (29.1)$$

$$\text{Duty cycle} = \frac{T_{high}}{T_{high} + T_{low}} = \frac{R_1 + R_2}{R_1 + 2R_2}$$

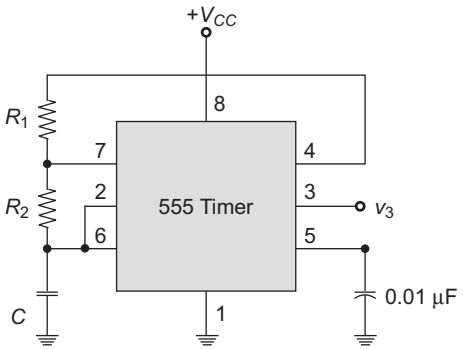


Fig. 29.4 *Astable operation of IC-555 timer*

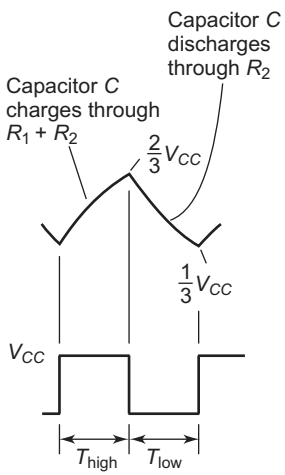


Fig. 29.5 *Output waveform and capacitor charging and discharging cycle*

$$= \frac{R_1 + R_2}{R_1 + 2R_2} \text{; less than } 50\% \tag{29.2}$$

Derivation of Charging and Discharging Time

❑ **Discharging** $v_c(t_1) = \frac{2}{3}V_{CC}\, e^{-t_1/\tau_1} = \frac{1}{3}V_{CC}$

$$2e^{-t_1/\tau_1} = 1, \quad \ln 2 - \frac{t_1}{\tau_1} = 0 \text{ or } t_1 = \tau_1 \ln 2 \tag{29.3}$$

❑ **Charging** $v_c(t) = V_{CC} + Ae^{-t/\tau_2}$

At t_2, $v_c(t_2) = V_{CC} + Ae^{-t_2/\tau_2} = \frac{1}{3}V_{CC} \quad \Rightarrow A = -\frac{2}{3}V_{CC}$

$$v_C(t_2) = V_{CC} - \frac{2}{3}V_{CC}\, e^{-t_2/\tau_2} = \frac{2}{3}V_{CC}$$

$$1 - \frac{2}{3}V_{CC}\, e^{-t_2/\tau_2} = \frac{2}{3}$$

$$2e^{-t_2/\tau_2} = 1$$

$$t_2 = \tau_2 \ln 2 \tag{29.4}$$

29.4 MONOSTABLE OPERATION

In monostable operation, a trigger (negative edge) produces a high output, which lasts for a time interval depending on *RC*. The 555 timer connected for monostable operation is shown in Fig. 29.6(a).

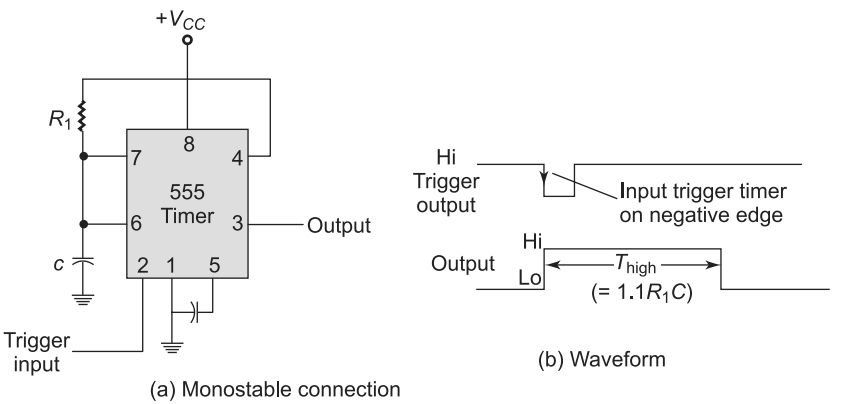


Fig. 29.6 *Monostable operation of IC-555 timer*

A negative edge trigger is applied at pin 2. Comparator 2 and F/F cause the output at pin 3 to go high, the transistor is 'off', and the capacitor begins to charge through R_1 at $\tau_1 = R_1C$. During this period, the

output stays high. So the voltage at pin 6 resistor reaches $(2/3)V_{CC}$, the output goes low, and the transistor discharges the capacitor. The output stays low afterwards.

The output stays high till the capacitor charges to $(2/3)V_{CC}$. This time is

$$T_{\text{high}} = 1.1\ R_1C \tag{29.5}$$

Derivation

During charging of the capacitor,

$$v_c(t) = V_{CC}\ (1 - e^{-t/R1C}) \tag{29.6}$$

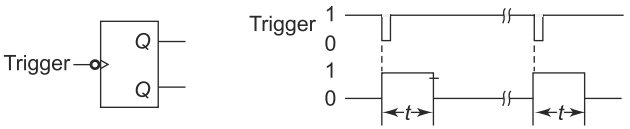
At T_h $$v_c(t) = \frac{2}{3}V_C \tag{29.7}$$

Substituting in Eq. (29.6), we find

$$T_h = CR_1\ln 3 = 1.1\ R_1C$$

The standard logic symbol for a monostable operator is shown in Fig. 29.7(a). The input is labelled *TRIGGER*, and the output is Q. The complement of the Q output may also be available at $\overline{Q}$. The input trigger circuit may be sensitive to either a positive or negative trigger. In this case, it is negative-edge-triggered. Usually, the output at Q is low when the circuit is in its stable state.

A typical set of waveforms showing the proper operation of a monostable circuit is shown in Fig. 29.7(b). In this case, the circuit is sensitive to a negative trigger at the trigger input, and the output is low when the circuit rests in its stable state. Once triggered, Q goes high, remains high for a predetermined time t, and then switches back to its stable state until another negative trigger appears at the trigger input.



(a) Logic symbol (b) Waveforms

Fig. 29.7 *Monostable circuit*

Example 29.1

For a 555 timer connected as astable multivibrator,

$R_1 = R_2 = 7.5\ \text{k}\Omega$, $C = 0.1\ \mu\text{F}$, $V_{CC} = 5\ \text{V}$

Calculate the frequency of operation and sketch the output waveform.

Solution

$$T_{\text{h}} = 0.7\ (R_1 + R_2)C = 0.7 \times 15 \times 10^3 \times 0.1 \times 10^{-6}$$

$$= 1.05\ \text{ms}$$

$$T_1 = 0.7\ R_2C = 0.525\ \text{ms}$$

$$T = 1.05 + 0.525 = 1.575\ \text{ms}$$

$$f = \frac{1}{T} = \frac{10^3}{1.575} = 635\ \text{Hz}$$

$$V_{\text{oh}} = 5\ \text{V}$$

$$V_{ol} = 0.2 \text{ V}$$

The output waveform is drawn in Fig. 29.8.

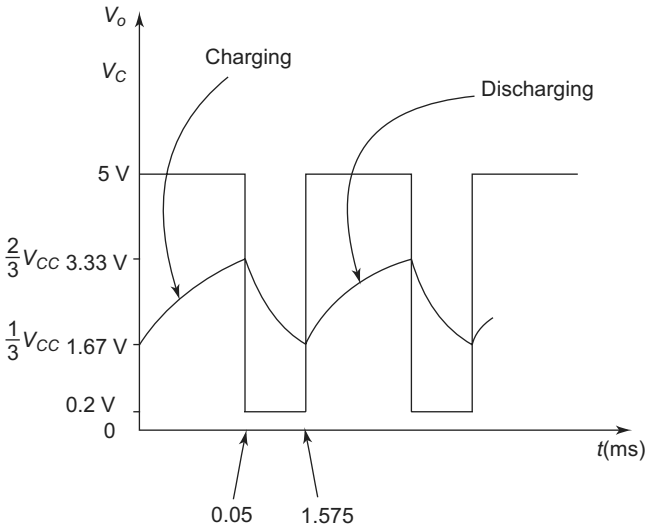


Fig. 29.8

Example 29.2

In Example 29.1, what should be the value of C for the astable frequency of 300 kHz?

Solution

$$T = 0.7\,(R_1 + R_2)C$$

$$f = \frac{1.44}{(R_1 + 2R_2)C} = \frac{1.44}{22.5 \times 10^3 C} = 300 \times 10^3$$

$$C = \frac{1.44}{22.5 \times 300 \times 10^6} = 0.213\ \mu\text{F}$$

Example 29.3

For the monostable multivibrator of Fig. 29.6, R_1 = 75 kΩ; calculate C for one shot high period of 25 μs.

Solution

$$T_h = 1.1\ R_1 C$$

$$25 \times 10^{-6} = 1.1 \times 7.5 \times 10^3 C$$

or

$$C = \frac{25 \times 10^{-6}}{1.1 \times 7.5 \times 10^{-3}} = 3 \text{ nF}$$

Summary

- Clock and timing circuits are introduced.
- Analysis and operation of IC 555 timer with block diagrams have been explained.

Exercises

Review Questions

1. What is a timer? (in general)
2. In brief, introduce the 555 work as an oscillator.
3. What is the internal structure of 555 timer according to its operation?
4. What are time-constant changes in different operations?
5. Explain the importance of threshold and discharge pins of the 555 timer.

Problems

1. A 555 timer is connected for astable operation at 400 kHz. Calculate the value of C if $R_1 = R_2 = 8$ kΩ.
2. Draw the circuit of a monostable 555 timer to produce a single pulse of time period 25 μs. If $R_1 = 8$ kΩ, what value of C is needed?
3. Sketch the input and output waveforms for monostable (one shot) 555 timer triggered by 12 kHz clock for $R = 5.45$ kΩ and $C = 5$ nF.

Multiple-Choice Questions

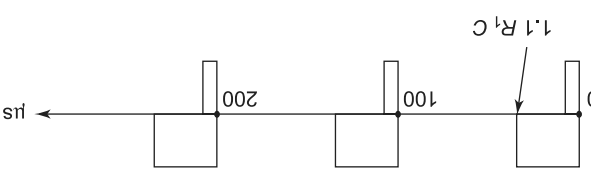
1. The supply voltage range of 555 timer is
   (a) 5 to 22 V (b) 10 to 30 V (c) 5 to 18 V (d) none of these
2. The 555 timer output is compatible with
   (a) N-MOS (b) P-MOS (c) C-MOS (d) none of these
3. Which flip-flop is used in the 555 timer?
   (a) *SR* F/F (b) *JK* F/F (c) *T* F/F (d) *D* F/F
4. In the 555 timer, monostable operation of pulse width of the output is shown in the equation
   (a) $t_p = 2.1\ R_1C_1$ (b) $t_p = 3.2\ R_1C_1$ (c) $t_p = 4\ R_1C_1$ (d) $t_p = 1.1\ R_1C_1$
5. The frequency oscillation of a 555 timer in a stable mode is given by
   (a) $f = \dfrac{1.44}{(R_1 + 2R_2)C_1}$ (b) $f = \dfrac{2.33}{(R_1 + 2R_2)C_1}$ (c) $f = \dfrac{3.12}{(R_1 + 2R_2)C_1}$ (d) $f = \dfrac{4.34}{(R_1 + 2R_2)C_1}$
6. In the bi-stable multivibrator, the stable state is
   (a) one stable state (b) two stable states (c) three stable states (d) none of these
7. A four stable multivibrator is commonly used in a
   (a) square waveform (b) sinusoidal waveform
   (c) triangular waveform (d) sawtooth waveform
8. In the monostable multivibrator, frequency of oscillation is
   (a) $f = \dfrac{1}{1.50\ RC}$ (b) $f = \dfrac{1}{1.38\ RC}$ (c) $f = \dfrac{1}{2.34\ RC}$ (d) $f = \dfrac{1}{3.33\ RC}$

9. In the 555 timer, the upper comparator is connected with
   (a) trigger terminal (b) discharge terminal (c) threshold terminal (d) none of these
10. A bistable multivibrator is normally called
   (a) oscillator (b) voltage regulator (c) voltage controller (d) flip-flop

Answers

Problems

1. 15 μF
2. 2.8 nF
3.



Multiple-Choice Questions

1. (c) 2. (c) 3. (a) 4. (d) 5. (a) 6. (b) 7. (a) 8. (b) 9. (c) 10. (d)

Communication Engineering

chapter 30

Goals & Objectives

- Introduction of electrical technology and communication systems
- Discussion of various types of modulations—amplitude, AM detection, frequency and phase modulation
- Explanation of digital modulation and digital communication
- Types of data transmission—asynchronous and synchronous transmission
- Introduction of different types communications—transmission lines, radio waves, antennas, television and satellite communication
- Telephone network and principle operation of mobile phone
- Discussion of various types of communications—microwave communications and optical fibre communication and its applications

30.1 INTRODUCTION

In electrical technology, one of the greatest applications is communication systems. It enhances the people's lives to a great extent. Today, we enjoy satellite television, fax machine and cellular phones, etc. Communication systems include the generation, storage and transmission of information. The basic elements of communication systems are transmitter, receiver and communication channels. We begin with analog communication, because many digital communication techniques require analog technology to function.

30.2 ELEMENTS OF COMMUNICATION SYSTEMS

Communication systems are used to transfer information from a generation point to the place where it is needed/processed. The information at the generation point is not in the form that can travel long distance through the channel. So a device called a *modulator cum transmitter* is needed. In the receiving end, the information must undergo the reverse process such as decoding/demodulation. The source is mostly analog and sometimes it may be digital. Fig. 30.1 shows the very basic elements of a communication system.

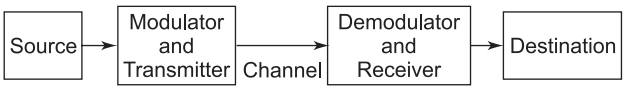


Fig. 30.1 *Communication system*

Common examples of sources are analog audio, video, signals from measuring devices in the field, and of course some digital data. The source can be described by its signal frequency, like an audio signal is in the range at 20 Hz to 20 kHz and a video signal in the ranges from dc to 4.2 MHz. Digital signals have different bandwidths depending on transmission rate and the method used to convert binary ones and zeroes to electrical signals.

Communication channels can be a pair of conductors, optical fiber or just free space. The signal can be directly sent through a twisted-pair telephone cable. But the radio link through free space cannot be used directly for audio signals; instead an antenna of great height would be required. In this case it is a carrier signal whose frequency is such that it will travel for long distance through a channel. A carrier wave will be altered/modulated by the information signal in such a way that the information can be recovered at the destination. Here, the information signal is called the modulated signal. The carrier signal frequency is much higher than information signal frequency.

30.3 MODULATION

The carrier is a sine wave, and the information signal may be any type of wave form. The instantaneous amplitude of the information signal is used to vary some parameters of the carrier.

The sine-wave carrier signal is represented as

$$e(t) = E_c \sin(\omega_c t + \theta) \tag{30.1}$$

$e(t)$ = instantaneous voltage as a function of time
E_c = peak magnitude
ω_c = frequency, rad/s, and $\omega_c = 2\pi f_c$
t = time
θ = phase angle in radians

In modulation, the amplitude E_c, frequency ω_c and phase θ can be varied in accordance with the instantaneous values of the modulating signal. The modulated signal is not a single frequency signal and it occupies a great bandwidth. In addition, the bandwidth of the modulated signal depends on the modulating-signal frequency range and modulating scheme in use. Table 30.1 gives the commonly used frequency ranges and its application.

Table 30.1 *Frequency ranges with application*

Frequency range		*Application*
Super high frequencies 3 GHz–30 GHz	→	Radar
Ultra high frequencies 300 MHz–3 GHz	→	Communication satellites, cellular phones, personal communication systems
Very high frequencies 30 MHz–300 MHz	→	TV and FM broadcast
High frequencies 3 MHz–30 MHz	→	Short-wave broadcast commercial
Medium frequencies 300 kHz–3 MHz	→	AM broadcast
Low frequencies 30 MHz–300 kHz	→	Navigation, submarine communications
Very low frequencies 3 kHz–30 kHz	→	Submarine communications, navigation
Voice frequencies 300 Hz–3 kHz	→	Audio, submarine communication, navigation
Extremely low frequencies 30 Hz–300 Hz	→	Power transmission

The wavelength of the signal is inversely proportional to frequency of the signal, i.e.,

$$v = f\lambda$$

v = velocity of the wave in meters per second
f = frequency of the wave in hertz
λ = wavelength in meters.

Low frequency signals are some times called *long-wave*, high frequencies corresponds to *short wave*, and so on. And of course, the term *microwave* is used to describe the signals in gigahertz range.

30.3.1 Amplitude Modulation (AM)

An AM signal can be produced by using the instantaneous amplitude of the information signal (modulating signal) to vary the peak amplitude of higher frequency carrier. Figure 30.2 shows a modulating signal (sine wave for simplicit of the carrier signal of much higher frequency and the modulated signal. It is seen that envelopes of the peaks of the modulated signal resemble the modulating signal.

Normally, the ratio between carrier frequency and modulating signal frequency is a few thousands. The AM is not a simple linear addition of the two signal instead AM is a nonlinear process.

As the amplitude of a sine wave is a positive quantity, the amplitude variation cannot be sinusoidal. To overcome this problem, a constant quantity is added to the modulating signal which then has the form

$$E_c + E_m \sin \omega_m t,\ E_c \geq E_m \tag{30.2}$$

This signal has positive value only. It is multiplied with the carrier wave $\sin \omega_c t$ to get the modulating signal.

$$e(t) = (E_c + E_m \sin \omega_m t) \sin \omega_c t \tag{30.3}$$

or

$$e(t) = E_c \sin \omega_c t + E_m \sin \omega_m t \sin \omega_c t \tag{30.4}$$

where E_c = peak amplitude of carrier in volts
E_m = peak amplitude of modulating signal in volts
ω_c = carrier frequency in rad/s

ω_m = modulating frequency rad/s
$e(t)$ = instantaneous value of the modulated signal in volts

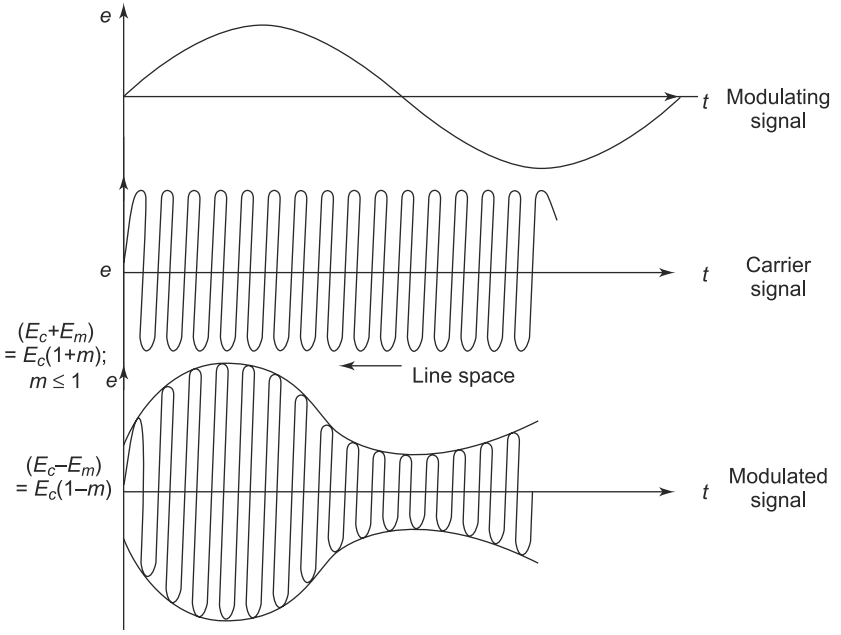


Fig. 30.2 *Amplitude modulation*

We can express Eq. (30.4) as

$$e(t) = E_c \sin \omega_c t + \frac{1}{2} E_m \cos (\omega_c - \omega_m)t - \frac{1}{2} E_m \cos (\omega_c + \omega_m)t \tag{30.5}$$

Carrier Difference frequency Sum frequency

The amount by which the carrier amplitude gets modified by the modulating signal depends on the *modulation index* defined as

$$m = \frac{E_m}{E_c} \tag{30.6}$$

where $m \leq 1$.

The modulated signal (Eq. 30.4) can be expressed in terms of the modulation index as

$$e(t) = E_c(1 + m \sin \omega_m t) \sin \omega_c t \tag{30.7}$$

As shown in Fig. 30.1, upper envelop in the modulated signal is

$$E_c(1 + m \sin \omega_m t) \tag{30.8}$$

and the lower envelop is

$$-E_c(1 + m \sin \omega_m t) \tag{30.9}$$

It is easily seen that the maximum magnitude of the envelop is

$$E_{\max} = E_c(1 + m) \tag{30.10}$$

And minimum magnitude is

$$E_{\min} = E_c(1 - m) \tag{30.11}$$

as shown in Fig. 30.1. It follows from these equations that

$$m = \frac{E_{\max} - E_{\min}}{E_{\max} + E_{\min}} \tag{30.12}$$

In terms of modulation index, the modulated signal of Eq. (30.5) can be written as

$$e(t) = E_c \sin \omega_c t + \frac{1}{2} mE_c \sin (\omega_c + \omega_m)t - \frac{1}{2} mE_c \sin (\omega_c - \omega_m)t \tag{30.13}$$

Carrier Upper side band Lower side band

For a single modulating frequency, the frequency component magnitude of the modulated signal are shown in Fig. 30.3. This representation is known as *frequency spectrum* or *just spectrum*.

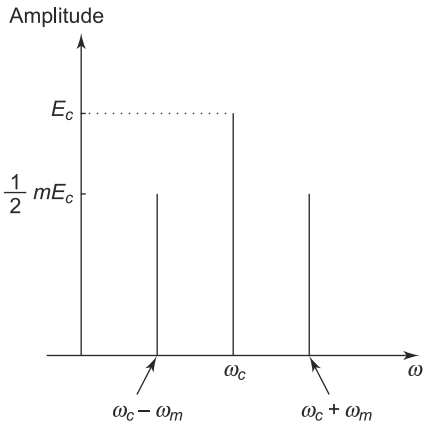


Fig. 30.3 *AM spectrum for single* ω_m

Spectrum Power

We will consider a single modulating frequency as in Fig. 30.3.

$$\text{Power, } P = \frac{V^2}{R}$$

It is convenient to take $R = 1\ \Omega$ for comparison. Actual power can be found by dividing *pu* power by R. From Fig. 30.3

$$P_{t(\text{total})} = P_{C(\text{carrier})} + P_{\text{LSB(lower side band)}} + P_{\text{USB (upper side band)}} \tag{30.14}$$

$$P_C = \left(\frac{E_c}{\sqrt{2}}\right)^2 = \frac{1}{2} E_c^2$$

$$P_{\text{LSB}} = P_{\text{USB}} = \left(\frac{\frac{1}{2} mE_c}{\sqrt{2}}\right)^2 = \frac{1}{8} m^2 E_c^2 = \frac{1}{4} m^2 P_c$$

$$P_t = P_c + 2 \times \frac{1}{4}\, m^2 P_c = \left(1 + \frac{1}{2} m^2\right) P_c \tag{30.15}$$

or
$$\frac{P_t}{P_c} = \left(1 + \frac{1}{2} m^2\right) \tag{30.16}$$

For $m = 1$ (maximum permissible)

$$P_t = 1.5\, P_c \text{ or } 50\% \text{ more than } P_c \tag{30.17}$$

The modulating signal (like audio and video) is a band of frequencies with varying amplitude of $\Delta\omega$ components. The spectrum of the modulating signal called the base band is switched in Fig. 30.4(a). The corresponding spectrum of the modulated signal is presented in Fig. 30.4(b). It comprises the carrier and lower and upper sidebands which are mirror in age of each other. The transmission bandwidth needed is 2 ω_u times the base bandwidth.

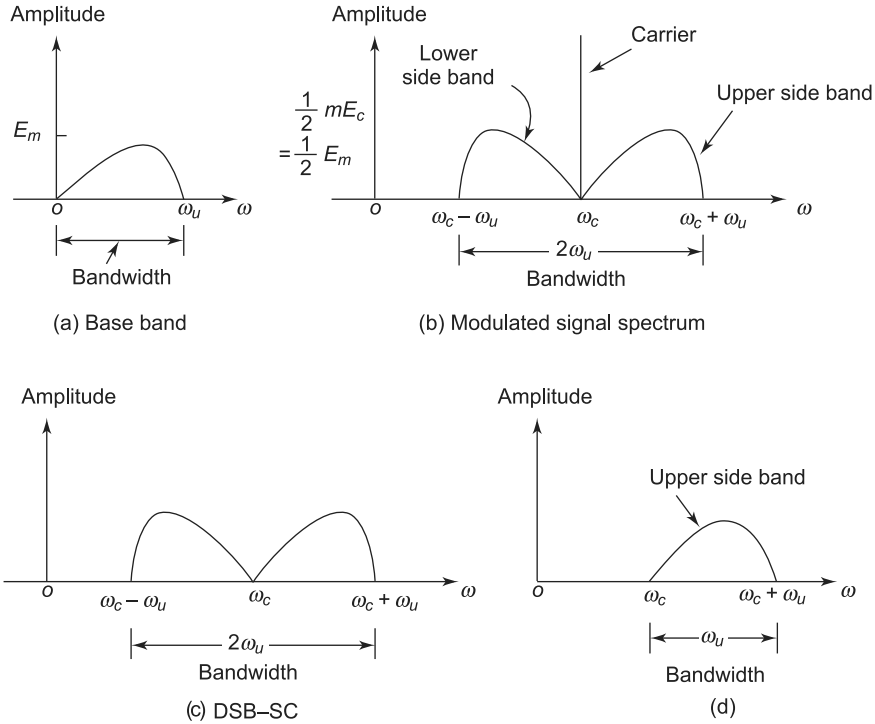


Fig. 30.4 *Modulating signal*

The carrier need not be transmitted, only two side bands are transmitted. This is called double side-band suppressed carrier, DSB–SC as shown in Fig. 30.4. DSB-SC requires less transmission power but the carrier has to be generated at the receiving end by a high-frequency oscillator. As a result DSB–SC detector is therefore more complicated than normal AM detector. This type of modulation is used in conjunction with FM (frequency modulation) stereo broadcasting.

As upper and lower side bands are mirror images of each other it is sufficient to transmit only the upper side band as shown in Fig. 30.4(d). This is called *Single Side Band (SSB)* signal. The detector at the receiving end becomes quite complicated generally not used for commercial broadcast.

Vestigial Side Band (VSB) Signal

In this type of AM comprises carrier, upper side band and the rising part of the lower side band (called vestige). VSB modulation is used in television video transmission. The base band of 4 MHz (megahertz) is shown in Fig. 30.5. The television stations are attached to a bandwidth of 6 MHz. A particular station is allotted the band 60–66 MHz. It employs a carrier of $f_c = 61.25$ Hz above which the upper side band occupies 4 MHz. The carrier is transmitted along with the side band. The vestige component is accommodated in 60–61.25 as shown in Fig. 30.5. The remaining part of the allotted spectrum is used for audio signal which is FM with carrier frequency (central) of 65.75. The difference between the two carrier frequencies is 4.5 MHz. There is a narrow guard band between video and audio, not shown in the figure.

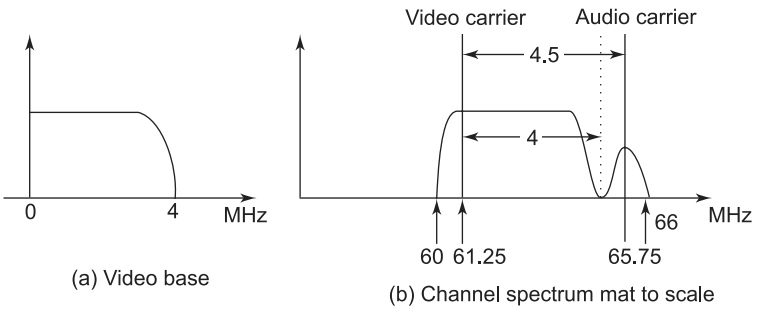


Fig. 30.5 *VSB signal*

Amplitude Modulation Circuit

Amplitude modulation is achieved by feeding the carrier to an amplifier whose gain varies in accordance with the modulating frequency. A BJT AM circuit is drawn in Fig. 30.6 in which the carrier signal e_c is fed to the base and modulating signal e_m to the emitter. The large modulating signal causes the emitter small signal resistance r_e to vary accordingly as

$$r_e = \frac{v_{be}}{i_e} = \frac{r_\pi}{(1+\beta)} \qquad (30.18)$$

As we have seen, the amplifier gain depends on r_e. Change in r_e requires a large e_m signal but the carrier amplitude must meet the condition $m \le 1$, m = modulation index.

To avoid the problem caused by coupling and bypass capacitor, a dc amplifier modulator is employed: beyond the scope of this book.

For *broadcasting* the audio modulated signal, a large power has to be fed to the antenna. At the output stage therefore, a class-C power amplifier is employed. In fact the modulation is carried out at the power-amplification stage. The carrier is fed to the

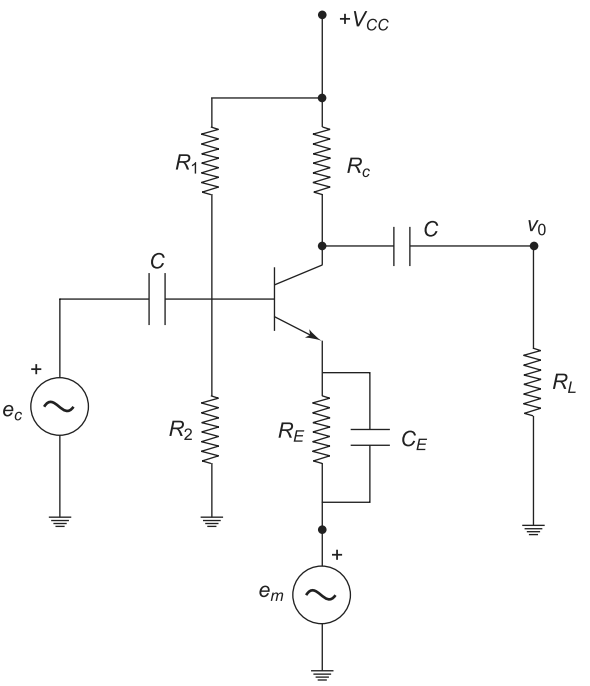


Fig. 30.6 *AM modulator*

base and the modulating signal to the emitter, and the coupling must be though transformers for high power efficiency.

As the conduction period in a class-C amplifier is only about 90°, its output is positive modulated pulses of carrier frequency as shown in Fig. 30.7. In order to get the complete carrier modulated signal, the truncated signal is fed to the *tank circuit* (*LC* parallel circuit) as shown in the figure. At each pulse, the capacitor gets charged and in the off period it discharges through *L*, generating the negative half pulse of the same height as input pulse, thereby creating the modulated signal as shown in the figure.

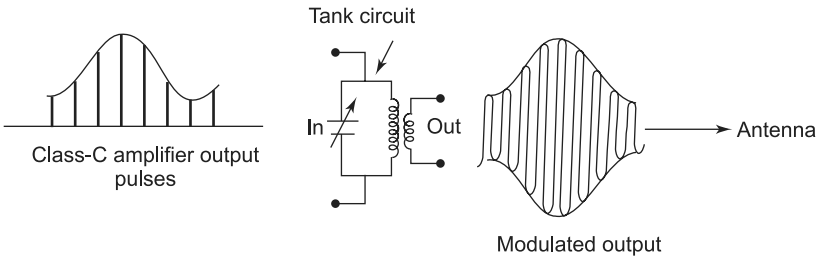


Fig. 30.7 *Stages in high power AM transmission*

Depending upon the station size and channel length (distance) the power to be fed to the antenna is in the range of hundred of watts, even above 100 kW. For such powers transistors can not be used as their power handling capacity is much smaller. Therefore, a transmitting station tube (*triode*) version of the class-C amplifier is used. The RF carrier is fed to the grid of the tube and the modulating signal in series with the grid bias. The circuitry will not be described here.

30.3.2 AM Detection (Demodulation)

To recover the information from AM signal at the receiving end, the signal envelop has to be detected. The process of detection or demodulation is simpler than modulation. The signal is passed through a diode to cut-off the lower half and the peaks detected and smoothed out by a parallel *RC* circuit as shown in Fig. 30.8(a). The diode is assumed to be ideal. It is seen that the voltage v_d always equals the capacitor voltage.

As $v(t)$ rises to first peak, so does the capacitor voltage and the capacitor charges to the peak value. As $v(t)$ falls below peak, the diode stops conducting and capacitor begins to discharge through the resistor *R*. The voltage v_a falls at peak when the time constant $t = RC$ as shown in Fig. 30.8(b). As the next wave of $v(t)$ rises above v_d, the diode begins to conduct till the peak. The process then repeats.

It is seen from the figure the v_d follows the modulated wave envelop except for small variation at carrier frequency which can easily be filtered out. In order that the magnitude of the variation is small, the time constant *RC* must meet the condition

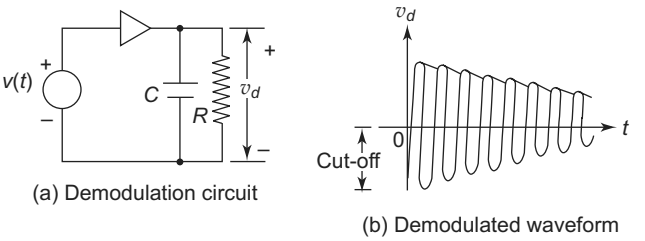


Fig. 30.8 *Demodulation process*

$$RC >> T_C = \frac{1}{f_c} = \frac{\omega_c}{2\pi}\ ;\ T_C = \text{carrier time period} \tag{30.19}$$

However, if the time constant is very large, in the nonconducting time v_d drops very slowly and may miss the next peak. Thus, the modulating envelop may not be detected. This situation is avoided by the condition.

$$RC << T_m = \frac{1}{f_m} = \frac{\omega_m}{2\pi}, \; T_m = \text{time period of modulating signal} \tag{30.20}$$

These two conditions can be combined as

$$\frac{\omega_c}{2\pi} \ll RC \ll \frac{\omega_m}{2\pi} \tag{30.21}$$

The detected envelop is indeed

$$v_m(t) = E_c + m\, E_c \sin \omega_m t \tag{30.22}$$

The dc content E_c can be filtered out by a simple RC low-pass filter.

30.3.3 Frequency (FM) and Phase (PM) Modulation

The frequency and phase of the carrier signals are closely related, since frequency is the rate of change of phase angle. If either frequency or phase is changed in a modulation system, the other will change as well. FM is extensively used for radio broadcasting. The most important advantage of FM or PM over AM is the possibility of a greatly improved signal-to-noise ratio. But FM signal may occupy much larger bandwidth than that required for an AM signal.

In FM, the frequency of the modulated signal varies with the amplitude of the modulating signal. In PM the phase varies directly with the modulating signal amplitude. In contrast to AM, the amplitude and the power in FM or PM signal do not change with modulation. The FM and PM modulations can be accomplished at low power levels. The FM signal can be expressed as

$$e(t) = A \sin [\omega_c + k_f e_m(t)]\, t \tag{30.23}$$

The sine-wave modulating signal $k_f e_m(t)$, the carrier and the frequency-modulated signal are exhibited in Fig. 30.9.

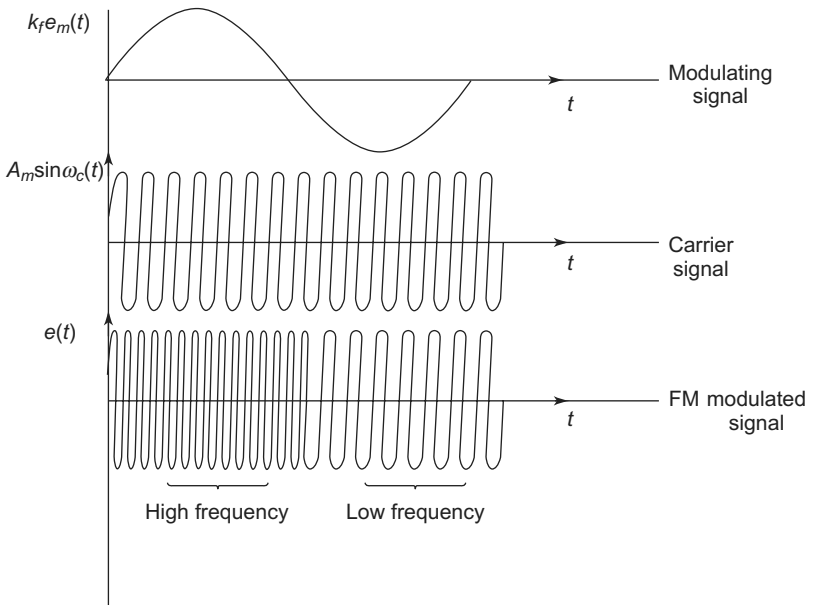


Fig. 30.9 *Frequency modulation*

The PM signal can be expressed as

$$v(t) = A \sin [\omega_c + \phi(t)] = A [\sin \omega_c t + k_p e_m(t)] \tag{30.24}$$

FM and PM are generally known as *angle modulation*.

The frequency of the modulated signal is varied in accordance with instantaneous values of modulating signal $k_f e_m > 0$, the modulated signal frequency is greater than carrier frequency and if $k_f e_m < 0$, the modulated frequency is less than carrier frequency. And the phase is advanced if $k_f e_m > 0$ and it is lagging if $kfe_m < 0$. The FM can be generated by simply with a *voltage controlled oscillator* (VCO). The frequency of a VCO is controlled by the input voltage. It increases and decreases with input voltage. The VCO with zero input voltage is set to produce carrier frequency. If the modulating frequency signal is applied at the input, VCO output is the frequency-modulated signal.

Modulation Index

From Eq. (30.23) , the modulated frequency is

$$2\pi f(\text{mod}) = 2\pi f_c + k_f e_m(t) \tag{30.25}$$

For sinusoidal modulation,

$$2\pi f(\text{mod}) = 2\pi f_c + k_f E_m \sin 2\pi f_m t$$

or
$$f(\text{mod}) = f_c + k'_f E_m \sin 2\pi f_m t;\ k'_f = \frac{k_f}{2\pi} \tag{30.26}$$

The frequency deviation is

$$f_{\text{div}} = k'_f E_m \sin 2\pi f_m t \tag{30.27}$$

The maximum frequency deviation is

$$\zeta = f_{\text{div}}(\text{peak}) = k'_f E_m \tag{30.28}$$

The modulation index is defined as

$$m_f = \frac{\zeta}{f_m}$$

or
$$m_f = \frac{\text{Peak frequency deviation}}{\text{Modulating frequency}} \tag{30.29}$$

The maximum permissible value of frequency deviation is 75 kHz for commercial FM broadcasting.

FM Bandwidth

The precise expression for bandwidth of FM is quite involved. An approximate relationship is

$$\text{BW}_{\text{FM}} \approx 2(\zeta + f_u) \tag{30.30}$$

where f_u = upper frequency of modulating signal bandwidth

ζ = peak frequency deviation, Eq. (30.28)

If $\zeta > f_u$, we refer it as *wideband* FM and if $\zeta < f_u$ it is referred as *narrowband* FM.

30.3.4 FM Demodulation

FM demodulation is accomplished by a Phase-Locked Loop (which is an IC chip). The block diagram of PLL is drawn in Fig. 30.10. It comprises three main parts.

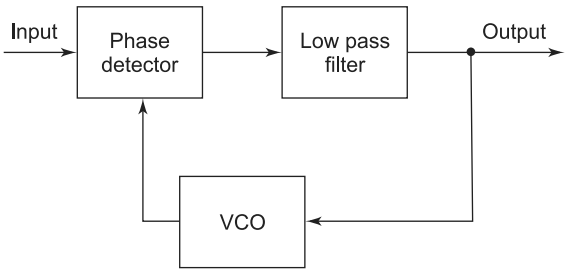


Fig. 30.10 *Phase locked loop*

- *VCO* Voltage Controlled Oscillator whose frequency depends on the input voltage
- *Phase Detector* It produces a voltage proportional to the frequency (or phase) difference between input and VCO frequency
- *Low-pass Filter* It cuts off the high frequencies.

At zero input voltage VCO is set at the carrier frequency. FM signal is applied at PLL input. If the modulating signal is not present, the VCO frequency matches the input frequency, the PLL output is essentially zero. With the modulating signal and the input frequency changes, it is detected by the phase detector and the PLL output voltage changes to cause the VCO frequency to change so as to match the FM signal frequency. The PLL output voltage thus tracks the modulating signal. PLL detects (or demodulates) the FM signal.

Electrical Noise

Noise is a random disturbance that adversely affects the normal working of electronics devices and systems. This is generated due to the fact that the electrical charge is carried in discrete amounts equal to the charge of an electron. The study of noise is important because it gives a lower limit to the size of the electrical signal that can be amplified by a system without significant deterioration in signal quality.

In most cases noise is an undesirable signal. However, noise has some useful applications such as its use as a broadband test signal, or as a cheap source for microwave heating. Besides electrical noise, there are many other types of noises as well. These are:

1. *Acoustic noise* (noise in sound systems in auditoriums)
2. *Hydrodynamic noise* (fluctuations in smooth fluid flow as studied in civil engineering)
3. *Scintillation noise* (in radio receivers due to atmospheric effects)
4. *Round-off noise* (in computation)
5. *Quantisation noise* (in analog to digital conversion process)

Noise in any system can be either from external sources or internal sources. *Internal sources* are within the semiconductor devices, vacuum devices and in the resistors. These noises are thermal, shot, flicker (1/*f*), burst, avalanche noise and dc noise such as offset error in an operational amplifier. Thermal noise is also known as *Johnson noise*. *External noises* are produced by the lightning discharge in the sky, as galactic noise (around 1.42 GHz) produced by hydrogen clouds lying in the intergalactic space, by sun spots on the sun, by human-made objects such as electric mixers, etc. that have universal motors in them and due to coupling from devices such as fluorescent tubes. Some of these noises have their amplitude distribution as Gaussian (thermal and shot) whereas others are non-Gaussian (flicker). Their spectral distribution may also be white (thermal) or nonwhite (flicker).

From the viewpoint of spectrum, all the electrical noise can be divided into two categories: white and coloured noise. *White noise* has equal power spectral density from dc to infinite frequency. This is a theoretical model, which is nonphysical in nature because it means that any white noise process has infinite

noise power. This is not possible for a physical system. In practice, the power density of white-noise sources starts falling beyond about 1013 Hz. For the ease of modelling, thermal noise is taken as white in nature. The *coloured noise* has non-uniform power spectral density. In a communication system noise may get added to the signal passing through the channel. Such a noise is called *Additive White Gaussian Noise (AWGN).* The noise may also get multiplied to the signal; then it is called as *multiplicative noise* which happens in a fading channel.

The measure of noise in communication is the *signal-to-noise ratio (S/N).* It is the ratio of signal to noise power in decibels It is one of the most important specifications of any communication equipment.

The effect of noise can be reduced by reducing the signal bandwidth increasing the transmitting power and low-noise amplifiers for weak signals.

The noise irrespective of the origin is amplitude additive in nature. It, therefore, directly affects the AM signal but the FM signal is immune to noise. Further, in FM, the greater the frequency deviation (and so the bandwidth), more effective is the signal's noise immunisation. Thus wideband FM is superior to narrowband in relation to noise immunity.

Table 30.2 *Comparison between AM and FM*

S. No.	*Characteristics*	*AM*	*FM*
1.	Channel bandwidth	AM has smaller bandwidth, i.e. 2 fm	FM has larger bandwidth because it produces a larger number of side bands
2.	Operating carrier frequency	AM comparatively utilises lower carrier frequency	FM utilises higher carrier frequency (above 30 MHz) because of its higher bandwidth
3.	Transmission efficiency	AM has less transmission efficiency	FM has better efficiency but not better than AM-SC
4.	Noise performance	AM has poor noise performance	FM has better noise performance
5.	Common Channel Interference (CCI)	Due to CCI, distortion occurs in AM	FM is better due to capture effect
6.	Externally generated noise pulses	In AM such tuning is not essential	FM receiver responds slightly to noise pulses generated by external sources but if it is slightly mistuned then its ability to suppress noise pulses is highly reduced
7.	Area of reception	AM covers more distance than FM	FM is limited to distance, that is it can strongly transmit its signal in smaller area; as distance increases signal quality becomes poorer

❑ Additional Information

- A small guard band is provided between FM stations to avoid interference
- FM stations operate in super VHF and UHF frequency ranges, which limits the signal to Line Of Sight (LOS). Individual stations out of LOS can operate at the same frequency.

30.4 TRANSMITTER

A transmitter has to generate a signal with the right type of modulation, with enough power at the proper carrier frequency, and with good efficiency. The output of the transmitter is connected to an antenna. An ideal communication system allows the original information signal to be received exactly, except for a time delay

and the transmitter would be capable of modulating any information signal frequency on the carrier, at any modulation level. Most widely used transmitters are

1. **Full carrier AM transmitters** where the carrier is generated by a frequency synthesiser and amplified to its full output power before modulation takes place
2. **Low level modulation of synthesiser (FM)**
3. **Heterodyne system (SSBSC AM)**

Super-heterodyne Receiver

It is the most widely used form of receiver whose block diagram is presented in Fig. 30.11.

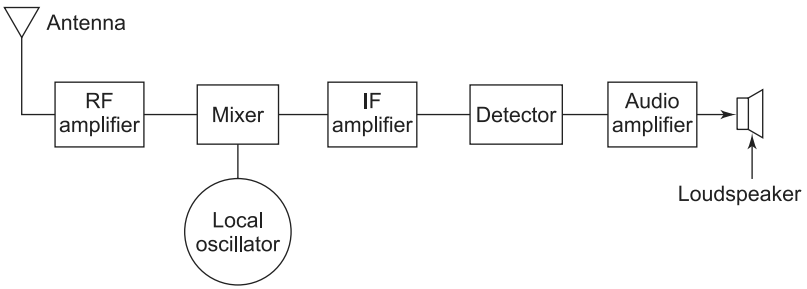


Fig. 30.11 *Schematic block diagram of super-heterodyne receiver*

A receiver has to perform three functions:

(i) Carrier frequency tuning (select desired channel and tune it),
(ii) Filtering (separate desired signal from other signals that entered the receiver), and
(iii) Amplification (to drive loudspeaker or monitor)

A super-heterodyne receiver does all the three functions. Practically, all the AM radio receivers are super-heterodyne receivers. The super-heterodyne receiver has remained in use because its gain, selectivity and sensitivity characteristics are superior to those of other receiver configuration such as Tuned Radio Frequency (TRF) receiver. Heterodyning means mixing two frequencies together in a nonlinear device. Essentially, there are five sections in a superheterodyne receiver: RF section, mixer, IF section, detector, and audio amplifier as shown in Fig. 30.11.

The primary functions of RF amplifier are selecting, band limiting and amplifying the received RF signals. RF amplifier provides some gain at a point of low noise in the receiver. A cheap receiver may not have RF amplifier section. The difference will show up in the performance in areas where signal strength is weak. An RF amplifier also determines the sensitivity of the receiver. Several advantages of including an RF amplifier in a receiver are better Signal-to-Noise (SNR) ratio, improved image frequency rejection and better selectivity.

The mixer stage performs heterodyning operation, which is translation or shifting on the frequency scale. This is a nonlinear device and its purpose is to convert the received RF frequencies to Intermediate Frequency (IF), which is the frequency that lies somewhere in between the RF and information frequencies, hence the name *intermediate*. Mixer includes a local oscillator. The most common Intermediate Frequency used in an AM Broadcast Band (550 kHz to 1650 kHz) receiver is 455 kHz.

The IF amplifier is a tuned amplifier, which is tuned at 455 kHz. Thus, this amplifier selects only 455 kHz and all other frequencies are rejected (or attenuated severely). A tuned amplifier can give good gain up to 30 dB to 40 dB. The IF amplifier stage gives about two-third or more of total receiver gain. The bandwidth of IF stage is ±5 kHz (10 kHz) for an AM Double Side Band (AM DSB) broadcast receiver. Most of the receiver gain and selectivity is achieved in the IF section. It is important to note that although the carrier frequency

changes in this stage but the bandwidth remains unchanged. Thus the original information contained in the envelop remains unchanged.

The purpose of the detector is to extract the original information from the IF signal. Mostly, an envelop detector is preferred for this purpose because it is simple and cheap. The audio amplifier is a power amplifier. An audio amplifier amplifies the recovered information signal such that it can drive the loudspeaker.

Receiver Parameters

Important receiver characteristics are the following:

Selectivity

Selectivity is the ability of a receiver to accept the desired signal frequency while rejecting all adjacent disturbances (undesired signals). The better the receiver's ability to exclude unwanted signals, the better its selectivity. It is usually poor at high frequency. The degree of selectivity is determined by the sharpness of resonance to which the frequency-determining components (band-pass filters) have been tuned. As the frequency to which the receiver is tuned is approached, the input level required to maintain a given output will fall. As the tuned frequency is passed, the input level will rise. Input levels are then plotted against frequency as shown in Fig. 30.12. The steepness of the curve at the tuned frequency indicates the selectivity of the receiver. Typically, this may be expressed as –6 dB at ±2.5 kHz of centre frequency and –60 dB at ±7.5 kHz of centre frequency, and –60 dB at 7.5 kHz of centre frequency.

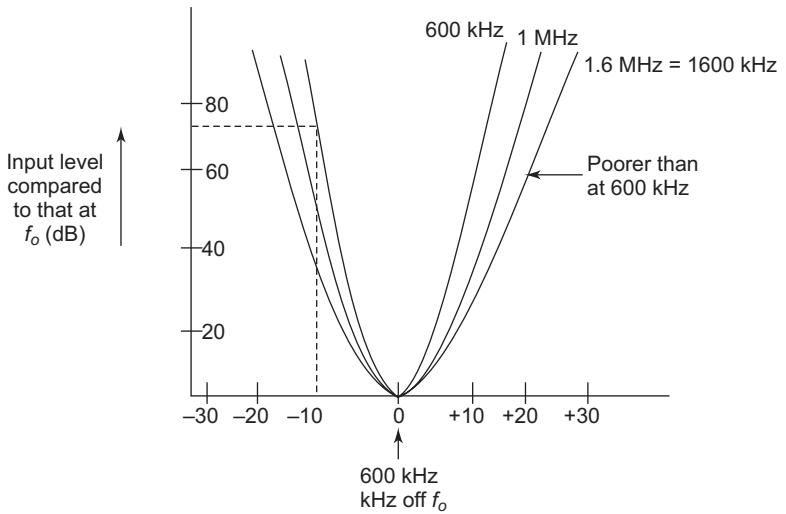


Fig. 30.12 *Selectivity of a typical broadcast receiver*

Sensitivity

Sensitivity is the ability to amplify weak signals or we can say that it is a measure of the receiver's ability to reproduce very weak signals. The weaker the signals that can be produce a certain signal-to-noise (S/N) ratio, the better that receiver's sensitivity rating. Sensitivity is specified as the signal strength in volt/m. Sensitivity is the input signal at antenna that will generate a signal at detector output with the desired SNR (say 20 dB). That is 20 dB above noise power at detector output.

Fidelity

Fidelity is a receiver's ability to reproduce the input signal accurately. Generally, the broader the band-pass, the greater the fidelity. Good selectivity requires a narrow band-pass. Good fidelity requires a wider band-pass to amplify the outer-most frequencies of the sidebands. Hence, most receivers make a compromise between good selectivity and high fidelity.

30.5 AUTOMATIC GAIN CONTROL (AGC) CIRCUIT

The dc component of the output signal of the detector is fed back to IF amplifier and also to RF amplifier as negative feedback. The received signal at the receiver can be of the following three types: weak signal, medium signal, strong signal. Weaker signal at the receiver antenna provides lesser dc voltage from the detector output which is fed back to the IF stage. So there is more gain of IF and RF stage. Thus, more output of the receiver. On the other hand, stronger signal at the receiver antenna provides more dc voltage from the detector output, which is fed back to the IF stage. So there is lesser gain of IF and RF stage and thus, lesser output of the receiver. That is, the AGC circuit automatically increases the receiver gain for weak RF input levels and automatically decreases the receiver gain when a strong RF signal is received. Thus, this circuit smoothens the input signal variations and keeps the output power almost constant.

30.6 DIGITAL COMMUNICATION

Many of the signals involved in today's communication are of digital nature (binary data). Digitising a signal often results in improved transmission quality and great accuracy. Figure 30.13 shows a digital communication system.

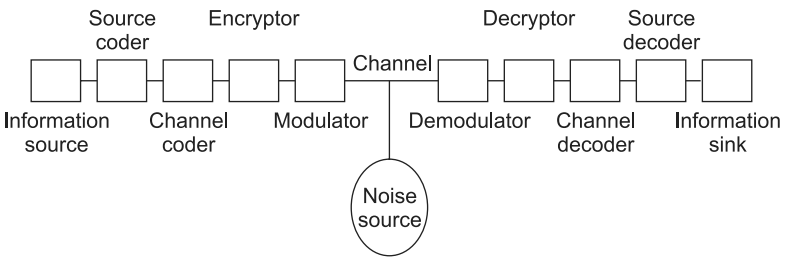


Fig. 30.13 *Schematic diagram of a typical digital communication system*

Source produces a stream of symbols. The source encoder removes the redundancy from the output of the source and performs data compression or source coding. Channel coder adds some redundancy again so as to achieve reliable communication on a noisy channel. Encryptor encodes message as per the chosen algorithm. The modulator prepares a signal for transmission on the physical channel. The channel adds some noise to the signal passing through it. Decryptor and decoder perform the inverse operations corresponding to the encryptor and modulator. The channel decoder performs error detection and correction. The source decoder decompresses the received data and presents the information to the sink.

Digital systems are not immune to noise and distortion, but it is possible to overcome their effect. The main advantage of digital communication is convenience in multiplexing and switching. Time-division multiplexing is quite easy with digital signals and different types of signals can be multiplexed together on the same channel. The bottleneck of the digital communication systems are the complexity and the larger bandwidth requirement.

30.6.1 Pulse Modulation

For transmitting an analog signal by means of a digital signal, the analog signals need to be sampled at least at twice the maximum frequency signal present in it. Then each sample can be expressed as a binary number for transmission. At the receiver side, the transmitted samples can be reconstructed to form a original signal. Figure 30.14 explains the simplest type of sampling, which is a multiplication of analog signal by train of pulses of having amplitude of 1 V. The output pulses will be equal to the amplitude of the analog signal at sampling times. The sampling rate must meet the condition of the sampling theorem: $f_s > 2\, f_u$; f_u being the upper limit of the signal bandwidth. This condition is easily met by modern electronic sampling hardware.

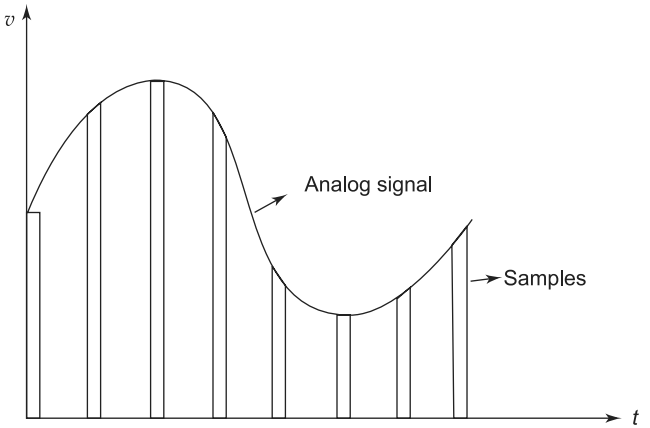


Fig. 30.14 *Sampling*

30.6.2 Analog Pulse Modulation

Sampling is one step of digital communication. The sampled signal in Fig. 30.14 is an example of *pulse amplitude modulation (PAM)* technique. The amplitude of the sampled signal is proportional to the amplitude of the analog signal at the instant at which it is sampled. The other popular pulse modulation technique is *Pulse Duration Modulation (PDM).* Here, the pulse duration is modified according to the amplitude of analog signal at that instant. PAM used in the high powered audio amplifiers is used to modulate AM transmitters and telemetry systems. The PDM is demonstrated in Fig. 30.15.

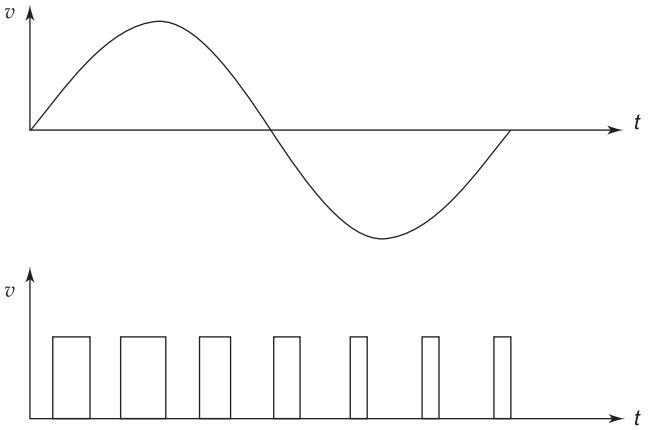


Fig. 30.15 *Pulse duration modulation (PDM)*

Another type of pulse modulation is *Pulse Position Modulation (PPM).* The amplitude and width of the pulse is same here, but their timings vary with the amplitude of original analog signal. It is also used in telemetry systems.

Pulse Code Modulation is the most commonly used digital modulation scheme. In this, the signal voltages are divided in to levels and each is assigned binary number representing the level close to its amplitude. And

this number is transmitted in serial/parallel form. The number of levels available depends on the number of bits used to express the sample value and it is given by $N = 2^m$; N is the number of levels and m is the number of bits per sample. It is also called *quantising*.

30.6.3 Coding and Decoding

The process of converting an analog signal into binary numbers is called coding and the inverse operation, reconstructing the original analog signal from digital signal is called decoding. Both are accomplished in a single integrated circuit device called a *codec*.

30.7 MULTIPLEXING

Multiplexing is a process where multiple analog message signals or digital data streams are combined into one signal and transmitted via transmission medium or simply air. There are two types of multiplexing, *Frequency Division Multiplexing (FDM)* and *Time Division Multiplexing (TDM)*. FDM is in analog form, it means different frequency signals are mixed together and transmitted through a transmitter; in the receiver sides, filter is used to separate desired signal from the group of frequency signals. TDM is used mainly in digital communication. In TDM, each information source is allowed to use all the available bandwidth for a particular periodic or interval. Many signals can be sent on one channel by sending a sample from each source in rotation. TDM is extensively used in telephony.

30.8 PULSE DEMODULATION

A pulse-modulated signal in radar may be detected by a simple circuit that detects the presence of RF energy. Circuits that are capable of this were covered in this chapter in the Sec. 30.3 (detection discussion); therefore, the information will not be repeated here. A radar detector, in its simplest form, must be capable of producing an output when RF energy (reflected from a target) is present at its input.

In communications pulse detectors the modulated waveform must be restored to its original form. There are three basic steps of pulse demodulation: peak detection, low-pass filter and conversion. We need to study only peak detection which is the basic step.

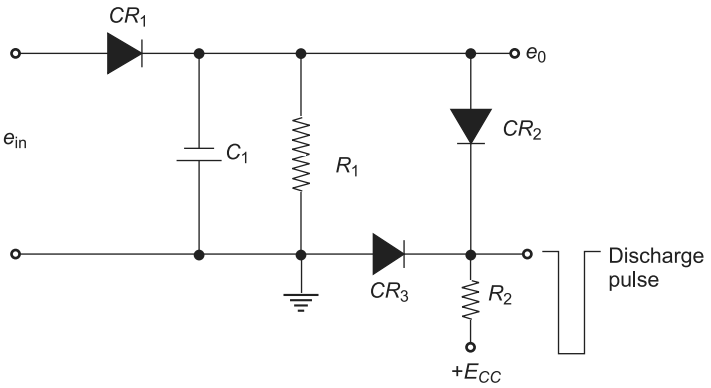
Peak Detection

Peak detection uses the amplitude of a pulse-amplitude modulated (PAM) signal or the duration of a pulse-duration modulated (PDM) signal to charge a holding capacitor and restore the original waveform. The demodulated waveform will contain some distortion because the output wave is not a pure sine wave. However, this distortion is not serious enough to prevent the use of peak detection.

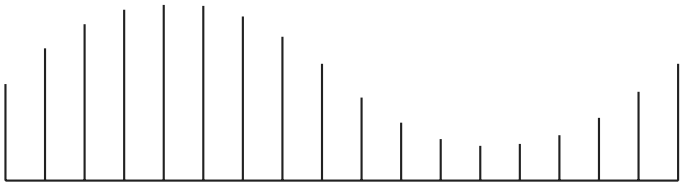
Pulse-Amplitude Demodulation

Peak detection is used to detect PAM. Figure 30.16(a) includes a simplified circuit (*a*) for this demodulator and its waveforms *b* and *c*. CR_1 is the input diode, which allows capacitor C_1 to charge to the peak value of the PAM input pulse. PAM input pulses are shown in *B*. The CR_1 is reverse biased between input pulses to isolate the detector circuit from the input. CR_2 and CR_3 are biased so that they are normally non-conducting. The discharge path for the capacitor is through the resistor R_1. These components are chosen so that their time constant is at least 10 times the inter-pulse period (time between pulses). This maintains the charge on C_1 between pulses by allowing only a small discharge before the next pulse is applied. The capacitor is discharged just prior to each input pulse to allow the output voltage to follow the peak value of the input pulses. This discharge is through CR_2 and CR_3. These diodes are turned on by a negative pulse from a source

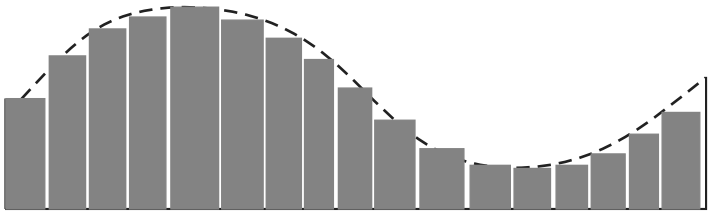
that is time-synchronous with the timing-pulse train at the transmitter. Diode CR_3 ensures that the output voltage is near 0 during this discharge period. Figure 30.16 shows the output wave shape from this circuit. The peaks of the output signal follow very closely the original modulating wave, as shown by the dotted line. With additional filtering, this stepped waveform closely approximates its original shape.



(a) Circuit to peak detector



(b) Amplitude modulated pulses



(c) Peak detection

Fig. 30.16 *Pulse-amplitude detection*

Pulse-Duration Modulation

The peak detector circuit may also be used for PDM. To detect PDM, you must modify (*a*) of Fig. 30.16 so that the time constant for charging C_1 through CR_1 is at least 10 times the maximum received pulse width. This may be done by adding a resistor in series with the cathode or anode circuit of CR_1. The amplitude of the voltage to which C_1 charges, before being discharged by the negative pulse, will be directly proportional to the input pulse width. A longer pulse width allows C_1 to charge to a higher potential than a short pulse. This charge is held, because of the long time constant of R_1 and C_1, until the discharge pulse is applied to diodes CR_2 and CR_3 just prior to the next incoming pulse. These charges across C_1 result in a wave shape similar to the output shown for PAM detection in (c) of Fig. 30.16.

30.9 THE TELEPHONE SYSTEMS

The public switched telephone system is the largest used communication system in the world. The telephone system is public in the sense that anyone can connect to it and is possible for anyone to communicate with anyone else. This is the basic difference from broadcasting system (radio and television) to private communication networks. In this, many interesting developments came like fiber optics and digital signal transmission, but it remains, in many ways, consistent with its origins. That is telephone signalling systems and the voltage and current levels that are found in subscriber lines are still unchanged. Also the compatibility is maintained in most areas of the system, so that simple dial-type telephones can connect with modern data-communication equipment with little change (without change also). Now the telephone network has been adapted to data communication, facsimile and even video. Figure 30.17 shows the basic topology of a typical switched telephone system.

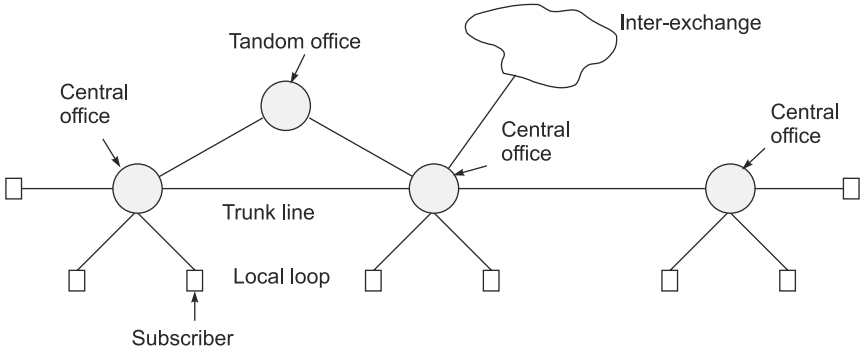


Fig. 30.17 *Typical telephone network*

Each subscriber is connected to a central office, where connection to other intended subscriber is made. Central office represents one exchange, the subscribers under each central office will have same three digits. Subscribers connected to the same central office can communicate with each other by means of the central office switch which can connect any line to any other line. The central office themselves connected together by trunk line, so that interconnection between the customer from different central offices is possible. Tandom Office is the connection medium when there are no trunk-line connections between two central offices. Normally, each individual subscriber telephone is connected to the central office by a single twisted pair of wires. The wires are twisted to help cancel the interference between circuits known as crosstalk Dialing can be accomplished one of the ways. The old fashioned rotary dial functions by breaking the loop circuit at a 10 Hz rate, with the number of interruptions equal to the number dialed. It is called *pulse dialing*. The second is to transmit a combination of two tones for each number. This is known as Dual Tone Multi-Frequency (DTMF) dialing, and it is commonly referred as touch tone dialing.

Finally, telephone instrument use carbon microphones (transmitters) and magnetic earphones (receivers). Carbon microphones have the advantages of simplicity and the ability to generate a relatively large signal voltage without amplification. In modern telephones, carbon microphones have been replaced by electric condenser microphones for improving audio quality. The signal twisted pair line is required to carry both sides of the conversation simultaneously, thus providing full duplex communication. This could be accomplished by simply connecting both transmitters and both receivers in series.

30.10 DATA TRANSMISSION

Transmission may be a serial, where single channel is used to transmit bit by bit, or parallel transmission, in which multiple channels are used to transmit several bits simultaneously. A five-bit "Baud of code" has the advantage of faster data transfer for a given bit rate, compared to codes with more bits per character. It is useful for low-data-rate channels like HF radio. The most common code for communication between micro computers is known as ACCII, which stands for American standard code for information interchange. ASCII is a seven-bit code, so it allows 128 possible ($2^7 = 128$) combinations without shifting.

30.10.1 Asynchronous Transmission

There must be a standard clock speed, and the transmitter and receiver clocks must be in phase with each other, so that the receiver checks the level of the line at the correct times. Data communication schemes may be synchronous or asynchronous depending on how the timing and framing information is transmitted. In asynchronous the frame is based on a single character; while that for synchronous, the frame is much longer block of data. In microcomputers, asynchronous communication is most commonly used. In asynchronous communication, the transmit and receive clocks are free running and set at the same speed. A start bit is transmitted at the beginning of each character, and at least one stop bit is sent at the end of the character. In an asynchronous communication system, the conversion between parallel and serial form is usually performed by an integrated circuit called a Universal Asynchronous Receiver Transmitter (UART). At the transmitting end, a UART converts parallel data from a computer or terminal into serial form, adds start and stop bits, and clocks it out of the correct rate. In receiver side, a UART detect the start bit transition at the beginning of the character, before the receiver and transmitter clocks are in phase. After the start bit has been identified, the signal is sampled once per bit time, approximately in the centre of the bit. Then the UART will assemble the received character in a shift register then transfer it to another register for access by the computer.

30.10.2 Synchronous Communication

Here, the transmitter and receiver are synchronised to the same clock frequency. It is more efficient than asynchronous, because start and stop bits are not necessary. However synchronous communication needs more complex hardware and software. It is mainly used in higher speed communication typical of mainframe computers.

30.10.3 Data Compression

The data consists largely of alphanumeric characters, it is possible that some letters occur more frequently than others. Rather than encoding all letters with the same number of bits as in the ASCII, the more common letters could be encoded with few bits than the less common letters. This technique is called *Huffman coding*. The other data-compression technique is *run-length encoding*. It uses the advantage of the fact that information bits are often repeated.

30.10.4 Encryption

Encryption is an attempt to conceal the information from unintended persons. It means the way in which the data is encoded is not public. So encryption is used when data must be kept secret from unauthorised persons. There are two main of the several types of encryptions, there are two main types—private key and public key. *Private-key method* is more convenient. A long binary number is combined with the message data according to an algorithm that is designed, before the data is transmitted. At the receiver side, the same private key is combined with the received data to reveal the message. In public key encryption technical, recipient issues a public key that can be used by anyone to encode messages for that recipient. Messages can only be encrypted, not decrypted, using the public key. The recipient needs a separate, private key to decode the message. That key does not have to be divulged to anyone.

30.11 DIGITAL MODULATION

Digital signals have become very important in communication. So, to send a digital signals by radio, it is necessary to use a higher frequency carrier wave, just as for analog communication. Because of the sine-wave high-frequency carrier signals, the same three basic parameters are available for modulation amplitude, frequency and phase. Here, the modulator and demodulator collectively described as a *modem*. We have frequency shift keying (FSK), phase shift keying (PSK) and rarely amplitude shift keying (ASK). The simplest digital modulation scheme is FSK. In this, two frequencies are transmitted—one corresponding to binary one, the other to zero. In PSK, the phase of the carrier is shifted by 180° if the bits are changed from one to zero or zero to one. If two continuous bits are same, like 11/00 then no phase shift in the carrier frequency signal. In amplitude shift keying 1 is represented by constant amplitude carrier and 0 by absence of carrier (no carrier transmission). Mathematically the pulse signals ($s(t)$) are.

$$s(t) = \text{A sin } \omega_c t, \text{ for pulse period (1)} \qquad (30.31)$$
$$= 0, \text{ for pulse period (0)}$$

The digital data has physical form of voltage pulses, HIGH for 1 and LOW for 0. All the pulses have uniform time duration and the pulse rate is quite high. In order to transmit the digital data on a channel, it has to be modulated on a carrier of frequency according to the channel form–telephone line, wireless.

Further details will follow in Section 30.6.

30.12 MULTIPLEXING AND MULTI-ACCESS

Most of the communication systems require sharing of channels. When all the signals passing through a given channel originate from the same source, it is called multiplexing of signals. Instead, the signals from several different sources combined on a signal channel is called *multiple-access system*. Multiple-access technique often happens in radio communication. The frequency spectrum can be divided up and part of it allocated to different users on a full-time basis. This is *Frequency Division Multiplexing (FDM)* or *Frequency Division Multiple Access (FDMA).*

On the other hand, the whole of the available spectrum can be allocated to each user for part of the time. This is *Time Division Multiplexing (TDM)* or *Time Division Multiple Access (TDMA).* The third form of multiple access is called *Code Division Multiple Access (CDMA).* Spread spectrum communication allows the multiplexing of signals from different sources CDMA. Here, each transmitter to be assigned a different *Pseudo Noise (PN)* sequence. If possible, an orthogonal sequence should be chosen, that is, the transmitter should never be in the same place at the same time. The PN sequence for the transmitter is given only to the receiver that is to operate with that transmitter, so that the receiver will then receive only the correct transmission and all the other receivers will ignore these signals.

30.13 TRANSMISSION LINES

The signal is sent from the transmitter to receiver by means of a channel. If it is wired, communication transmission lines are the medium to take the signals. The transmission line includes metallic cable and optical fibre. Almost any configuration of two or more conductors can operate as a transmission line. Figure 30.18 shows a coaxial cable, in which the two conductors are connected and are separated by an insulating dielectric, which may be solid or air with a single helical spacer. Coaxial cables are referred to as *unbalanced lines* because they are unsymmetrical with respect to ground. Instead parallel lines are usually operated as balanced lines. Figure 30.18(b) shows parallel line cables.

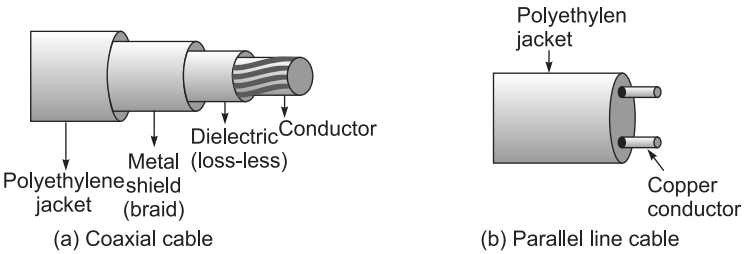


Fig. 30.18 *Transmission lines*

In parallel line cables, two conductors are separated by a thin ribbon of plastic, but air actually forms a good part of the dielectric. Parallel line cables may be an open-wire-type also. Twisted pairs of wires are often used as transmission lines for relatively low frequencies, because of their low cost. Transmission lines are more complex in their behaviour as frequency increases. Besides resistance in the conductors, inductive and capacitive effects become important with higher frequencies and longer lines. The higher the frequency, the larger the series inductive reactance, and the lower the parallel capacitive reactance. The circuit model of a short line is drawn in Fig. 30.19. For a long line, distributive effects have to be accounted for. Its equivalent circuit can be found in this form.

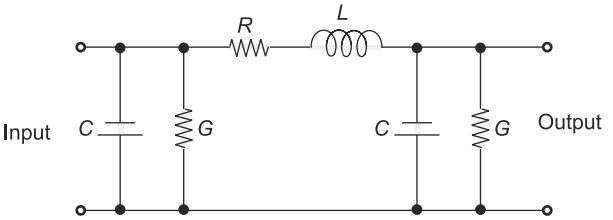


Fig. 30.19 *Model of a transmission line for unbalanced case (short line)*

30.14 RADIO WAVES

Radio waves are one form of electromagnetic radiation, and the other forms are infrared, visible light, ultraviolet, X-rays and gamma rays. The radio waves that propagate are known as *Transverse ElectroMagnetic (TEM)* waves, which means that the electric field, the magnetic field and the direction of travel of the wave are all mutually perpendicular. Electromagnetic radiation can be generated by many different means, but all of them involve the movement of electrical charges. In the case of radio waves, the charges are electrons moving in a conductor or set of conductors called an antenna. Once the electromagnetic waves are launched, they can travel through free space and through many materials. The speed of propagation of EM waves in free space is the same as that of light. Freespace propagation is also of interest in satellite communication.

30.15 ANTENNAS

An antenna is the interface between a transmitter and transmission media and is thus a very important part of the communication path. The antenna is a passive device, the power radiated by a transmitting antenna cannot be greater than the power entering from the transmitter. The antenna gain in one direction results from a concentration of power and is accompanied by a loss in other directions. The term *active antenna* simply

describes the combination of a receiving antenna with a low noise preamplifier. The antenna will do both transmission and receive with same gain. The conductors in a transmitting antenna must be sized to handle large currents. The task of the transmitting antenna is to convert the electrical energy travelling along a transmission line into electromagnetic waves in space. The energy in the transmission line is contained in the electric field between the conductors and in the magnetic field surrounding them. At the receiving antenna, the electric and magnetic fields in space cause current to flow in the conductors that wake up the antenna. Some of the energy is thereby transferred from these fields to the transmission line connected to the receiving antenna. The isotropic radiator, five-eight wavelength antenna, discone. helical, monopole, ground-plane antenna, loop antenna and half-wave dipole are the common antennas.

30.16 TELEVISION

The television is a very important part of communication systems. Television video systems form pictures by a scanning process. The image is divided into a number of horizontal lines, which are traced out in synchrony at the camera and receiver. The more the number of lines, the more the resolution in the vertical direction. The North American standard uses 525 lines and 625 is used in Europe. In order to make the image visible all at once, rather than as a series of consecutively drawn lines the process must be completed quickly. The more quickly the images follow one another, the less flicker is present. The images/frames sent at the rate of 30 per second to have good response. Frame rates of 25 or 30 Hz cause noticeable flicker; to reduce this, interlaced scan is used. It involves transmitting alternate lines of the picture, then returning and filling in the missing lines. As Fig. 30.20 shows, the picture is scanned from left to right and from top to bottom. The electron beam that traces the picture is blanked during the time intervals in which the beam retraces its path, from right to left and from bottom to top.

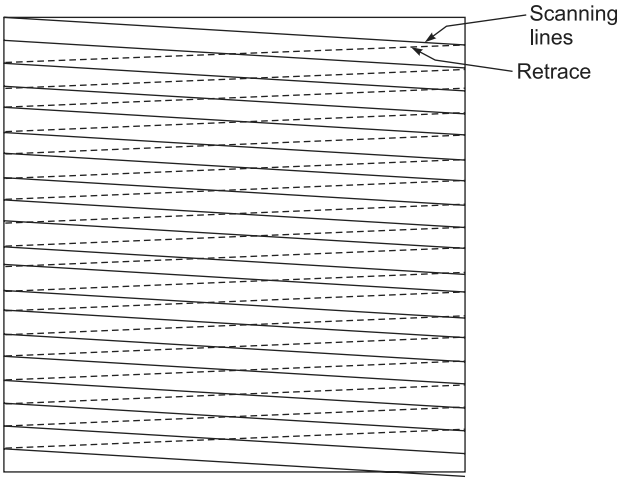


Fig. 30.20 *Interlaced video scanning*

The ratio of width to height as called *aspect ratio* of the image, and its value is 4:3. For 30 Hz frame rate and 525 lines, the transmission rate is $525 \times 30 = 151750$ Hz. Good colour reproduction can be achieved by mixing three primary colours: red, green and blue. So, it is necessary to transmit information for three colours: red, green and blue. Thus considerably more information must be transmitted for colour television than for monochrome. Colour television requires three electron guns in the picture tube. The signal which is sent, with picture information along with synchronising pulses, is called composite video signal. There

are three colour standards mainly used—NTSC (National Television Systems Committee), PAL (Phase Alternation by Line) and SECAM (Sequential Colour and Memory).

Monochrome Cathode Ray Tube

The basic structure of a monochrome CRT is shown in Fig. 30.21. The electron gun emits a beam of electrons, the intensity of which is controlled by the video signal. Inside the electron gun a hot cathode emits electrons. The control grid maintains negative potential with respect to the cathode to accelerate and focusing electrons. As the video signal becomes more positive, the intensity of the electron beam is reduced. The G_2, G_3 and G_4 are used to accelerate and focus the electron beam on the screen.

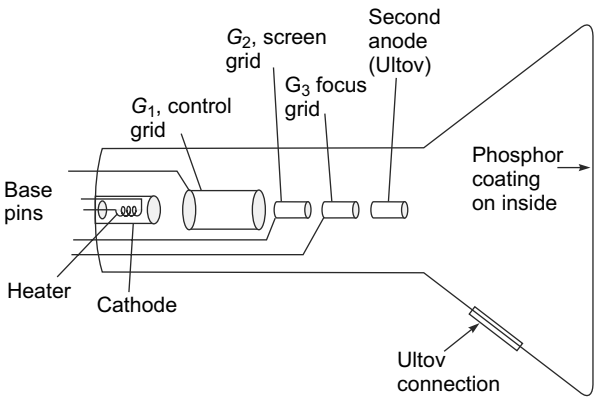


Fig. 30.21 *Cathode ray tube*

The second anode is often called the *ultov*. Its connection is on the flared part of the tube, called the bell to avoid arcing, which could occur as high voltage is applied to the pins at the end of the tube. The electron beams strike a phosphor coating on the inside of the CRT face plate. In colour the cathode tube will have three electron beams from three electron guns arranged either in a triangle (delta gun) or in a straight line (in-line guns). The three video signals are applied at the cathodes, one to each electron gun. The faceplate is covered with a dot pattern using three types of phosphors that glow red, green and blue when bombarded with electrons.

30.17 SATELLITE COMMUNICATION

The first satellite was Echo, a metallised balloon 30 m in diameter that was launched by the United States in 1960 and orbited at a height of about 1600 km. For getting stronger return signals, a repeater must be put into the satellite. The signal path from the earth station transmitter to the satellite receiver is called the *uplink*, and the path from the satellite to the earth is known as the *downlink*. The choice of orbit is an important consideration in satellite-system design. *Geosynchronous orbit* is such an orbit that occupies a circular orbit above the equator at a distance of 35, 784 km above the earth's surface. At the height, the satellite orbital period is equal to the time taken by the earth to rotate once, that is 24 hours. If the direction of the satellite's motion is the same as that of earth's rotation, the satellite appears to remain almost stationary above one spot on the earth's surface. This is called *geostationary orbit*.

One disadvantage of geostationary satellite is the considerable amount of time it takes for a signal to make the round trip from the earth to the satellite one back. Signals received by the satellite are received at one frequency, amplified and moved to another frequency for transmission ray by an equipment called *transponder*. The transmit and receive frequencies are quite widely separated to avoid interference.

Earth stations vary greatly in design, depending on whether they are used to transmit to a satellite as well as to receive its signals, the type of signals in use (television, data, etc.), and the strength of the received signal. Intelsat satellites have antenna beams that cover nearly half the earth, though at a very low received power density. Domestic communication satellites often use spot beams, which cover only one country or part of a large country. Receiving stations for these satellites do not have to be as sophisticated as those used with Intelsat hemispheric beams. Applications of geostationary satellites, are namely television and radio broadcasting, telephony and data transmission.

Satellites in Low and Medium Earth Orbit (LEO, MEO) also possible to avoid high gain antenna and high powered transmitters in the case of geostationary orbit satellites. The problems of having satellites in LEO and MEO are (i) their position in space is not fixed with respect to a ground station, (ii) the annoying tendency of such satellites to disappear below the horizon, and (iii) Doppler effect. Low Earth Orbit (LEO) satellite are positioned from 300 to 1,500 km above the earth. Medium Earth Orbit (MEO) satellites are positioned about 8,000 to 20,000 km in altitude. The gab between LEO to MEO is to avoid the lower of the two Van Allen radiation belts that surround the earth; this radiation can damage the satellite, equipment.

Ref: *Electronic Communication Systems*, 2nd Edition by Thomson Delmar Blake.

30.18 PRINCIPLE OF OPERATIONS OF MOBILE PHONE

A cellular/mobile system provides standard telephone operation by full-duplex two-way radio at remote locations. It provides a wireless connection to the Public Switched Telephone Network (PSTN) from any user location within the radio range of the system.

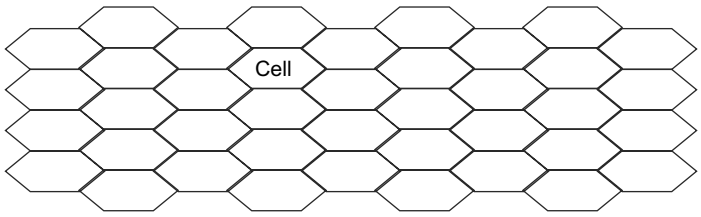


Fig. 30.22 *Cell area*

The basic concept behind the cellular radio system is that rather than serving a given geographical area within a single transmitter and receiver, the system divides the service area into many small areas known as cells as shown in Fig. 30.22. The typical cell covers only several square kilometres and contains its own receiver and low-power transmitter. The cell area shown in Fig. 30.22 is an ideal hexagon. However, in reality they will have circular or other geometric shapes. These areas may overlap and cells may be of different sizes. A basic cellular system consists of mobile stations, base stations and a *Mobile Switching Centre (MSC).* The MSC is also known as *Mobile Telephone Switching Office (MSTO).*

The MSTO controls the cells and provides the interface between each cell and the main telephone office. Each mobile communicates via radio with one of the base stations and may be handed off to any other base station throughout the duration of the call.

Each mobile station consists of a *transceiver*, an antenna and control circuit. The base station consists of several transmitters and receivers which simultaneously handle full-duplex communication and generally have towers which support several transmitting and receiving antennas. The base station serves as a bridge between all mobile users in the cell and connects the simultaneous mobile calls via telephone lines or microwave link to the MSC. The MSC co-ordinates the activities of all the base stations and connects the entire cellular system to the PSTN. Most cellular systems also provide a service known as *roaming*.

The cellular system operates in the 800–900 MHz range. The newer digital cellular system has even greater capacity. Some of these systems operate in 1.7–1.8 GHz bands.

Cellular Telephone Unit

Figure 30.23 shows the block diagram of a cellular mobile radio unit. The unit consists of five major blocks as shown:

1. Control unit
2. Logic unit
3. Receiver
4. Frequency synthesiser
5. Transmitter

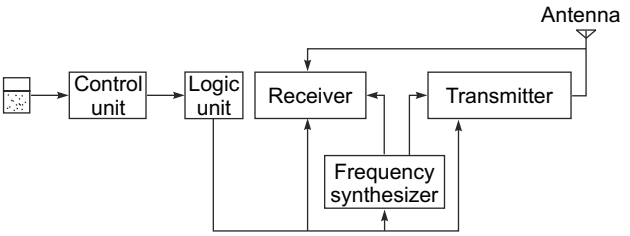


Fig. 30.23 *Block diagram of a cellular mobile radio unit*

References: 1. C.W. Lee, *Mobile/Cellular Communication*
2. *www. itbloas. com/community*

30.19 FAX

FAX is the short form for *facsimile*, also called telecopying, the telephonic transmission of scanned printed material (both text and images) normally to a telephone number connected to a printer or other output device.

Principle of Operation

The original document is scanned with a fax machine, which processes the contents (text or images) as a single fixed graphic image, converting it into a bitmap. The information is then transmitted as electrical signals through the telephone system. The receiving fax machine reconverts the coded image, printing a paper copy.

30.20 ISDN

The Integrated Services Digital network (ISDN) was developed by ITU-T in 1976. It is a set of protocols that combines digital telephony and data transport services. The whole idea is to digitise the telephone network to permit the transmission of audio, video and text over existing telephone lines.

Services

The purpose of the ISDN is to provide fully integrated digital services to users. These services fall into three categories: bearer services, teleservices (Fig. 30.24) and supplementary services. (Fig. 30.24).

❑ **Bearer Services** Bearer services provide the means to transfer information (voice, data and video) between users without the network manipulating the content of that information. The network does not need to process the information and, therefore, does not change the content.

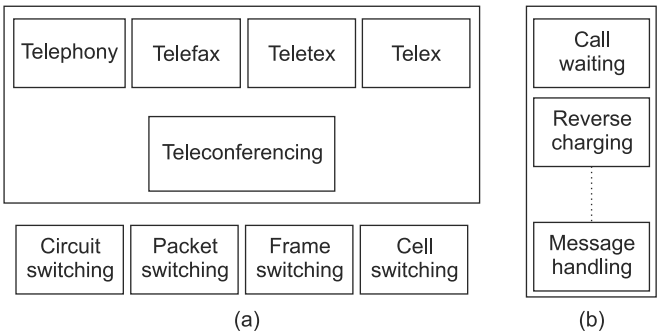


Fig. 30.24 *(a) Teleservices and bearer services (b) Supplementary services*

❑ **Teleservices** In teleservicing, the network may change or process the content of the data.

Teleservices include telephony, telefax, videofax and teleconferencing. Although the ISDN defines these services by name, they have not yet become standards.

❑ **Supplementary Services** Supplementary services are those services that provide additional functionality to the bearer services and teleservices. Examples of these services are reverse charging, call waiting and message handling, all familiar from today's telephone company services.

Integrated Services Digital Network (ISDN) services are much more efficient and flexible than analog services. To receive the maximum benefit from the integrated digital networks, the next step is to replace the analog local loops with digital subscriber loops. Voice transmission can be digitised at the source, thereby removing the final need for analog carriers. In ISDN, all customer services will become digital rather than analog, and the flexibility offered by the new technology will allow customer services to be made available on demand. Most importantly, ISDN will allow all communication connections in a home or building to occur via a single interface.

Figure 30.25 gives a conceptual view of the connections between users and an ISDN central office. Each user is linked to the central office through a digital pipe. These pipes can be of different capacities to allow different rates of transmission and support different subscriber needs.

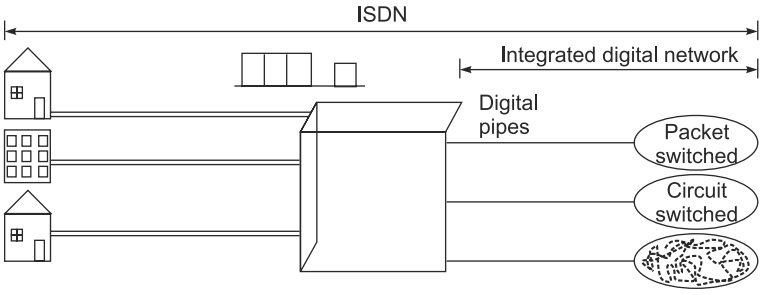


Fig. 30.25 *ISDN*

There are three types of ISDN channels:

1. Bearer (B Channels)
2. Data (D Channels)
3. Hybrid (H Channels)

❑ **B Channels** A bearer channel is defined at a rate of 64 kbps.

❑ **D Channels** A data channel can be either of 16 or 64 kbps, depending on the need of the users. Although the name says data, the primary function of a D Channel is to carry control signalling for the B Channels.

❑ **H Channels** Hybrid channels are available with data rates of 384 kbps, 1536 kbps, or 1920 kbps. These rates suit H Channels for high data rate applications such as video, teleconferencing and many more digital techniques.

30.21 MICROWAVE COMMUNICATION

Microwave communication is the transmission of signals via radio using a series of microwave towers. Microwave communication is known as a form of "Line of Sight" communication, because there must be nothing obstructing the transmission of data between these towers for signals to be properly sent and received.

Microwave Communication History

Microwave communication technology was developed in the early 1940's by the Western union.

With the development of satellite and cellular technologies, microwave is now less widely used in the telecommunication industry.

Means of Microwave Communication

Microwave communication takes place both by analog and digital formats. While digital is the most advanced form of microwave communication, both analog and digital methods pose certain benefits for the users.

Economical Option

Analog microwave communication may be most economical for users at the tower site simply because it is already paid for and in service. If we are already operating a microwave component, it is most likely analog.

Digital Microwave Options

Digital microwave communication utilises more advanced, more reliable technology. It is much easier to find equipment to support this transmission method because it is the newer form of microwave communication. Because it has a higher bandwidth, it also allows to transmit more data using more verbose protocols. The increased speeds will also decrease the time it takes to select your microwave site equipment.

Frequencies Available for Microwave Communication

It covers the frequency range from UHF to EHF.

Bands UHF (Ultra High Frequency): 300 MHz to 3 GHz

EHF (Extremely High Frequency): 30 GHz to 300 GHz

30.22 OPTICAL FIBRE COMMUNICATION

- Fibre optics deals with the transmission of light through fibres of glass, plastic or other transparent materials and works on the principle of total internal reflection.

- In electronic communication, optical fibres are preferred over copper wires because they are extremely light, small and can be accommodated in a small space. By using optical fibres, the number of signals that can be transmitted simultaneously is enhanced.
- After the availability of LASER in 1960, there has been fast growth in the field of fibre optics. Optical fibres and LASERs together increase the capacity of communication system by one lakh times the conventional system.
- In 1973, the Airborne Light Optical Fibre Technology (ALOFT) program replaced 302 cables, which weighed 40 kg by the fibre system weighing only 1.7 kg.
- By the late 1970s and early 1980s, every major telephone communication company was rapidly installing new and more efficient fibre system
- In optical region of electromagnetic spectrum, the transmission of information is carried out not by frequency modulation of the carrier, but by varying the intensity of optical power. This is known as *optical communication*.

30.22.1 Block Diagram of Optical Fibre Communication

The basic fibre optic transmission system consists of three basic elements (Fig. 30.26):

1. The optical transmitter
2. The fibre optic cable
3. The optical receiver

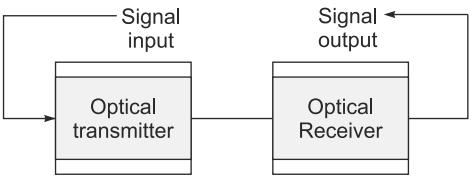


Fig. 30.26 *The basic communication system*

The *transmitter* converts an electrical analog or digital signal into a corresponding optical signal. The source of optical signal can be either a Light Emitting Diode (LEDs) or a laser diode. The block diagram of optical fibre communication is given in Fig. 30.27.

The transmission medium in optical fibre communication system is an *optical fibre cable*. It is a very thin and flexible medium that guides light from an optical transmitter to an optical receiver. The cable consists of one or more glass fibres, which acts as waveguides for the optical signal.

The *receiver* converts optical signals back into a replica of the original electrical signal. The detector of the optical signal is either a PIN-type photodiode or avalanche type photodiode.

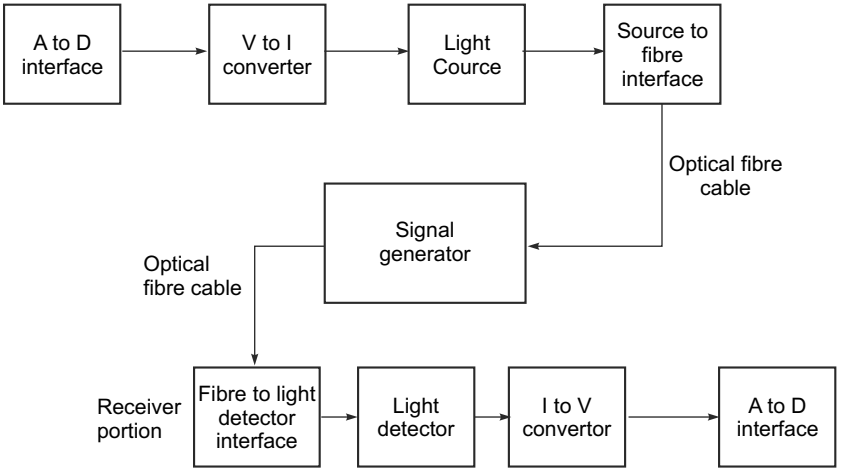


Fig. 30.27 *Block diagram of optical fibre communication*

30.22.2 Advantages of Optical Fibres

❑ **Long Distance Transmission** Optical fibres have lower transmission losses compared to copper wires. Data can be transmitted over longer distances.

❑ **Large Information Capacity** Optical fibres have wider bandwidth than copper wires. This property decreases the number of physical lines required for sending a given amount of information.

❑ **Small Size and Low Weight** The low weight and the small dimensions of fibre offers a distinct advantage over heavy wire cables in crowded underground city ducts or in ceiling mounted cable trays.

❑ **Immunity to Electrical Interference** An especially important feature of an optical fibre relates to the fact that it is a dielectric material which means it does not conduct electricity.

❑ **Enhanced Safety** Optical fibres offer a high degree of operational safety, since they do not have the problems of ground loops, sparks and potentially high voltages inherent in copper lines.

❑ **Increased Signal Security** The optical signal is well confined within the fibre and an opaque coating around the fibre absorbs any signal emission.

30.22.3 Application of Optical Fibre Communication

1. Optical Fibre Communication (OFC) proves efficient and cost effective in public network application.
2. Fibre optical cables can be used under the sea.
3. Public utility organisations like railways, TV transmissions etc. find tremendous use of OFC.
4. Colleges, universities, offices, industrial plants, etc. employ optical fibres within their LAN (Local Area Network) systems.
5. Fibre optic is widely used in telecommunication such as voice telephones, video phones, telegraph services, message services, etc.

Summary

- ➢ Communication systems have been introduced.
- ➢ Various types of modulations discussed.
- ➢ Digital modulation and digital communication have been explained.
- ➢ Different types of communications have been dealtwith.

Exercises

Review Questions

1. What are advantages of digital communication over analog communication?
2. What is the approximate frequency range of operation of cellulor telephony?
3. Which types of modulation is resistant to channel noise—AM or PM? Explain why.
4. What is the difference between sensitivity and selectivity of a receiver?
5. A 2 mV (peak to peak) the signal varying between –1 mV to +1 mV is quantised using 64 levels. What is the number of bits required to represent one sample of the quantised signal?

6. In AM, what is the maximum value of modulation index. Why cannot it be more than that?
7. Explain how frequency modulation is accomplished using CVO.
8. Define modulation index of FM.
9. What is wideband FM?
10. Write the expression of the bandwidth of FM.
11. In TV signal transmission, why is AM is used for video signals and FM for audio signals?
12. Which modulated signal has higher bandwidth—AM or FM?
13. What are BSB–SC signals and SSB–SC signals? Compare the transmission channel bandwidth needed for these kinds of signals.
14. What is meant by base-band?
15. Sketch the spectrum of AM signal.
16. Write a brief account of VCO.
17. Draw the block diagram of PLL. How is FM demodulation achieved by PLL.
18. What conditions must be met by the time constant of the AM demodulation circuit?
19. Distinguish between asynchronous and synchronous data transmission.
20. Describe the function of a modem.
21. What is meant by encryption? What are the two main types of encryption.
22. In satellite communication what is a transponder?
23. Describe interlaced video screening. Relate it to the transmission rate.
24. In digital modulation by FSK, drawn the signal waveform for data 0100110. Also, draw the signal for PSK. Which is easier to implement?
25. Compare and distinguish AM demodulation and pulse demodulation.
26. What is a tank circuit. Describe the circuit operation.
27. Why super-heterodyne method is used in radio receivers?

Multiple-Choice Questions

1. The following is not the purpose of modulation:
   (a) Multiplexing (b) Effective radiation
   (c) Narrow banding (d) Increase in signal power
2. The modulation index of an AM wave is changed from 0 to 1. The transmitted power is
   (a) halved (b) increased by 50% (c) quadrupled (d) unchanged
3. Which one is an advantage of AM over FM?
   (a) FM has wide bandwidth
   (b) Probability of noise spike generation is less in AM.
   (c) FM has better fidelity
   (d) FM is more immune to noise
4. The following is not an advantage of FM over AM
   (a) Sputtering effect (b) Capture effect (c) Fidelity (d) Noise immunity
5. Which of the following modulations is digital in nature?
   (a) PPM (b) PAM (c) DM (d) None of these
6. Quantisation noise occurs in
   (a) PAM (b) PWM (c) DM (d) None of these
7. In a single-tone FM discriminator, (S/N) is
   (a) proportional to square of deviation (b) inversely proportional to deviation
   (c) proportional to cube of deviation (d) proportional to deviation.

8. A PAM signal can be detected by using
   (a) an integrator (b) a band-pass filter (c) a high-pass filter (d) low-pass filter
9. Flat-top sampling leads to
   (a) an aperture effect (b) aliasing (c) loss of signal (d) none of these
10. Pulse stuffing is used in
   (a) synchronous TDM (b) any TDM (c) asynchronous TDM (d) none of these

Answers

Multiple-Choice Questions

1. (d) 2. (b) 3. (a) 4. () 5. (c) 6. (c) 7. (a) 8. (d) 9. (a) 10. (c)

Frequency Response of the FET Amplifier

appendix A

A.1 FREQUENCY RESPONSE OF THE FET AMPLIFIER

The typical frequency response of an amplifier is presented in the form of a graph that shows output amplitude (or, more often, voltage gain) plotted versus log frequency. The typical plot of the voltage gain is shown in Fig. A.1. The gain is null at zero frequency, then rises as frequency increases, levels off for further increases in frequency, and then begins to drop again at high frequencies. The frequency response of an amplifier can be divided into three frequency regions.

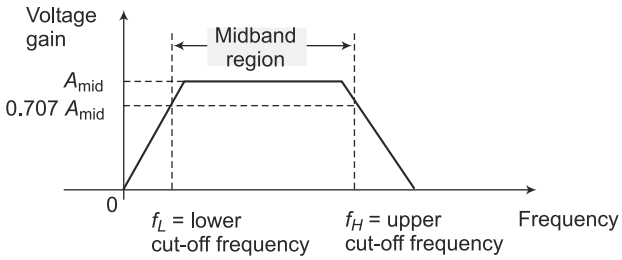


Fig. A.1 *Diagram of voltage gain versus frequency for an amplifier*

The frequency response begins with the lower frequency region designated between 0 Hz and lower cut-off frequency. At lower cut-off frequency, f_L, the gain is equal to 0.707 A_{mid}. A_{mid} is a constant midband gain obtained from the midband frequency region. The third region, the upper frequency region, covers frequency between upper cut-off frequency and above. Similarly, at upper cut-off frequency, f_H, the gain is equal to 0.707 A_{mid}. After the upper cut-off frequency, the gain decreases with frequency increase and dies off eventually.

The Lower Frequency Response

Since the impedance of coupling capacitors increases as frequency decreases, the voltage gain of a FET amplifier decreases as frequency decreases. At very low frequencies, the capacitive reactance of the coupling capacitors may become large enough to drop some of the input voltage or output voltage. Also,

the emitter-bypass capacitor may become large enough so that it no longer shorts the emitter resistor to ground. Approximately, the following equations can be used to determine the lower cut-off frequency of the amplifier, where the voltage gain drops 3 dB from its midband value (= 0.707 times the midband A_{mid}):

(1) $f_1 = 1/(2\pi r_{in} C_1)$ where:
f_1 = lower cut-off frequency due to C_1
C_1 = input coupling capacitance
r_{in} = input resistance of the amplifier

(2) $f_2 = 1/(2\pi r_{out} C_2)$ where:
f_2 = lower cut-off frequency due to C_2
C_2 = output coupling capacitance
r_{out} = output resistance of the amplifier

Provided that f_1 and f_2, are not close in value, the actual lower cut-off frequency is approximately equal to the largest of the two.

The Upper Frequency Response

Transistors have inherent shunt capacitances between each pair of terminals. At high frequencies, these capacitances effectively short the ac signal voltage.

A.2 THE CLASS B AMPLIFIER

To improve the full power efficiency of the previous Class A amplifier by reducing the wasted power in the form of heat, it is possible to design the power amplifier circuit with two transistors in its output stage producing what is commonly termed as a **Class B amplifier** also known as a **push-pull amplifier** configuration.

Push-pull amplifiers use two "complementary" or matching transistors, one being an *NPN*-type and the other being a *PNP*-type with both power transistors receiving the same input signal together that is equal in magnitude, but in opposite phase to each other. This results in one transistor only amplifying one half or 180° of the input waveform cycle while the other transistor amplifies the other half or remaining 180° of the input waveform cycle with the resulting "two halves" being put back together again at the output terminal.

Then the conduction angle for this type of amplifier circuit is only 180° or 50% of the input signal. This pushing and pulling effect of the alternating half cycles by the transistors gives this type of circuit its amusing "push-pull" name, but more generally known as the **Class B amplifier** shown in Fig. A.2.

The circuit above shows a standard **Class B amplifier** circuit that uses a balanced centre-tapped input transformer, which splits the incoming waveform signal into two equal halves and which are 180° out of phase with each other. Another centre-tapped transformer on the output is used to recombine the two signals providing the increased power to the load. The transistors used for this type of transformer push-pull amplifier circuit are both *NPN* transistors with their emitter terminals connected together.

Here, the load current is shared between the two power transistor devices as it decreases in one device and increases in the other throughout the signal cycle reducing the output voltage and current to zero. The result is that both halves of the output waveform now swing from zero to twice the quiescent current, thereby reducing dissipation. This has the effect of almost doubling the efficiency of the amplifier to around 70%.

Assuming that no input signal is present, each transistor carries the normal quiescent collector current, the value of which is determined by the base bias which is at the cut-off point. If the transformer is accurately centre tapped then the two collector currents will flow in opposite directions (ideal condition) and there will be no magnetisation of the transformer core, thus minimising the possibility of distortion.

When an input signal is present across the secondary of the driver transformer T_1, the transistor base inputs are in "anti-phase" to each other as shown. Thus, if TR_1 base goes positive, driving the transistor into heavy conduction, its collector current will increase but at the same time the base current of TR_2 will go negative further into cut-off and the collector current of this transistor decreases by an equal amount and

vice versa. Hence, negative halves are amplified by one transistor and positive halves by the other transistor, giving this push-pull effect.

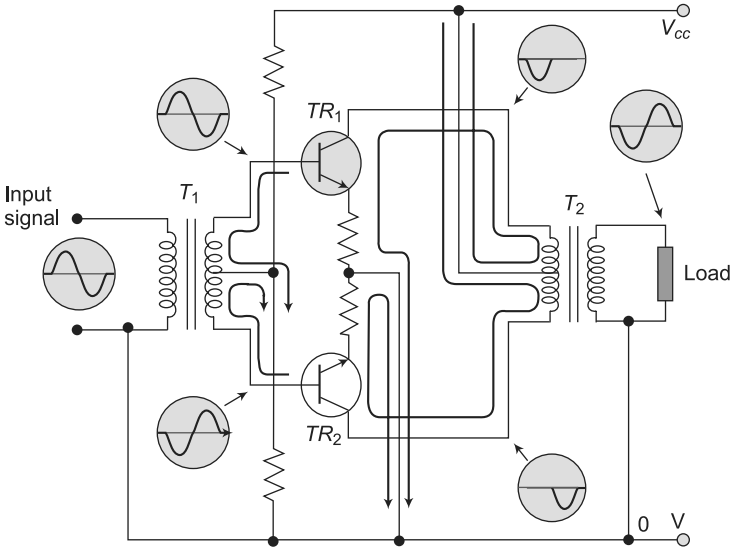


Fig. A.2 *Class B push-pull transformer amplifier circuit*

Unlike dc condition, these ac currents are additive resulting in the two output half-cycles being combined to reform the sine wave in the output transformer's primary winding which then appears across the load.

Class B amplifier operation has zero dc bias as the transistors are biased at the cut-off, so each transistor only conducts when the input signal is greater than the base-emitter voltage. Therefore, at zero input, there is zero output and no power is being consumed. This then means that the actual Q-point of a Class B amplifier is on the V_{ce} part of the load line as shown in Fig. A.3.

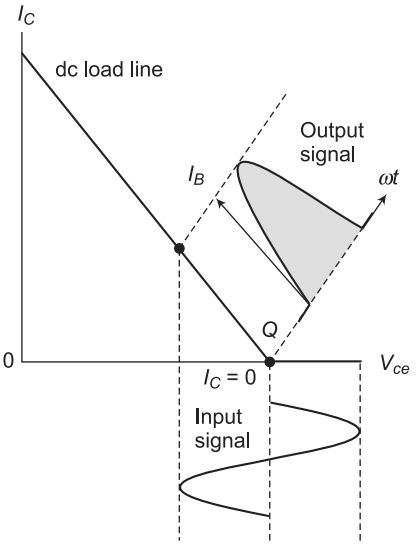


Fig. A.3 *Class B output characteristics curves*

The **Class B amplifier** has the big advantage over their Class A amplifier cousins in that no current flows through the transistors when they are in their quiescent state (i.e. with no input signal). Therefore, no power is dissipated in the output transistors or transformer when there is no signal present unlike Class A amplifier stages that require significant base bias, thereby dissipating lots of heat—even with no input signal present. So the overall conversion efficiency (η) of the amplifier is greater than that of the equivalent Class A with efficiencies reaching as high as 70% possible resulting in nearly all modern types of push-pull amplifiers operated in this Class B mode.

Transformerless Class B Push-Pull Amplifier

One of the main disadvantages of the Class B amplifier circuit above is that it uses balanced centre-tapped transformers in its design, making it expensive to construct. However, there is another type of Class B amplifier called a **complementary-symmetry Class B amplifier** that does not use transformers in its design. Therefore, it is transformerless, using instead complementary or matching pairs of power transistors. As transformers are not needed, this makes the amplifier circuit much smaller for the same amount of output. Also, there are no stray magnetic effects or transformer distortion to effect the quality of the output signal. An example of a "transformerless" Class B amplifier circuit is given below.

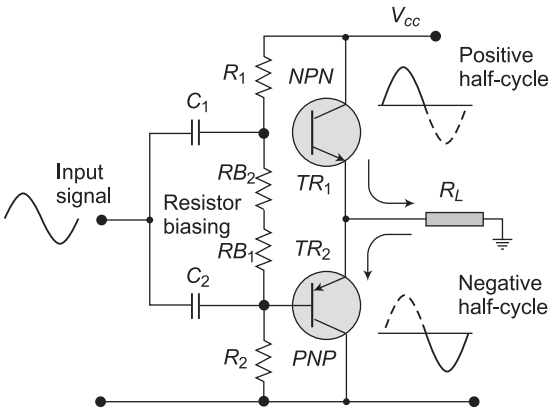


Fig. A.4 *Class B transformerless output stage*

The Class B amplifier circuit above uses complementary transistors for each half of the waveform and while Class B amplifiers have a much high gain than the Class A types, one of the main disadvantages of Class B type push-pull amplifiers is that they suffer from an effect known commonly as **crossover distortion**.

Hopefully, we remember from our tutorials about transistors that it takes approximately 0.7 volt (measured from base to emitter) to get a bipolar transistor to start conducting. In a pure Class B amplifier, the output transistors are not "pre-biased" to an "ON" state of operation.

This means that the part of the output waveform which falls below this 0.7 volt window will not be reproduced accurately as during the transition between the two transistors (when they are switching over from one transistor to the other), the transistors do not stop or start conducting exactly at the zero crossover point even if they are specially matched pairs. The output transistors for each half of the waveform (positive and negative) will each have a 0.7 volt area in which they are not conducting. The result is that both transistors are turned "OFF" at exactly the same time.

A simple way to eliminate crossover distortion in a Class B amplifier is to add two small voltage sources to the circuit to bias both the transistors at a point slightly above their cut-off point. This then would give us what is commonly called a **Class AB amplifier** circuit. However, it is impractical to add additional voltage

sources to the amplifier circuit, so *pn*-junctions are used to provide the additional bias in the form of silicon diodes.

The Class AB Amplifier

We know that we need the base-emitter voltage to be greater than 0.7 V for a silicon bipolar transistor to start conducting. So if we were to replace the two voltage divider biasing resistors connected to the base terminals of the transistors with two silicon diodes, the biasing voltage applied to the transistors would now be equal to the forward voltage drop of the diode. These two diodes are generally called **biasing diodes** or **compensating diodes** and are chosen to match the characteristics of the matching transistors. The circuit below shows diode biasing.

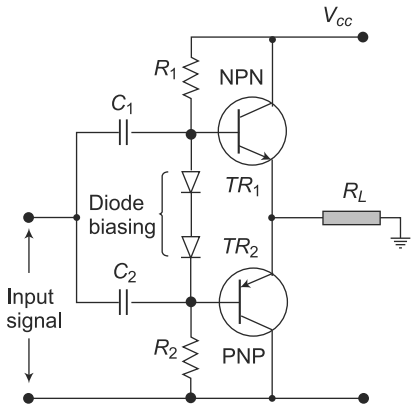


Fig. A.5 *Class AB amplifier*

The **Class AB amplifier** circuit is a compromise between the Class A and the Class B configurations. This very small diode-biasing voltage causes both transistors to slightly conduct even when no input signal is present. An input signal waveform will cause the transistors to operate as normal in their active region, thereby eliminating any crossover distortion present in pure Class B amplifier designs.

A small collector current will flow when there is no input signal but it is much less than that for the Class A amplifier configuration. This means then that the transistor will be "ON" for more than half a cycle of the waveform but much less than a full cycle giving a conduction angle of between 180° to 360° or 50% to 100% of the input signal depending upon the amount of additional biasing used. The amount of diode-biasing voltage present at the base terminal of the transistor can be increased in multiples by adding additional diodes in series.

Class B amplifiers are greatly preferred over Class A designs for high-power applications such as audio power amplifiers and PA systems. Like the Class A amplifier circuit, one way to greatly boost the current gain (A_i) of a Class B push-pull amplifier is to use Darlington transistor pairs instead of single transistors in its output circuitry.

A.3 RIGHT-HAND RULE

In mathematics and physics, the **right-hand rule** is a common mnemonic for understanding notation conventions for vectors in three dimensions. It was invented for use in electromagnetism by the British physicist John Ambrose Fleming in the late 19th century.

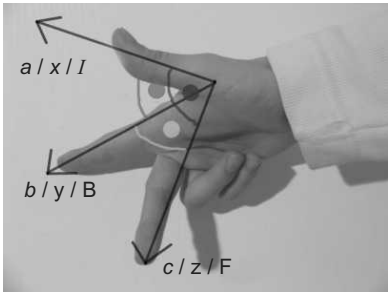


Fig. A.6 *Right-hand rule*

When choosing three vectors that must be at right angles to each other, there are two distinct solutions. Thus, when expressing this idea in mathematics, one must remove the ambiguity of which solution is meant.

There are variations on the mnemonic depending on context, but all variations are related to the one idea of choosing a convention.

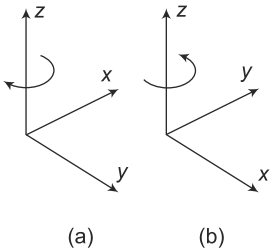


Fig. A.7 *(a) Left-handed orientation (b) Right-hand orientation*

Right-handed and Left-handed Coordinates

Let the *X* and *Y* axes define a horizontal plane with the *X*-axis pointing toward you. Then the *Z*-axis can either point up (right-handed) or down (left-handed). If the coordinates are right-handed and you place your right fist on the plane then your fingers will curl from the first or *X*-axis to the second or *Y*-axis and your thumb will point along the *Z*-axis. If the coordinates were left-handed, the fingers of your left hand would curl from the first axis to the second and your left thumb would point along the *Z*-axis.

If any one axis is reversed, the handedness changes. To preserve handedness, one of the other axes must also reverse which is equivalent to switching the labels on the other two axes. Note that the handedness of coordinates has no meaning unless the axes are labelled in sequence: 1,2,3 or *x*, *y*, *z*.

Applications

The first form of the rule is used to determine the direction of the cross product of two vectors. This leads to widespread use in physics, wherever the cross product occurs. A list of physical quantities whose directions are related by the right-hand rule is given below. (Some of these are related only indirectly to cross products, and use the second form.)

- The angular velocity of a rotating object and the rotational velocity of any point on the object
- A torque, the force that causes it, and the position of the point of application of the force
- A magnetic field, the position of the point where it is determined, and the electric current (or change in electric flux) that causes it

- A magnetic field in a coil of wire and the electric current in the wire
- The force of a magnetic field on a charged particle, the magnetic field itself, and the velocity of the object
- The vorticity at any point in the field of flow of a fluid
- The induced current from motion in a magnetic field (known as Fleming's right-hand rule)
- The x, y and z unit vectors in a Cartesian coordinate system can be chosen to follow the right-hand rule
- Right-handed coordinate systems are often used in rigid body physics and kinematics.

A.4 LEFT-HAND RULE

In certain situations, it may be useful to use the opposite convention, where one of the vectors is reversed and so creates a left-handed triad instead of a right-handed triad.

An example of this situation is for left-handed materials. Normally, for an electromagnetic wave, the electric and magnetic fields, and the direction of propagation of the wave obey the right-handed rule. However, left-handed materials have special properties, notably the **negative refractive index**. It makes the direction of propagation point in the opposite direction.

De Graaf's translation of Fleming's left-hand rule—which uses thrust, field and current—and the right-hand rule, is the FBI rule. The **FBI rule** changes thrust into F (Lorentz force), B (direction of the magnetic field) and I (current). The FBI rule is easily remembered by US citizens because of the commonly known abbreviation for the Federal Bureau of Investigation.

Fleming's left-hand rule is a rule for finding the direction of the thrust on a conductor carrying a current in a magnetic field.

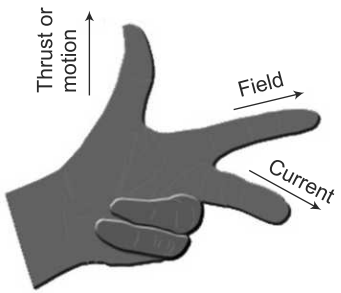


Fig. A.8 *Left-hand rule*

Symmetry

Vector	Right hand	Right hand	Right hand	Left hand	Left hand	Left Hand
a, x or I	Thumb	Fingers or palm	First or index	Thumb	Fingers or palm	First or index
b, y or B	First or index	Thumb	Fingers or palm	Fingers or palm	First or index	Thumb
c, z or F	Fingers or palm	First or index	Thumb	First or index	Thumb	Fingers or palm

A.5 HALL EFFECT

The Hall effect is due to the nature of the current in a conductor. Current consists of the movement of many small charge carriers, typically electrons, holes, ions or all three. When a magnetic field is present, which is not parallel to the direction of motion of moving charges, these charges experience a force, called the **Lorentz force**. When such a magnetic field is absent, the charges follow approximately straight, 'line of sight' paths between collisions with impurities, photons, etc. However, when a magnetic field with a perpendicular component is applied, their paths between collisions are curved so that moving charges accumulate on one face of the material. This leaves equal and opposite charges exposed on the other face, where there is a scarcity of mobile charges. The result is an asymmetric distribution of charge density across the Hall element, perpendicular to both the 'line of sight' path and the applied magnetic field. The separation of charge establishes an electric field that opposes the migration of further charge. Hence, a steady electrical potential is established for as long as the charge is flowing.

In the classical view, there are only electrons moving in the same average direction both in the case of electron or hole conductivity. This cannot explain the opposite sign of the Hall effect observed. The difference is that electrons in the upper bound of the valence band have opposite group velocity and wave vector direction when moving, which can be effectively treated as if positively charged particles (holes) moved in the opposite direction to that of the electrons.

Refer Fig. A.9. Initially, the electrons follow the curved arrow, due to the magnetic force. After a short time, electrons pile up on the left side and deplete from the right side, which creates an electric field ξ_y. In steady state, ξ_y will be strong enough to exactly cancel out the magnetic force so that the electrons follow the straight arrow (dashed).

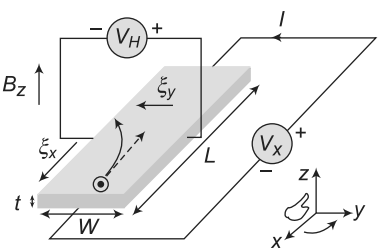


Fig. A.9 *Hall-effect measurement set-up for electrons*

For a simple metal, where there is only one type of charge carrier (electrons), the Hall voltage V_H is given by

$$V_H = -\frac{IB}{net}$$

where I is the current across the plate length, B is the magnetic field, t is the thickness of the plate, e is the elementary charge, and n is the charge carrier density of the carrier electrons.

The Hall coefficient is defined as

$$R_H = \frac{E_y}{j_x B}$$

where j is the current density of the carrier electrons, and E_y is the induced electric field. In SI units, this becomes

$$R_H = \frac{E_y}{j_x B} = \frac{V_H t}{IB} = -\frac{1}{ne}$$

(The units of R_H are usually expressed as m^3/C, or Ω·cm/G, or other variants.) As a result, the Hall effect is very useful as a means to measure either the carrier density or the magnetic field.

One very important feature of the Hall effect is that it differentiates between positive charges moving in one direction and negative charges moving in the opposite. The Hall effect offered the first real proof that electric currents in metals are carried by moving electrons, not by protons. The Hall effect also showed that in some substances (especially *p*-type semiconductors), it is more appropriate to think of the current as positive "holes" moving rather than negative electrons. A common source of confusion with the Hall effect

is that holes moving to the left are really electrons moving to the right; so one expects the same sign of the Hall coefficient for both electrons and holes. This confusion, however, can only be resolved by modern quantum mechanical theory of transport in solids.

The sample in homogeneity might result in spurious sign of the Hall effect, even in ideal van der Pauw configuration of electrodes. For example, positive Hall effect was observed in evidently *n*-type semiconductors.

Hall Effect in Semiconductors

When a current-carrying semiconductor is kept in a magnetic field, the charge carriers of the semiconductor experience a force in a direction perpendicular to both the magnetic field and the current. At equilibrium, a voltage appears at the semiconductor edges.

The simple formula for the Hall coefficient given above becomes more complex in semiconductors where the carriers are generally both electrons and holes which may be present in different concentrations and have different mobilities. For moderate magnetic fields, the Hall coefficient is

$$R_H = \frac{p\mu_h^2 - n\mu_e^2}{e(p\mu_h + n\mu_e)^2}$$

where n is the electron concentration, p is the hole concentration, μ_e is the electron mobility, μ_h is the hole mobility and e is the absolute value of the electronic charge.

For large applied fields, the simpler expression analogous to that for a single carrier type holds.

$$R_H = \frac{(p - nb^2)}{e(p + nb)^2}$$

with

$$b = \frac{\mu_e}{\mu_h}$$

Quantum Hall Effect

For a two-dimensional electron system which can be produced in a MOSFET, in the presence of large magnetic field strength and low temperature, one can observe the quantum Hall effect, which is the quantisation of the Hall voltage.

Spin Hall Effect

The spin Hall effect consists in the spin accumulation on the lateral boundaries of a current-carrying sample. No magnetic field is needed. It was predicted by M I Dyakonov and V I Perel in 1971 and observed experimentally more than 30 years later, both in semiconductors and in metals, at cryogenic as well as at room temperatures.

Quantum Spin Hall Effect

The quantum spin Hall effect has been recently observed for mercury telluride two-dimensional quantum wells with strong spin-orbit coupling, in zero magnetic field, at low temperature.

Anomalous Hall Effect

In ferromagnetic materials (and paramagnetic materials in a magnetic field), the Hall resistivity includes an additional contribution, known as the **anomalous Hall effect** (or the **extraordinary Hall effect**), which depends directly on the magnetisation of the material, and is often much larger than the ordinary Hall effect.

(Note that this effect is *not* due to the contribution of the magnetisation to the total magnetic field.) For example, in nickel, the anomalous Hall coefficient is about 100 times larger than the ordinary Hall coefficient near the Curie temperature, but the two are similar at very low temperatures. Although a well-recognised phenomenon, there is still debate about its origins in the various materials. The anomalous Hall effect can be either an *extrinsic* (disorder-related) effect due to spin-dependent scattering of the charge carriers, or an *intrinsic* effect which can be described in terms of the **Berry phase effect** in the crystal momentum space (k-space).

Hall Effect in Ionised Gases

The Hall effect in an ionised gas (plasma) is significantly different from the Hall effect in solids (where the **Hall parameter** is always very inferior to unity). In a plasma, the Hall parameter can take any value. The Hall parameter, β, in a plasma is the ratio between the electron gyrofrequency, Ω_e, and the electron-heavy particle collision frequency, ν:

$$\beta = \frac{\Omega_e}{\nu} = \frac{eB}{m_e \nu}$$

where

- e is the elementary charge (approx. 1.6×10^{-19} C)
- B is the magnetic field (in tesla)
- m_e is the electron mass (approx. 9.1×10^{-31} kg).

The Hall parameter value increases with the magnetic field strength.

Physically, the trajectories of electrons are curved by the Lorentz force. Nevertheless, when the Hall parameter is low, their motion between two encounters with heavy particles (neutral or ion) is almost linear. But if the Hall parameter is high, the electron movements are highly curved. The current density vector, J, is no longer collinear with the electric field vector, E. The two vectors J and E make the **Hall angle**, θ, which also gives the Hall parameter:

$$\beta = \tan(\theta)$$

Applications

Hall probes are often used as magnetometers, i.e. to measure magnetic fields, or inspect materials (such as tubing or pipelines), using the principles of magnetic flux leakage.

Hall-effect devices produce a very low signal level and thus require amplification. While suitable for laboratory instruments, the vacuum-tube amplifiers available in the first half of the 20th century were too expensive, power consuming, and unreliable for everyday applications. It was only with the development of the low-cost integrated circuit that the Hall-effect sensor became suitable for mass application. Many devices now sold as Hall-effect sensors in fact contain both the sensor as described above plus a high-gain Integrated Circuit (IC) amplifier in a single package. Recent advances have further added into one package an analog-to-digital converter and I²C (Inter-integrated circuit communication protocol) IC for direct connection to a microcontroller's I/O port.

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Capacitive Sensors

appendix B

There are several physical effects, which result in the direct generation of electrical signals in response to non-electrical influences and thus can be used in direct sensors. Examples are thermoelectric (Seebeck) effect, piezoelectricity, and photo effect. Let us take two isolated conductive objects of arbitrary shape (plates) and connect them to the opposite poles of a battery. The plates will receive equal amounts of opposite charges; i.e. a negatively charged plate will receive additional electrons while there will be a deficiency of electrons in the positively charged plate. Now, let us disconnect the battery. If the plates are totally isolated and exist in a vacuum, they will remain charged theoretically infinitely long. A combination of plates, which can hold an electric charge is called a *capacitor*. If a small *positive* electric test charge, q_0, is positioned between the charged objects, it will be subjected to an electric force from the positive plate to the negative. The positive plate will repel the test charge and the negative plate will attract it, resulting in a combined push-pull force. Depending on the position of the test charge between the oppositely charged objects, the force will have a specific magnitude and direction, which is characterized by vector **f**.

The capacitor may be characterized by q, the magnitude of the charge on either conductor, and by V, the positive potential difference between the conductors. It should be noted that q is not a net charge on the capacitor, which is zero. Further, V is not the potential of either plate, but the potential difference between them. The ratio of charge to voltage is constant for each capacitor: $q/V = C$.

This fixed ratio, C, is called the *capacitance* of the capacitor. Its value depends on the shapes and relative position of the plates. C also depends on the medium in which the plates are immersed.

Capacitance is a very useful physical phenomenon in a sensor designer's toolbox. It can be successfully applied to measure distance, area, volume, pressure, force, and so forth. The following background establishes fundamental properties of the capacitor and gives some useful equations.

Parallel-plate Capacitor

In a parallel-plate capacitor, in which the conductors take the form of two plane parallel plates of area A separated by a distance d. If d is much smaller than the plate dimensions, the electric field between the plates will be uniform, which means that the field lines (lines of force **f**) will be parallel and evenly spaced. To calculate the capacitance, we must relate V, the potential difference between the plates, to q, the capacitor charge:

$$C = q/V \tag{B.1}$$

Alternatively, the capacitance of a flat capacitor can be found from

$$C = \varepsilon_0 A/d \tag{B.2}$$

The above formula is important for the capacitive sensor's design. It establishes a relationship between the plate area and the distance between the plates. Varying either of them will change the capacitor's value, which can be measured quite accurately by an appropriate circuit. It should be noted that the above equations hold only for capacitors of the parallel type. A change in geometry will require modified formulas. The ratio *A/d* may be called a *geometry factor* for a parallel-plate capacitor.

Cylindrical Capacitor

A cylindrical capacitor consists of two coaxial cylinders of radii a and b and length l. For the case when $l \gg b$, we can ignore fringing effects and calculate capacitance from the following formula:

$$C = 2\pi\varepsilon_0 l / \ln(b/a).$$

In this formula, l is the length of the overlapping conductors and $2\pi l[\ln(b/a)]^{-1}$ is called a *geometry factor* for a coaxial capacitor. A useful displacement sensor can be built with such a capacitor if the inner conductor can be moved in and out of the outer conductor. According to the above equation, the capacitance of such a sensor is in a linear relationship with the displacement, l.

Capacitive Occupancy Detectors

Being a conductive medium with a high dielectric constant, a human body develops a coupling capacitance to its surroundings. This capacitance greatly depends on such factors as body size, clothing, materials, type of surrounding objects, weather, and so forth. However wide the coupling range is, the capacitance may vary from a few picofarads to several nanofarads. When a person moves, the coupling capacitance changes, thus making it possible to discriminate static objects from the moving ones. In effect, all objects form some degree of a capacitive coupling with respect to one another. If a human (or, for that purpose, anything) moves into the vicinity of the objects whose coupling capacitance with each other has been previously established, a new capacitive value arises between the objects as a result of the presence of an intruding body.

Capacitive Sensors

The capacitive displacement sensors have very broad applications, they are employed directly to gauge displacement and position and also as building blocks in other sensors where displacements are produced by force, pressure, temperature, and so forth. The ability of capacitive detectors to sense virtually all materials makes them an attractive choice for many applications. Equation (B.2) states that the capacitance of a flat capacitor is inversely proportional to the distance between the plates. The operating principle of a capacitive gauge, proximity, and position sensors is based on either changing the geometry (i.e. a distance between the capacitor plates) or capacitance variations in the presence of conductive or dielectric materials. When the capacitance changes, it can be converted into a variable electrical signal. As with many sensors, a capacitive sensor can be either monopolar (using just one capacitor) or differential (using two capacitors), or a capacitive bridge can be employed (using four capacitors). When two or four capacitors are used, one or two capacitors may be either fixed or variable with the opposite phase.

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